Problem 1. (20 points) The following instructions executed on a 5-stage pipelined datapath:

I.   If there is no forwarding or hazard detection, insert NOPS to ensure correct execution. (Hint: for the first sw instruction, register r1 needs to be written first by "add" instruction and then sw instruction can read it.)

II.   In this case, use NOPS only when changing or rearranging instructions cannot avoid a hazard. You can assume register R7 can be used to hold temporary values in your modified code.

```
add  r1, r5, r3
sw   r1, 0(r2)
lw   r1, 4(r2)
add  r5, r5, r1
sw   r1, 0(r2)
```

Problem 2. (20 points) Calculate how many clock cycles will take execution of the following segment one RISC-V simple pipeline without forwarding when the outcome of branch instruction is available after EXE stage. Draw the pipelined diagram for this question.

```
lw   r1, 0(r4)
lw   r2, 400(r4)
addi r3, r1, r2
sw   r3, 0(r4)
sub  r4, r4, 4
beq  r4, r5, L1
```

Problem 3. (20 points) The individual stages of datapath have the following latencies:

IF	ID	EXE	MEM	WB
250ps	350ps	150ps	300ps	200ps

Also, assume that instructions executed by the processor are broken down as follows:

ALU	Branch	Load	Store
45%	20%	15%	20%

a) What is the clock cycle time in a pipelined and non-pipelined processor?

b) What is the total latency of **ld** instruction in a pipelined and non-pipelined processor?

c) Assuming there are no hazards or stalls, what is the utilization of data memory?

(Utilization is the fraction of clock cycles in which data memory is used).
d) Assuming there are no hazards or stalls, what is the utilization of register block's write port?

Problem 4. (20 points) Consider the following sequence of instructions being processed on the 5-stage RISC-V pipelined processor:

```
lw  r4, 100(r2)
add r5, r2, r3
sub r6, r4, r5
and r7, r2, r5
```

a) Identify all the data dependencies in the above instruction sequence. For each dependency, indicate the two instructions and the register that causes the dependency.

b) Assume that the pipelined uses full forwarding. Draw a pipelined diagram that represents the flow of instructions through the pipeline during each clock cycle. Indicate forwarding by arrows.

Problem 5 (20 points):

One particular branch (i.e., one specific PC) has the following actual outcomes. Show the predictions for both a one-bit counter and a two-bit counter (no history). For the two-bit counter, use **T** for strongly taken **t** for weakly taken, **n** for weakly not-taken, and **N** for strongly not taken. Finally fill in the accuracy (percentage of predictions that were correct) at the bottom of the table. The first prediction is done for you.

Branch Outcome	1-bit predictor		2-bit predictor	
	Prediction	Correct?	Prediction	Correct?
T	T	Yes	T	yes
T				
T				
N				
T				
N				
T				
T				
T				
N				
Accuracy				

Good luck