CECS 341: Computer Architecture and Organization

Homework 2 – RISC-V ISA

Due: Monday, Oct 5, 2020, by 11PM

Note: Submit you HW into Beachborad Dropbox folder. Each HW has its own Dropbox folder.

Using *Ripes* simulator, implement the following C code for RISC-V assembly. Assume that the values of a, b, i, j are in registers X5, X6, X7 and X29 respectively. Also, assume that register X10 holds the base address of the array A. (Note: A is an array of Bytes which means each element of array A holds one Byte of data).

```
for ( i = 0 ; i < a ; i++)

for ( j = 0 ; j < b ; j++)

A[i] = A[i] + 5*j + i;
```

```
.data
A: .byte 2,0,3,1
.text
li x5, 4
li x6, 2
la x10, A
```

put your code here

Submit your assembly source code (.as file) as well as a screenshot of part of memory that stores data for your code.

Note: For information regarding *Ripes* simulator, refer to the provided links in the BB (Chapter 2).

Good Luck