HCMUT

Course: Biomedical Electronics

Instructor: Hồ Trung Mỹ

Ch 3
Amplifiers & Signal Processing
(Các mạch khuếch đại và xử lý tín hiệu)

Refs:

1. Prof. Andrew Mason - Michigan State University, USA
2. J.G. Webster, “Medical Instrumentation Application and Design”, John Wiley & Sons, 2010

Outline

1. Ideal Op Amps
2. Inverting Amplifiers
3. Noninverting Amplifiers
4. Differential Amplifiers
5. Comparators
6. Rectifiers
7. Logarithmic Amplifiers
8. Integrators
9. Differentiators
10. Active Filters
11. Frequency Response
12. Offset Voltage
13. Bias Current
14. Input and Output Resistance
15. Phase-Sensitive Demodulators
16. Timers
17. Microcomputers in Medical Instrumentation

Khuếch đại và Xử lý tín hiệu

Cần khuếch đại và xử lý tín hiệu vì tín hiệu điện sinh học có:

- **Biên độ điện áp nhỏ (vài $\mu V, mV$)**
- **Dòng điện nhỏ (vài pA, nA)**
- **Dải tần số nhỏ (vài Hz đến vài trăm Hz)**

Applications of Operational Amplifier In Biological Signals and Systems

Các phép toán của Op-amp với các tín hiệu y sinh:

1)Khuếch đại và suy giảm
2)Lệch DC: cộng hoặc trừ DC
3)Lọc: tạo hình dạng nội dung tần số

3.1 Ideal Op-Amp

Most bioelectric signals are small and require amplifications

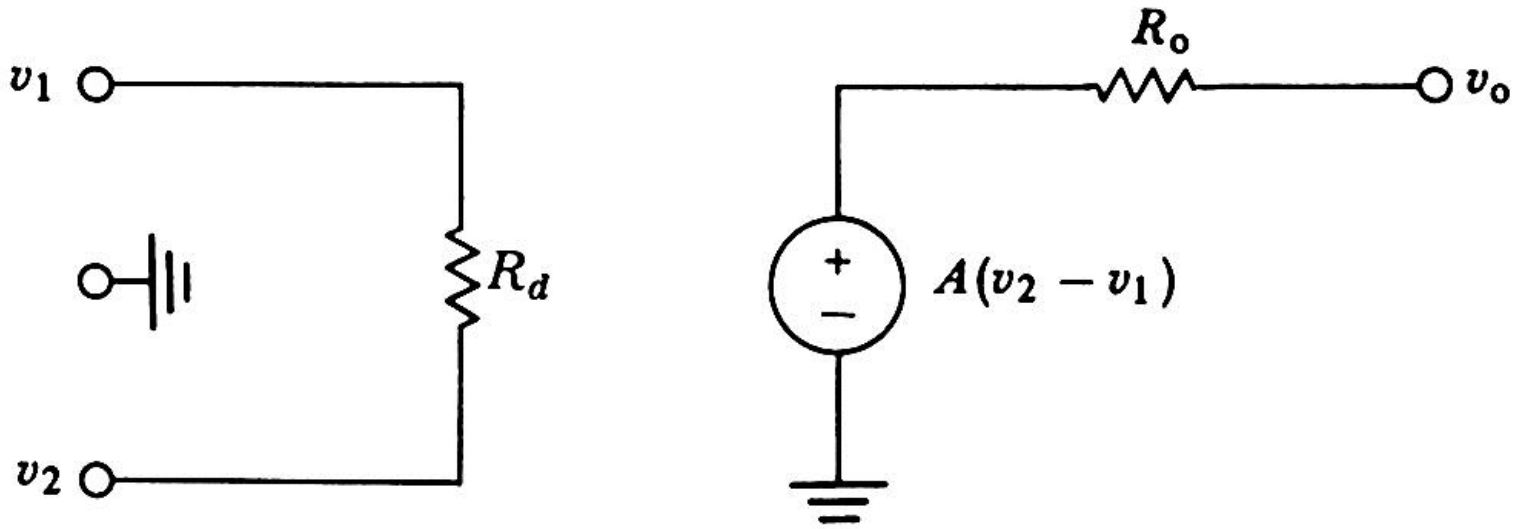
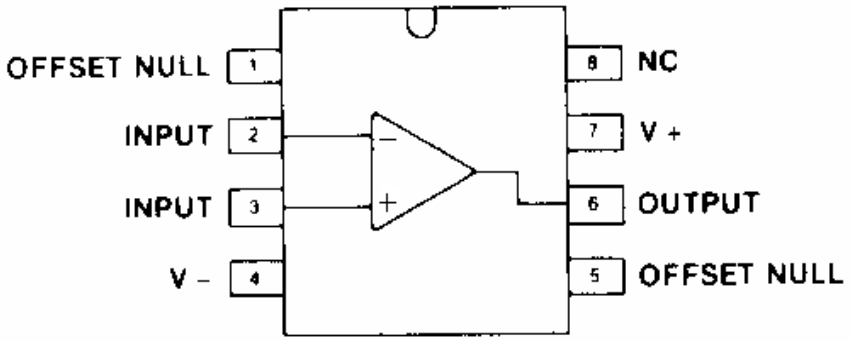
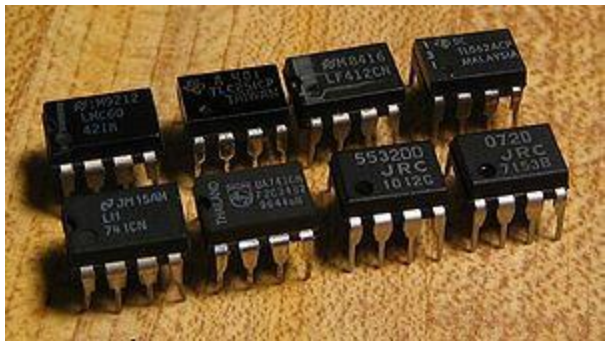


Figure 3.1 Op-amp equivalent circuit.
The two inputs are υ_1 and υ_2. A differential voltage between them causes current flow through the differential resistance R_d. The differential voltage is multiplied by A, the gain of the op amp, to generate the output-voltage source. Any current flowing to the output terminal v_o must pass through the output resistance R_o.

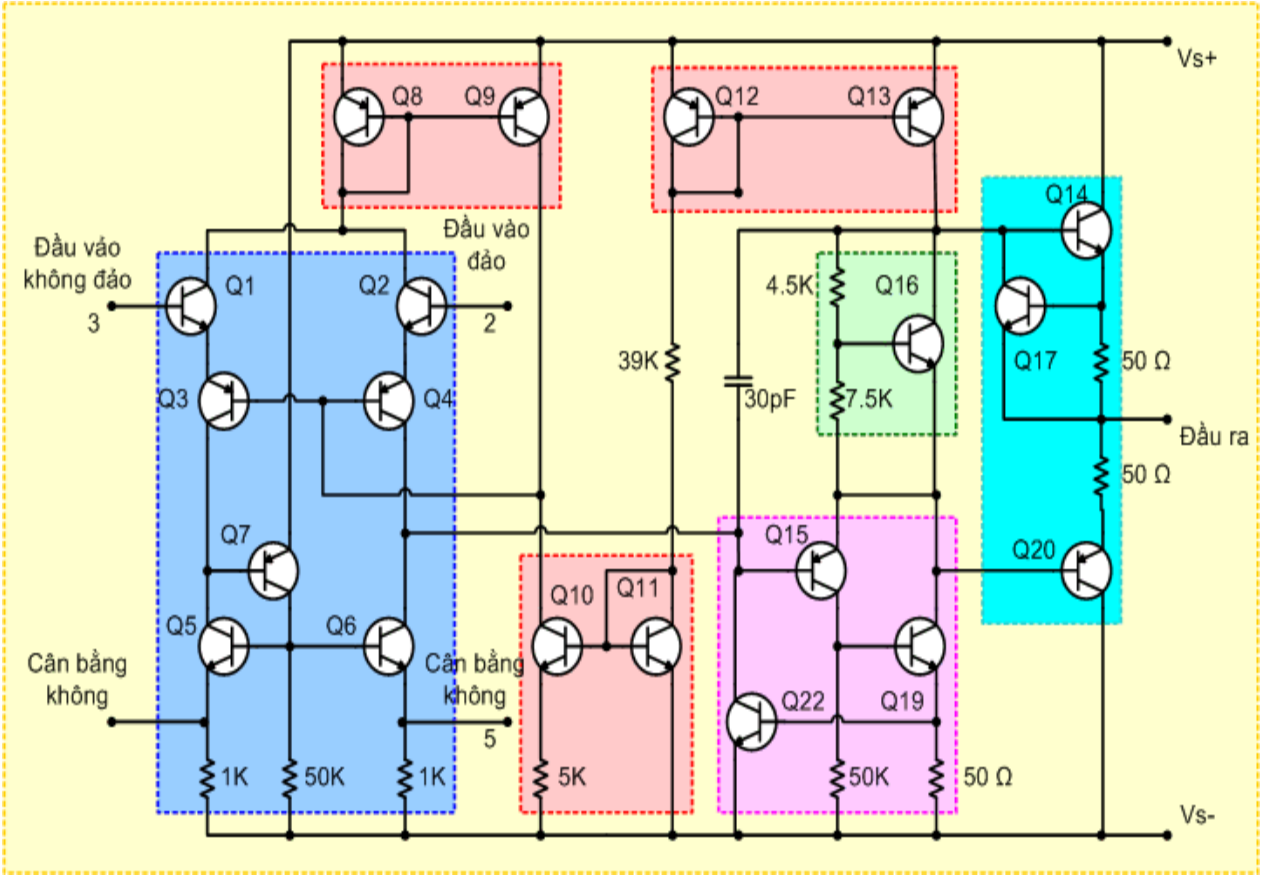
Inside the Op-Amp (IC-chip)



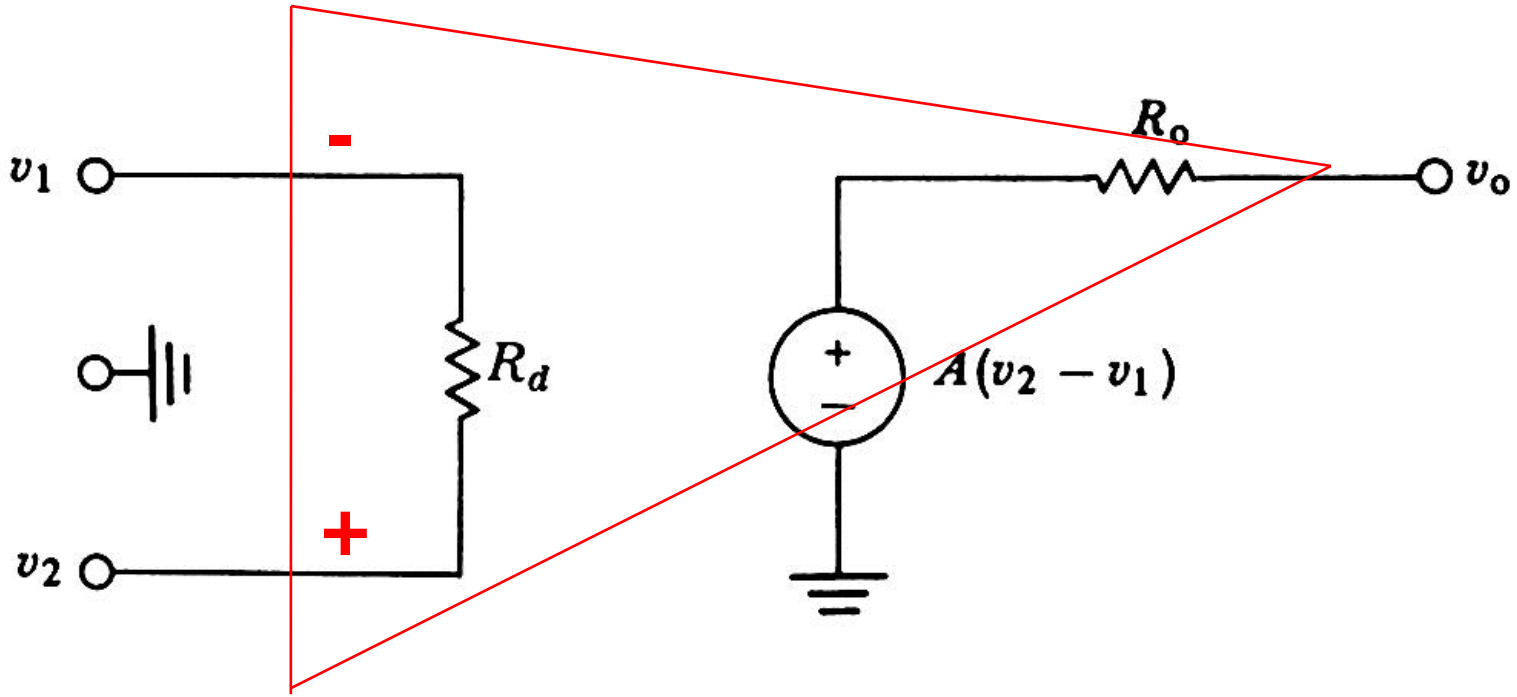
741 op amp



20 transistors
11 resistors
1 capacitor



Ideal Characteristics



1- $A = \infty$ (gain is infinity)

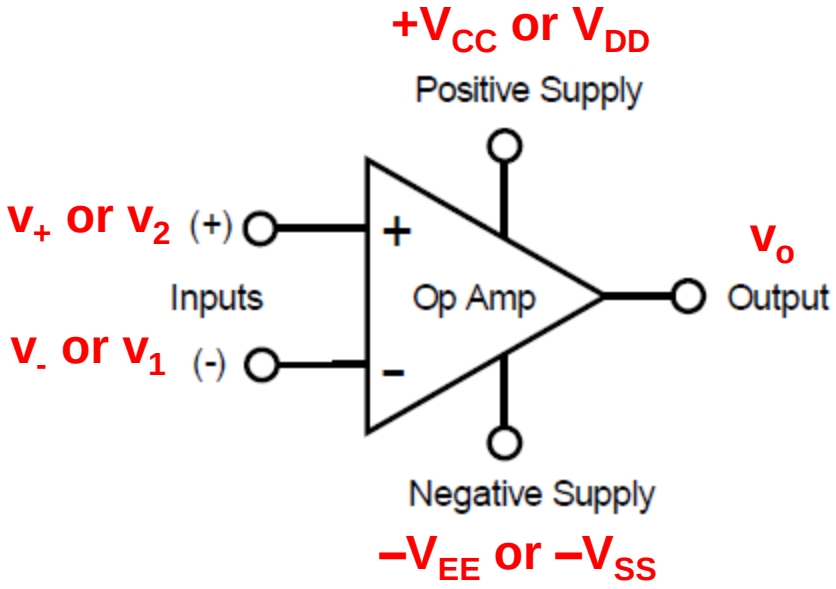
2- $V_o = 0$, when $v_1 = v_2$ (no offset voltage)

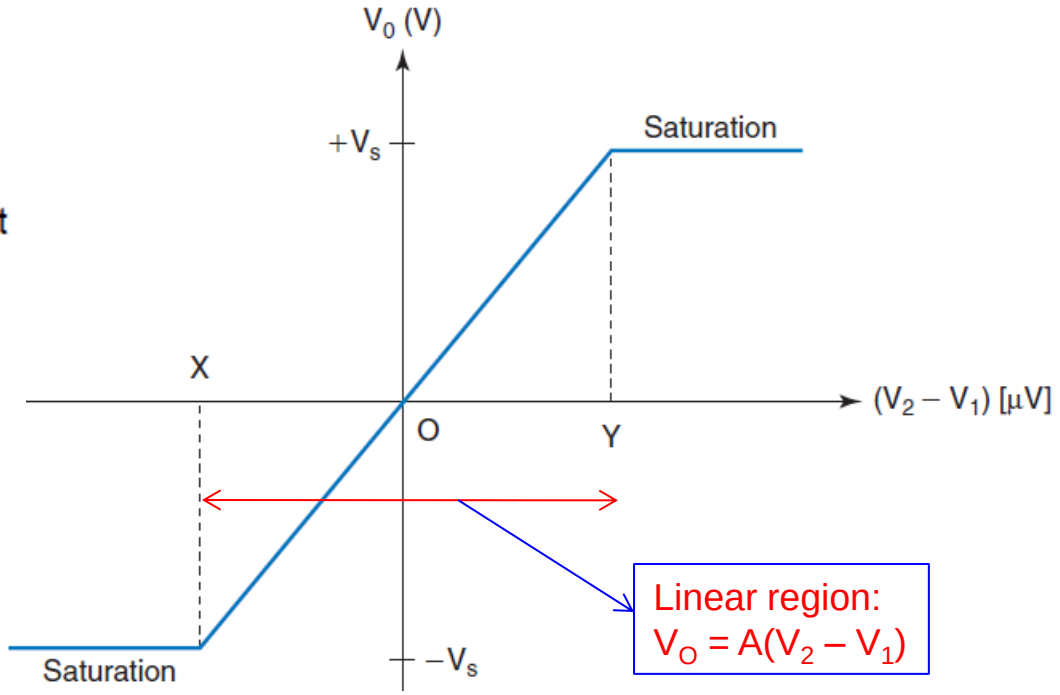
3- $R_d = \infty$ (input impedance is infinity)

4- $R_o = 0$ (output impedance is zero)

5- Bandwidth = ∞ (no frequency response limitations) and no phase shift

Đặc tuyến truyền đạt của opamp (Đường cong truyền đạt áp)





Chú ý:

- **Với opamp BJT: CC (Collector) và EE (Emitter)**
- **Với opamp FET: DD (Drain) và SS (Source)**
- **Cấp nguồn lưỡng cực:**
  Thường $V_{CC} = V_{EE}$
- **Cấp nguồn đơn (thường gặp trong ĐTYS):**
  - ❑ $V_{EE} = 0$ (thường gặp), hoặc
  - ❑ $V_{CC} = 0$

Typical values: X =-25 and Y = 25

Vsat+ = $+V_S$ ($Vs < V_{CC}$)

Vsat- = $-V_S$

Op-Amp Properties

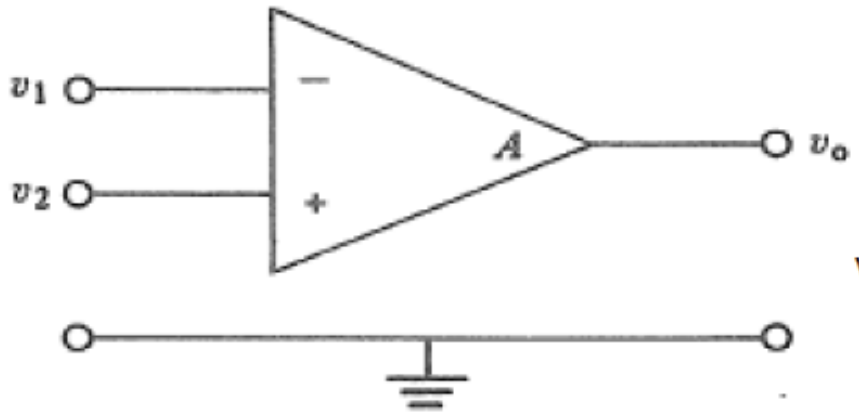
- Properties
  - open-loop gain: ideally infinite: practical values 20k-200k
    - high open-loop gain → virtual short between + and - inputs
  - input impedance: ideally infinite: CMOS opamps are close to ideal
  - output impedance: ideally zero: practical values 20-100Ω
  - zero output offset: ideally zero: practical value <1mV
  - gain-bandwidth product (GB): practical values ~MHz
    - frequency where open-loop gain drops to 1 V/V

- Commercial opamps provide many different properties
  - low noise
  - low input current
  - low power
  - high bandwidth
  - low/high supply voltage
  - special purpose: comparator, instrumentation amplifier

The ideal characteristics for an op amp and typical actual values for a 741 op amp

Characteristic	Ideal	Typical actual value (741)
open-loop voltage gain (A_0)	infinite	200 000 (106 dB)
input resistance	infinite	1 MΩ
output resistance	zero	75 Ω
bandwidth	infinite	up to 1 MHz
common mode rejection ratio (CMMR)	infinite	30 000 (90 dB)
slew rate	infinite	0.5 V/μS

Basic Op-Amp Principles



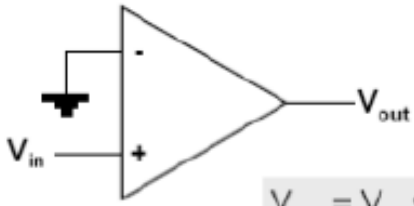
typical op-amp schematic symbol

v_o, v_1, v_2 referenced to ground

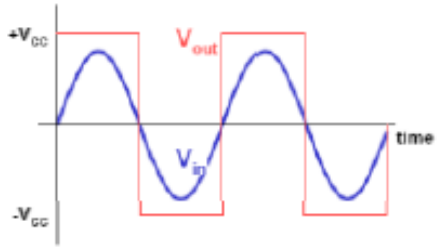
- Open loop gain: $v_o = A\,(v_2 - v_1)$
  - since A is very large, $v_1 - v_2$ must be very small
- When the op-amp output is in its linear range
  - two input terminals are at (essentially) the same voltage
  - i.e., "virtual ground" between op-amp inputs
    - rely on this for DC/bias calculations
- Single vs. Dual Supply Voltage
  - most modern ICs use single supply
    - "ground" in a dual supply becomes VDD/2 in single supply
      - mid way between VDD and Ground

Basic Opamp Configuration

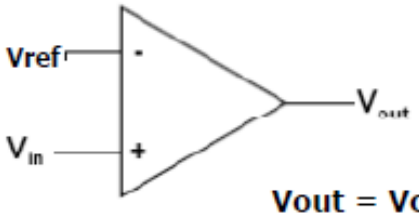
- Voltage Comparator
  - digitize input
  - assumes very high DC gain
  - Vcc = supply voltage



$V_{out} = V_{CC}\,\mathrm{sign}(V_{in})$

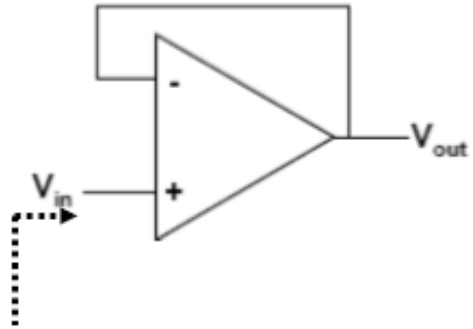


- Negative Feedback
  - output tied back into negative input terminal
  - generally avoid positive feedback



Vout = Vcc (sign(Vin-Vref))

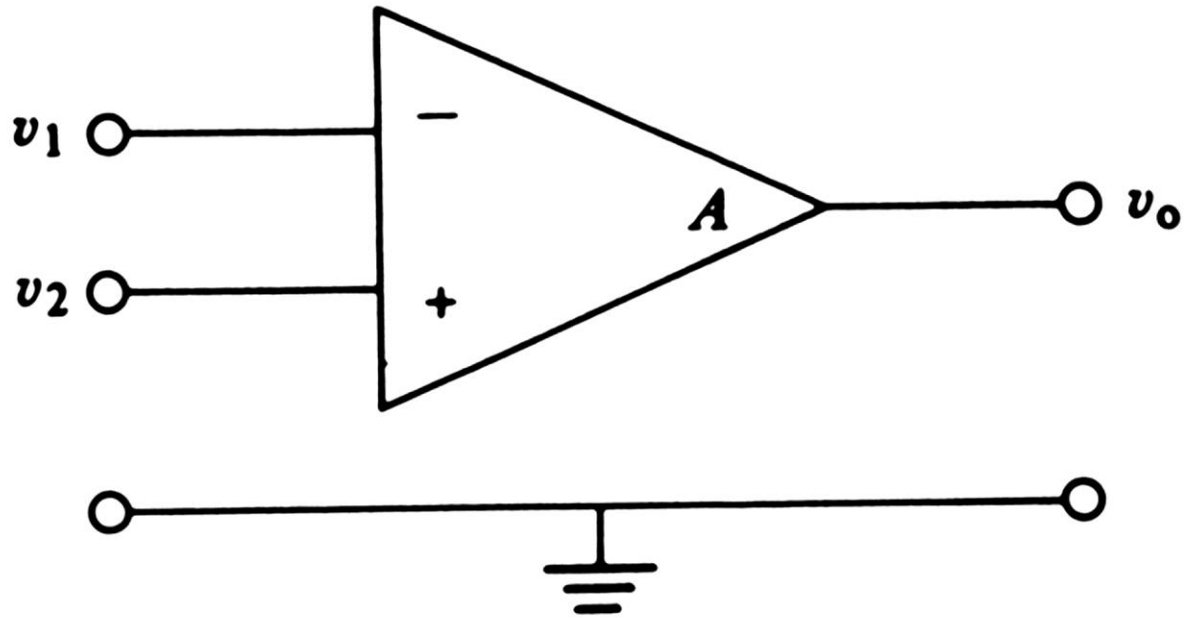
- Voltage Follower
  - buffer
  - prevents input signal from being loaded down by a low-resistance load



$V_{out} = V_{in}$

Rin = ∞

2 quy tắc cơ bản



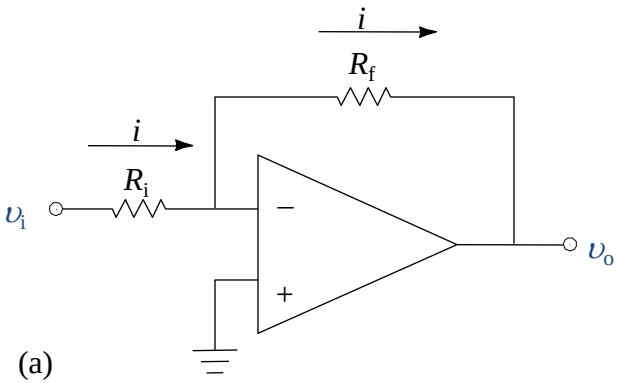
Quy tắc 1:

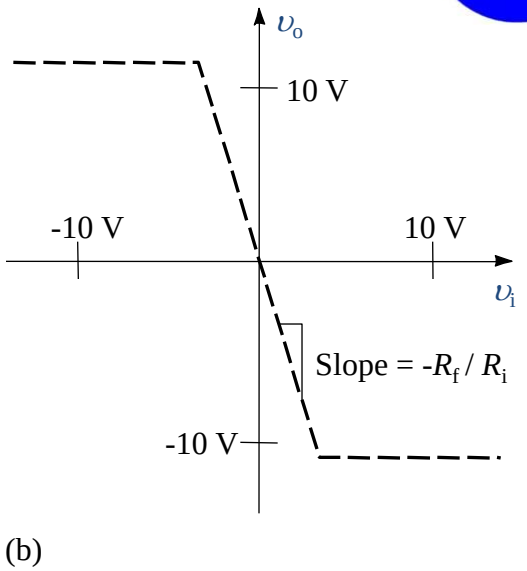
Ở miền tuyến tính (hay còn gọi là miền khuếch đại): $v_+ = v_-$

Quy tắc 2

Không có dòng vào/ra ở các ngõ vào của op-amp: $i_+ = i_- = 0$

3.2 Khuếch đại đảo

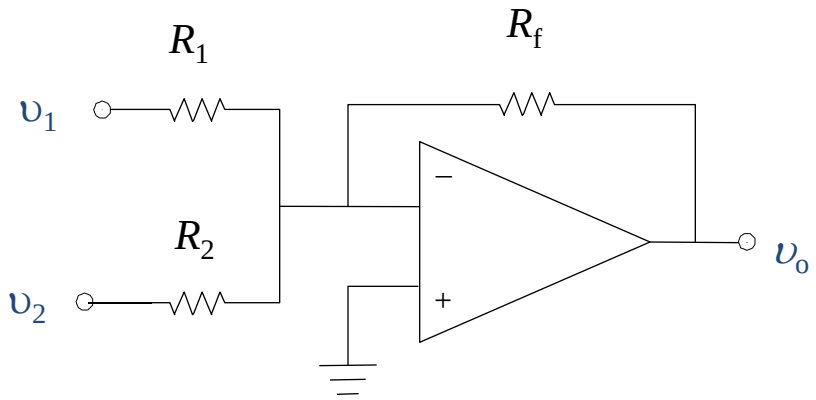




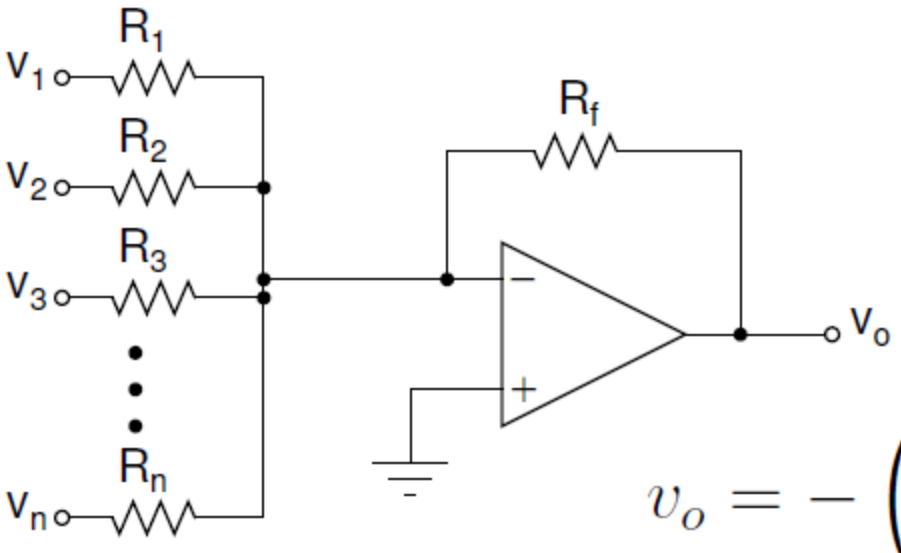
$$v_o = -\frac{R_f}{R_i} v_i \qquad G = \frac{v_o}{v_i} = -\frac{R_f}{R_i}$$

Figure 3.3 (a) An inverting amplified. Current flowing through the input resistor R_i also flows through the feedback resistor R_f. (b) The input-output plot shows a slope of $-R_f / R_i$ in the central portion, but the output saturates at about ± 13 V.

Mạch KĐ tổng đảo (Summing Amplifier)



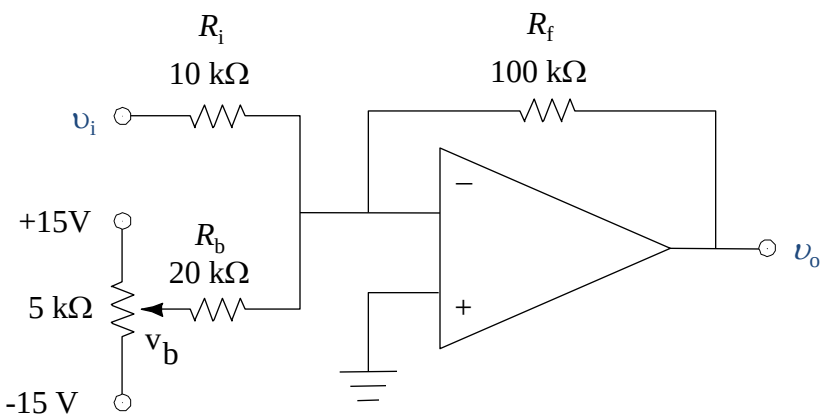
$$v_o = -R_f\left(\frac{v_1}{R_1} + \frac{v_2}{R_2}\right)$$



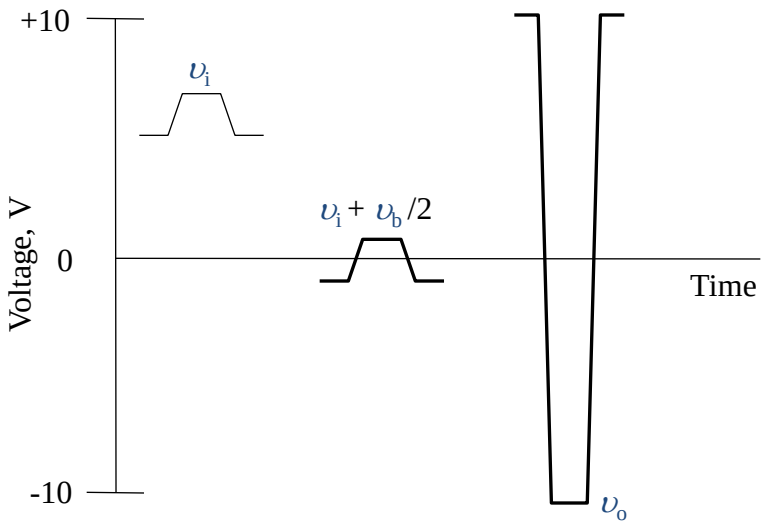
$$v_o = -\left(\frac{R_f}{R_1}v_1 + \frac{R_f}{R_2}v_2 + \ldots + \frac{R_f}{R_n}v_n\right)$$

Example 3.1

The output of a biopotential preamplifier that measures the electro-oculogram is an undesired dc voltage of ±5 V due to electrode half-cell potentials, with a desired signal of ±1 V superimposed. Design a circuit that will balance the dc voltage to zero and provide a gain of -10 for the desired signal without saturating the op amp.

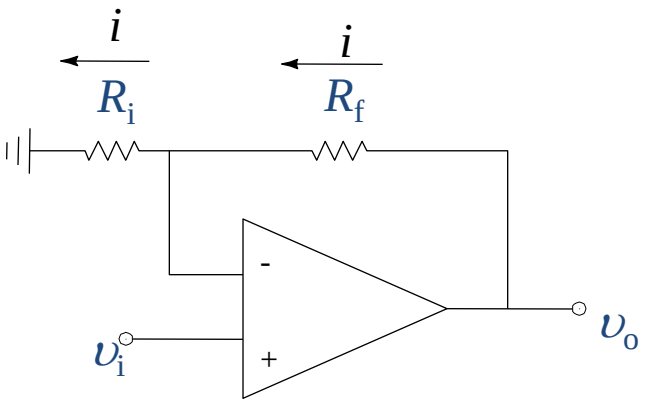


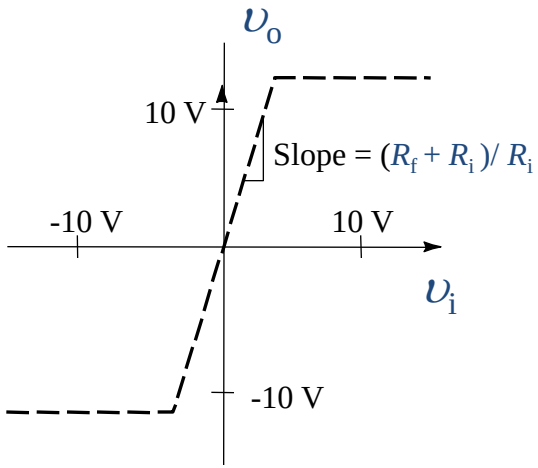
(a)



(b)

3.3 Mạch khuếch đại không đảo





$$v_o = \frac{R_f + R_i}{R_i} v_i$$

$$G = \frac{R_f + R_i}{R_i} = \left(1 + \frac{R_f}{R_i}\right)$$

Fundamental Circuit: Source and Load

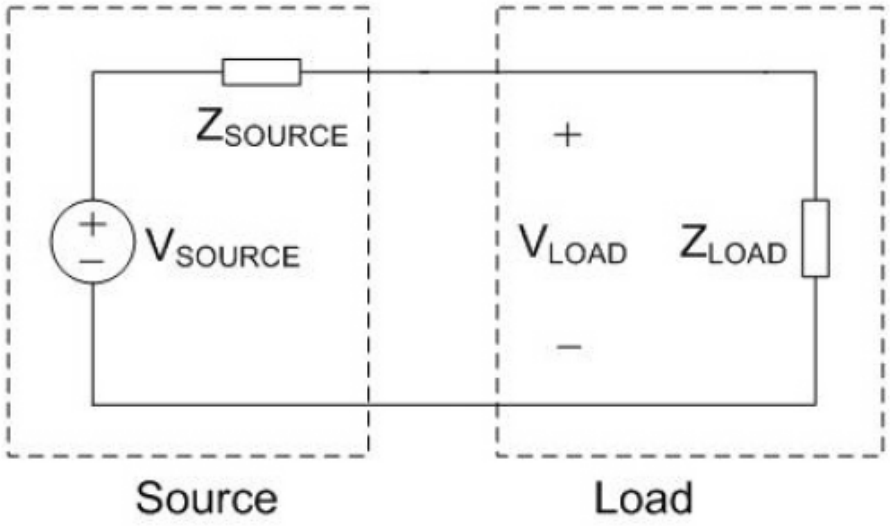
Sources

Power supply

Signal Generator

Sensor

Amplifier output



Loads

Actuator

Measurement device

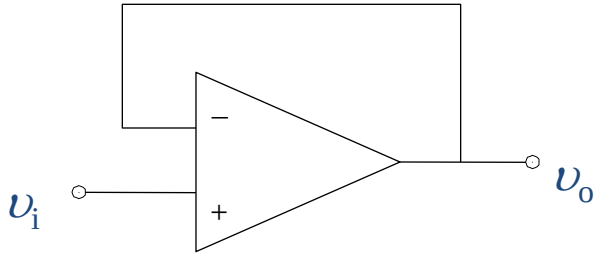
Amplifier input

- Optimize for Voltage: $Z_{LOAD} >> Z_{SOURCE}$
- Optimize for Current: $Z_{LOAD} << Z_{SOURCE}$
- Optimize for Power: $Z_{LOAD} = Z_{SOURCE}$

- Amplifier / active circuit – impedance transform

Follower (buffer)

Used as a buffer, to prevent a high source resistance from being loaded down by a low-resistance load. In another word it prevents drawing current from the source.

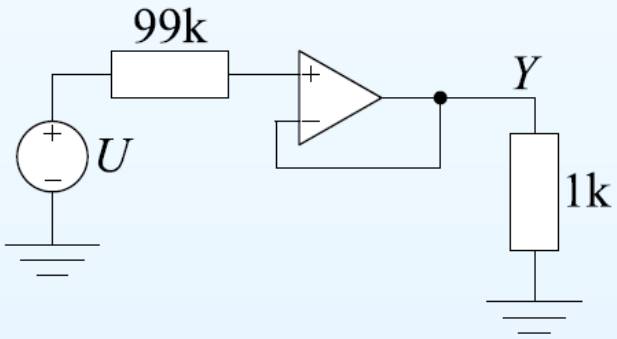


$$v_o = v_i \qquad G = 1$$

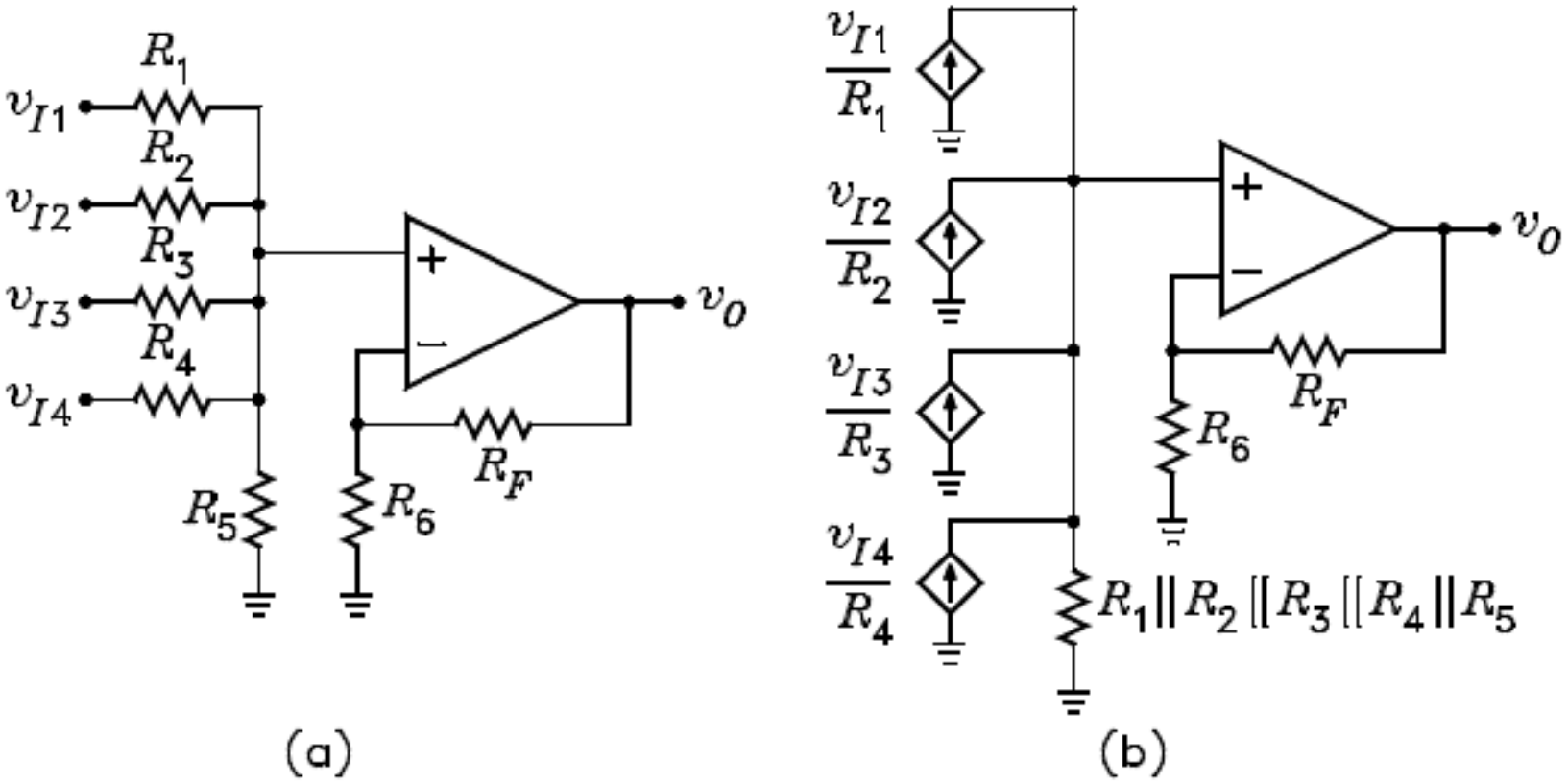
Advantage: Can supply a large current at Y while drawing almost no current from X. Useful if the source supplying X has a high resistance.

Without voltage follower: $Y = 0.01U$.

With voltage follower: $Y = U$.



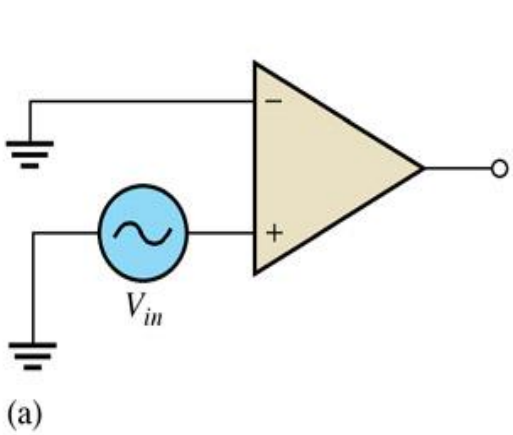
Mạch KĐ tổng không đảo



(a) Four input non-inverting summer. (b) Equivalent circuit for calculating v_o.

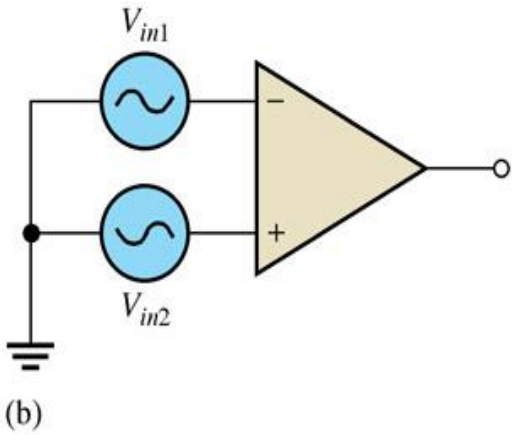
$$
\begin{aligned}
v_O &= v_+ \left(1 + \frac{R_F}{R_6}\right) \\
&= \left(\frac{v_{I1}}{R_1} + \frac{v_{I2}}{R_2} + \frac{v_{I3}}{R_3} + \frac{v_{I4}}{R_4}\right) (R_1 \| R_2 \| R_3 \| R_4 \| R_5) \left(1 + \frac{R_F}{R_6}\right)
\end{aligned}
$$

Input modes for op-amp



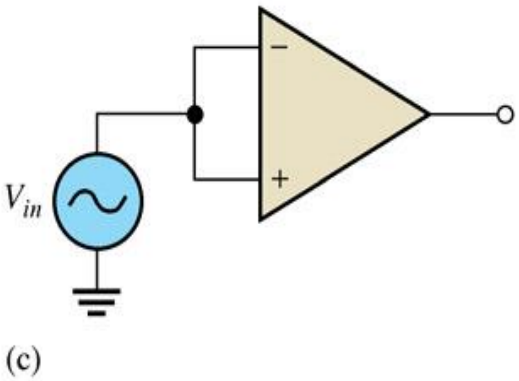
(a) Single-ended input

(Ngõ vào đơn cực)



b) Differential input

(Ngõ vào vi sai)



(c) Common-mode

(Ngõ vào cách chung)

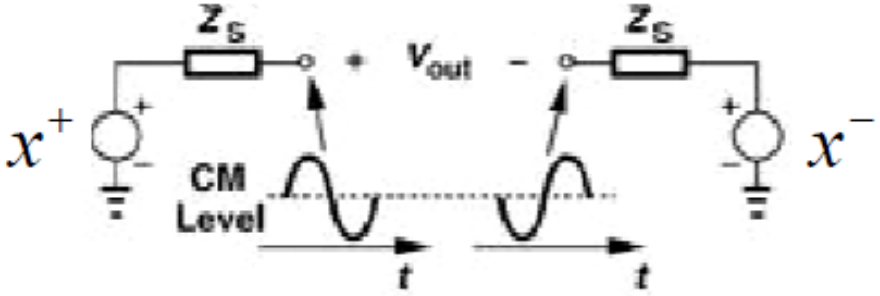
Ref: **Floyd**

Differential vs. Common Mode Signal

- Define
  - x^+ = input at + terminal
  - x^- = input at – terminal
  - c = common mode signal on both inputs
- Differential inputs

$$V_{out} = x^+ - x^-$$

- Add common mode input
  - *c* rejected by differential amplifier (not amplified)
  - *c* must be small enough to keep op-amp biased in linear operation

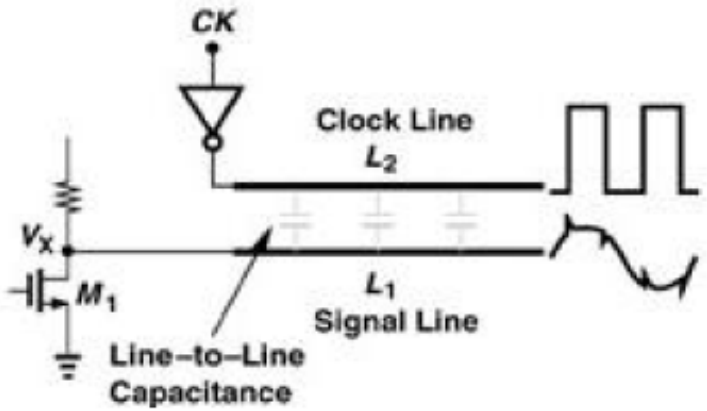


$$V_{out} = (x^+ + c) - (x^- + c)$$

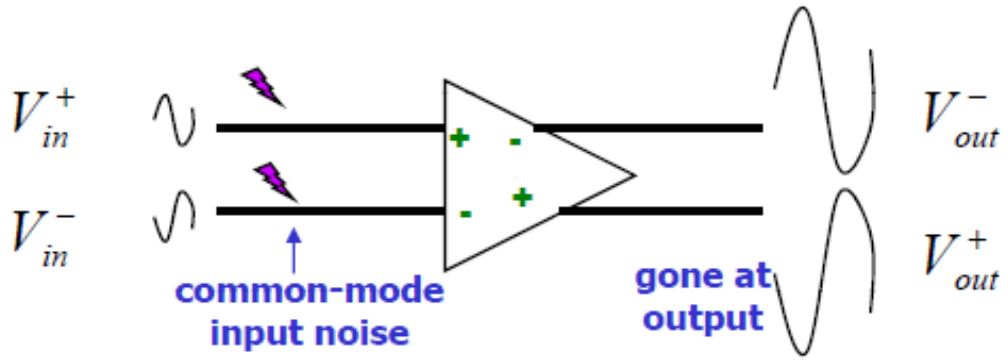
$$c = \frac{x^+ + x^-}{2}$$

Noise in Differential Amplifiers

- Global interference (e.g., supply voltage variations)
  - assumed to be located far away from amp. input terminals
    - same interference on both the terminals
  - appear as common mode disturbance.
  - example: clock noise

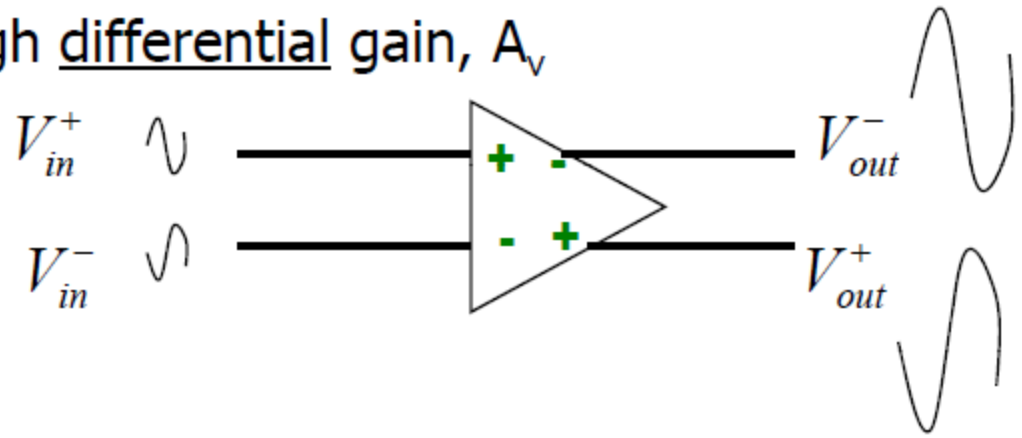


- Differential amplifiers
  - amplify only the difference
  - reject the interference (common-mode)



Desirable Properties of Amplifiers

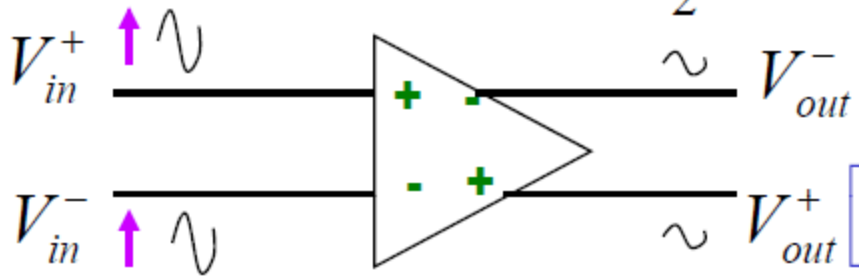
- High <u>differential</u> gain, A_v



$$A_v = \frac{\Delta V_{out}^{+} - \Delta V_{out}^{-}}{\Delta V_{in}^{+} - \Delta V_{in}^{-}}$$

- Low common mode gain, A_{cm}
  = high "common mode rejection"

Common-mode signal $\dfrac{\Delta V_{in}^{+} + \Delta V_{in}^{-}}{2}$

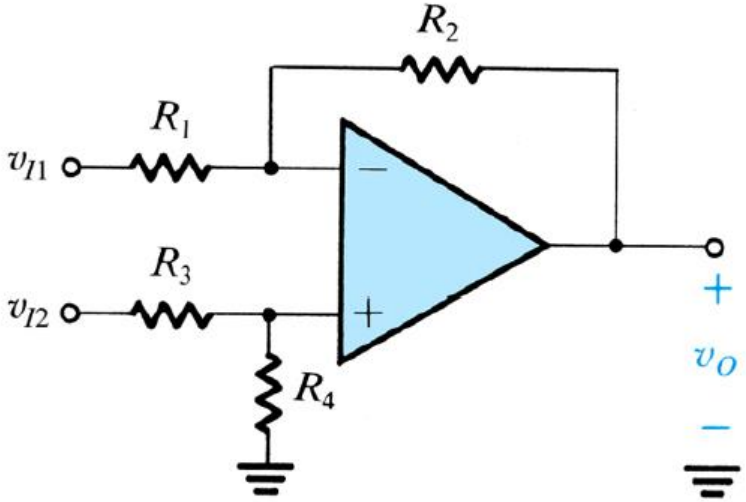


$$A_{CM} = \frac{\Delta V_{out}^{+} - \Delta V_{out}^{-}}{\frac{\Delta V_{in}^{+} + \Delta V_{in}^{-}}{2}}$$

common mode rejection ratio: $\mathrm{CMRR} = \dfrac{A_v}{A_{cm}}$

3.4 Mạch KĐ vi sai (Differential Amplifiers)

Mạch KĐ hiệu (Difference Amplifier)



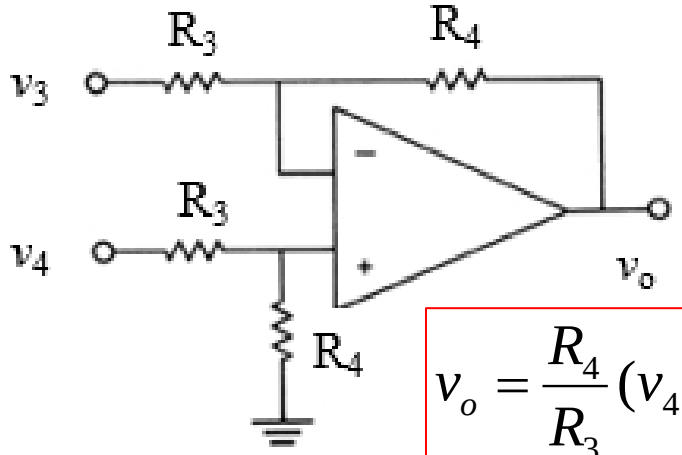
Áp dụng nguyên tắc xếp chồng (supersition principle) ta có:

$V_O = (1 + R_2/R_1)R_4V_{I2}/(R_4+R_3) - R_2/R_1V_{I1}$

Nếu R4/R3 = R2/R1 thì ta có mạch KĐVS

$$V_O = (R2/R1)(V_{I2} - V_{I1})$$
$$= (R4/R3)(V_{I2} - V_{I1})$$

Mạch KĐ vi sai



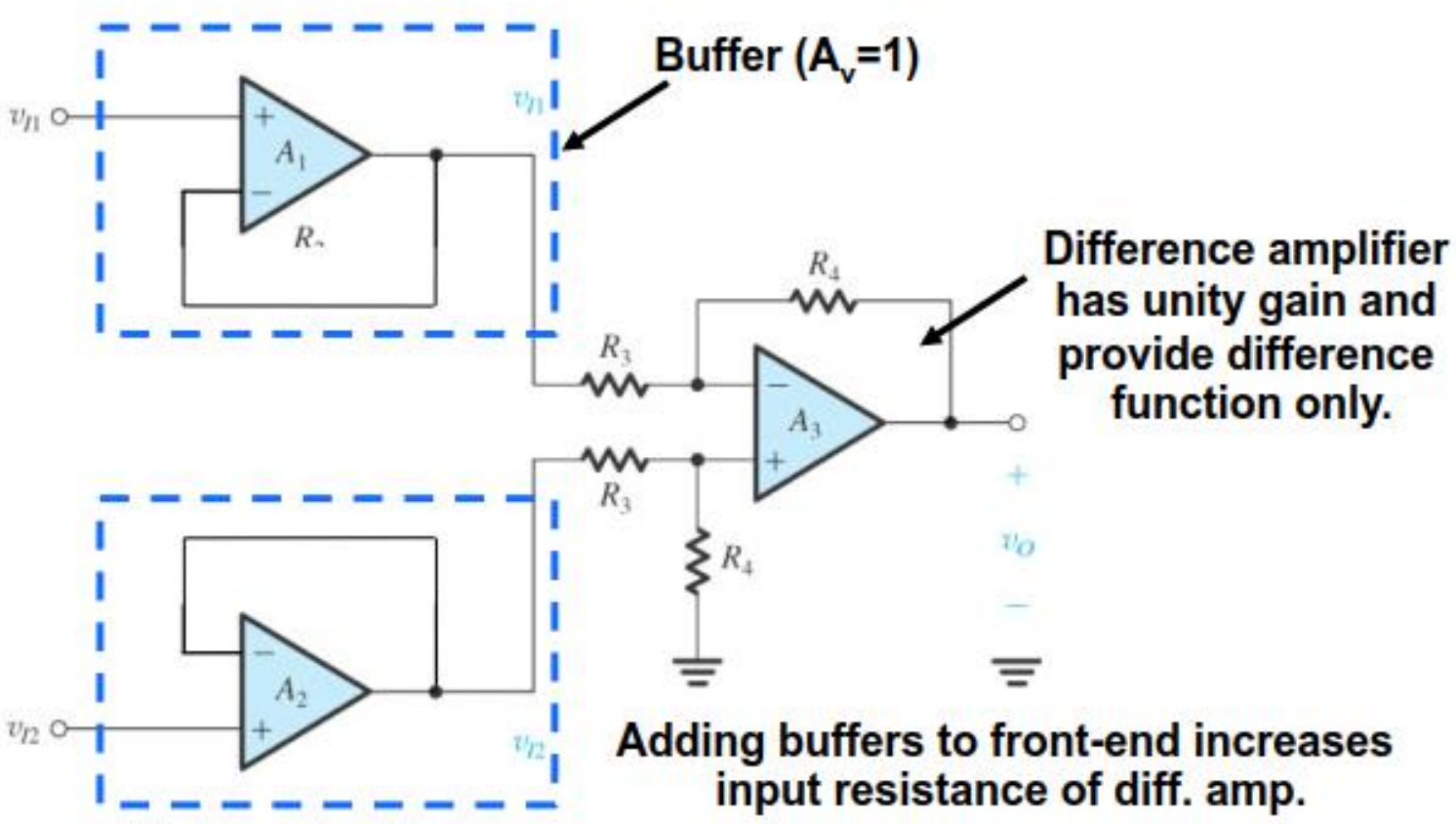
$$v_o = \frac{R_4}{R_3}(v_4 - v_3)$$

- ***Độ lợi VS*: $G_d = V_o/(V_4 - V_3) = R_4/R_3$**
- ***Độ lợi cách chung Gc*:** lý tưởng thì **$Gc = 0$**, nhưng thực tế thường $Gc \neq 0$.
- Tỉ số triệt cách chung CMRR (Common Mode Rejection Ration):

  $CMRR = |Gd/Gc|$ hoặc

  $CMRR_{dB} = 20\ log_{10}\ |Gd/Gc|$
- Bất lợi của mạch này là tổng trở vào nhỏ: $R_{in} = 2R_3$

Mạch KĐ vi sai có thêm mạch đệm

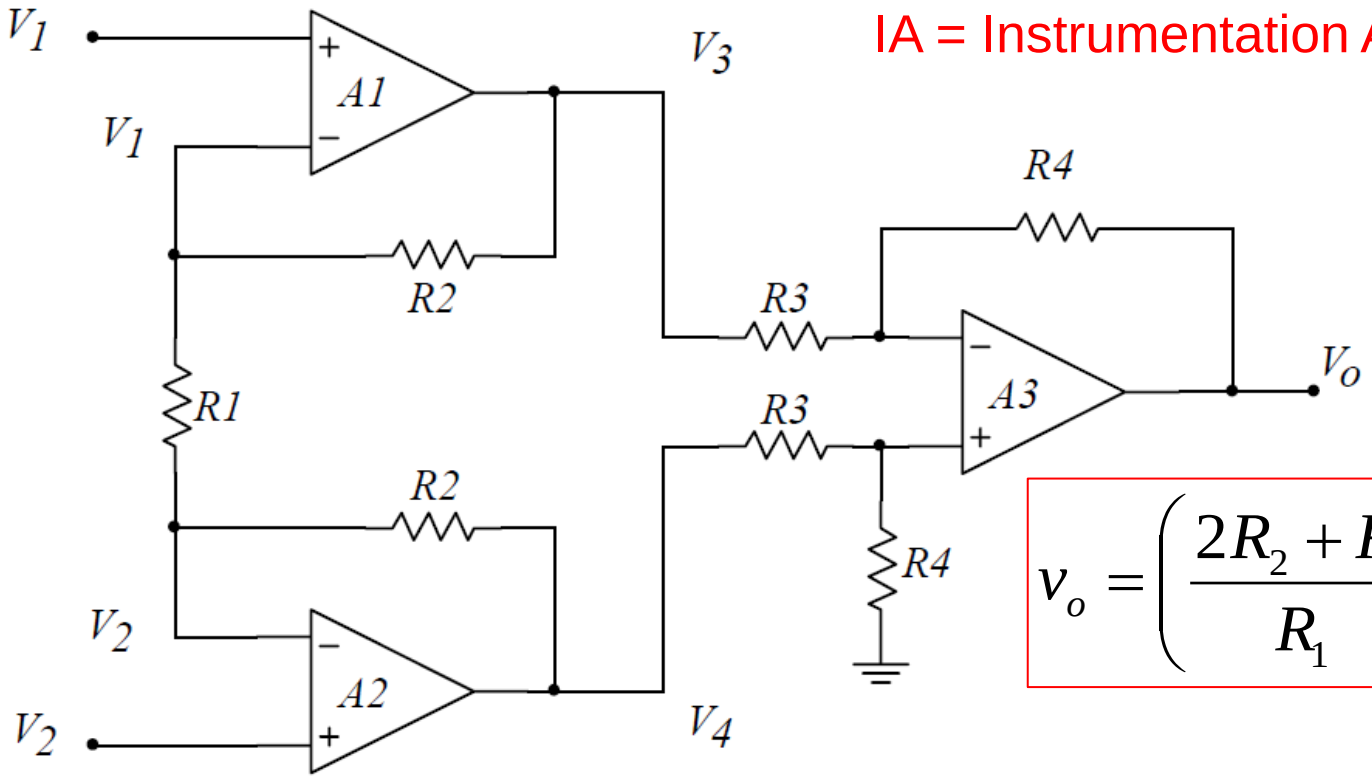


Ưu điểm: Mạch này có tổng trở vào: $R_{in} = \infty$

Khuyết điểm: khó chỉnh độ lợi

Mạch KĐ đo lường (IA) dùng 3 opamp

IA = Instrumentation Amplifier



$$v_o = \left(\frac{2R_2 + R_1}{R_1}\right)\frac{R_4}{R_3}(v_2 - v_1)$$

Differential Mode Gain:

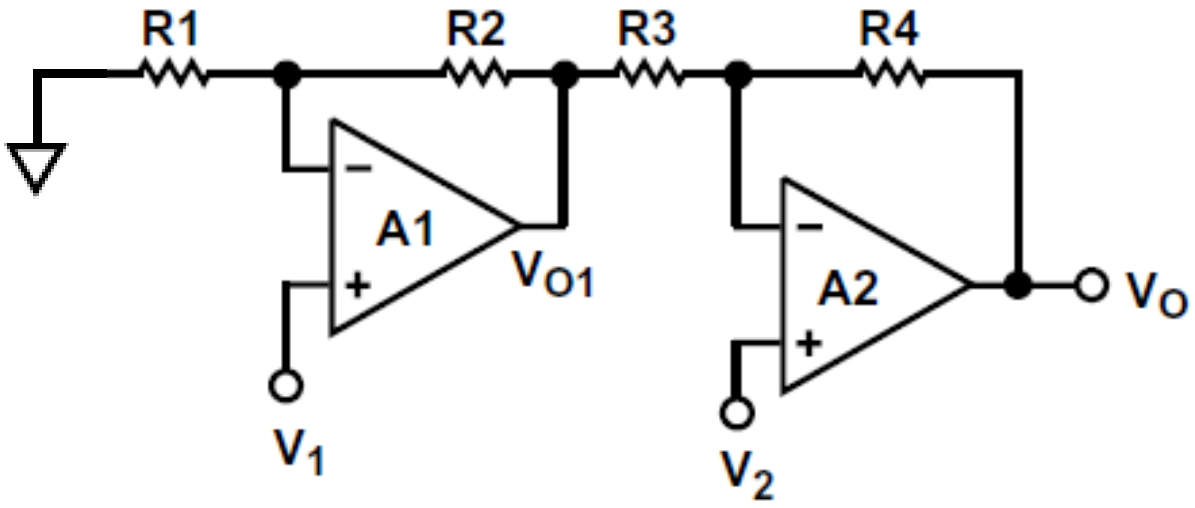
$$v_3 - v_4 = i(R_2 + R_1 + R_2)$$

$$v_1 - v_2 = iR_1$$

$$G_d = \frac{v_3 - v_4}{v_1 - v_2} = \frac{2R_2 + R_1}{R_1}$$

Advantages: High input impedance, High CMRR, Variable gain

Mạch KĐ đo lường (IA) dùng 2 opamp



- Điện áp ra Vo = G1V1 + G2V2
  với

  $G1 = -(1 + R2/R1)R4/R3$ và $G2 = 1 + R4/R3$

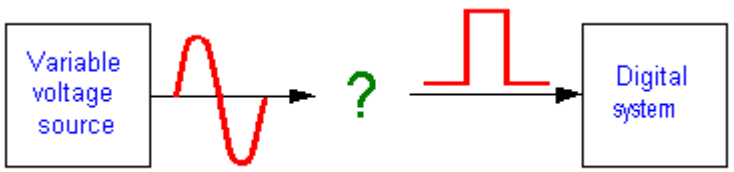
- Nếu R1/R2 = R4/R3 thì ta có mạch KĐVS:

$$V_o = (1 + R_4/R_3)(V_2 - V_1)$$

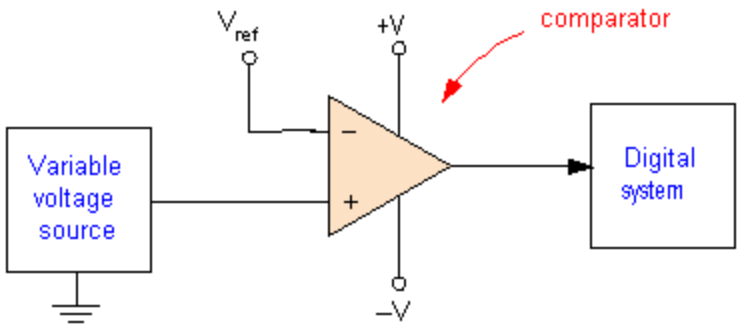
3.5 Mạch so sánh (Comparator)

- Mạch so sánh là mạch op-amp so sánh hai điện áp đầu vào và tạo ra đầu ra chỉ ra mối quan hệ giữa chúng. Các đầu vào có thể là hai tín hiệu (như hai sóng hình sin) hoặc tín hiệu và điện áp tham chiếu dc cố định V_{REF} (còn được gọi là điện áp chuẩn)
- Thường được sử dụng như một giao tiếp giữa tín hiệu số và tín hiệu tương tự.

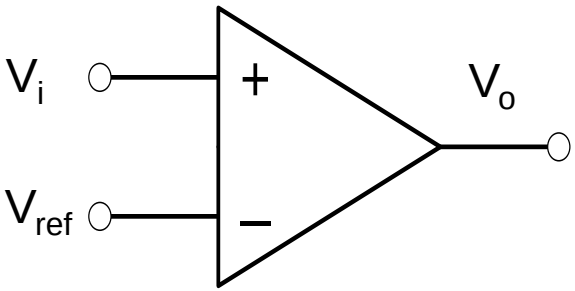
Vấn đề



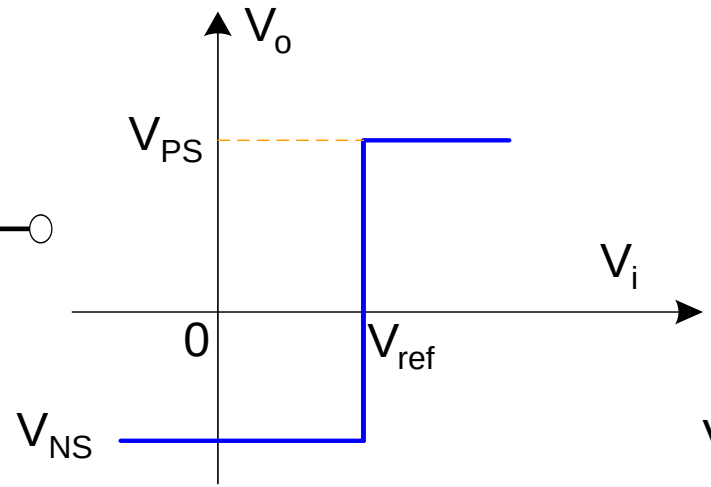
Giải pháp



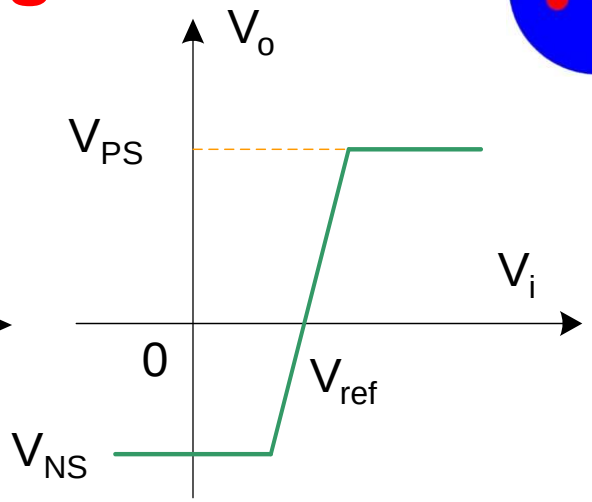
Mạch so sánh đơn giản



$V_o = V_{SAT}\,\text{sign}(V_i - V_{ref})$



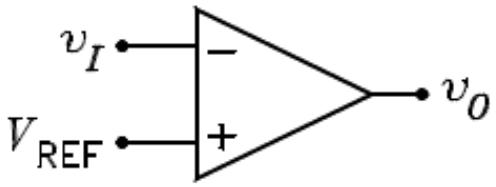
Đặc tuyến truyền đạt lý tưởng

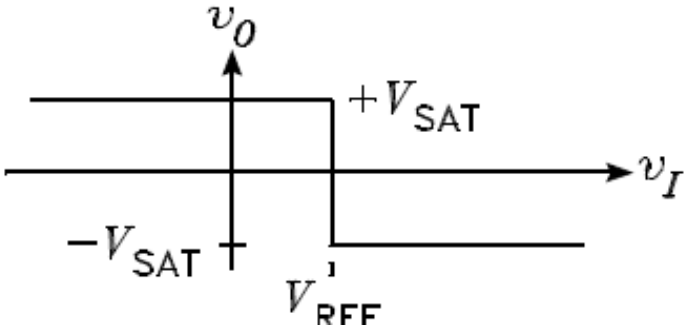


Đặc tuyến truyền đạt thực tế

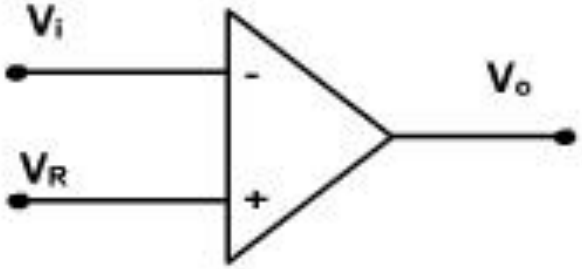
Chú ý:

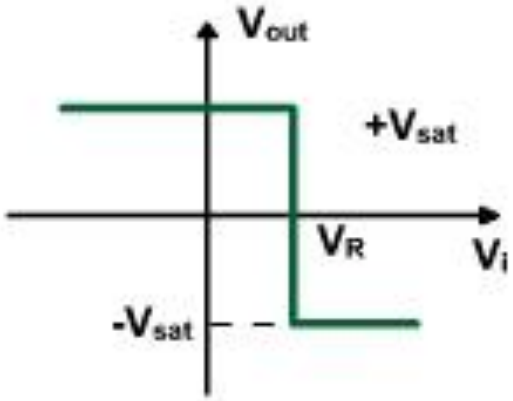
- ***Điện áp bão hòa dương*** V_{PS} = Vsat+ = $+V_{SAT}$
- ***Điện áp bão hòa âm*** V_{NS} = Vsat– = $–V_{SAT}$
- Nếu cấp nguồn lưỡng cực và đối xứng thì (lý tưởng) $V_{SAT} = V_{CC} = V_{EE}$.
- Nếu hoán đổi các đầu vào thì $V_o = –V_{SAT}\,\text{sign}(V_i – V_{ref})$ và đặc tuyến truyền đạt sẽ đảo ngược.
- Đây là ***mạch phát hiện mức zero***.

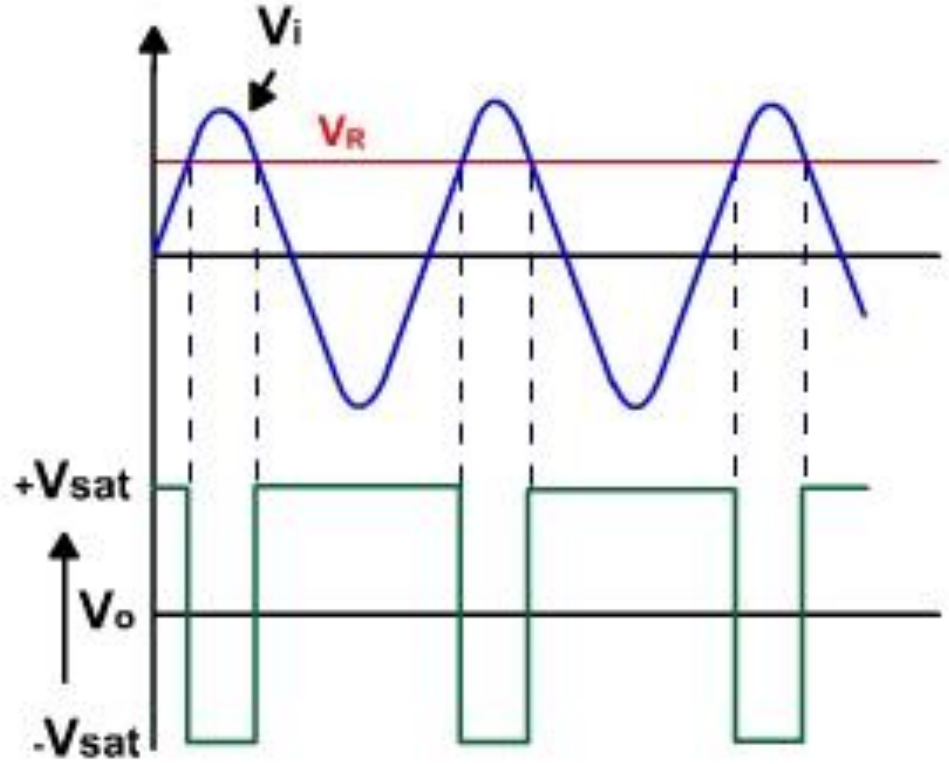




3.5 Mạch so sánh (Comparator)

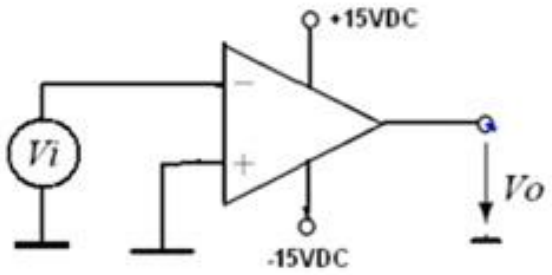


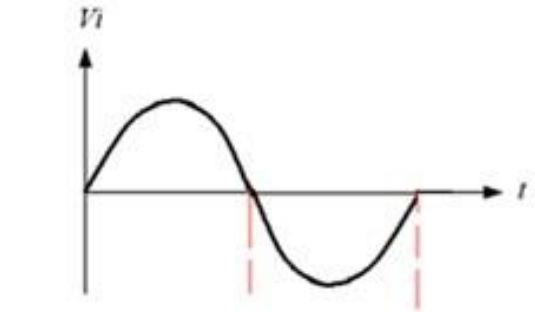


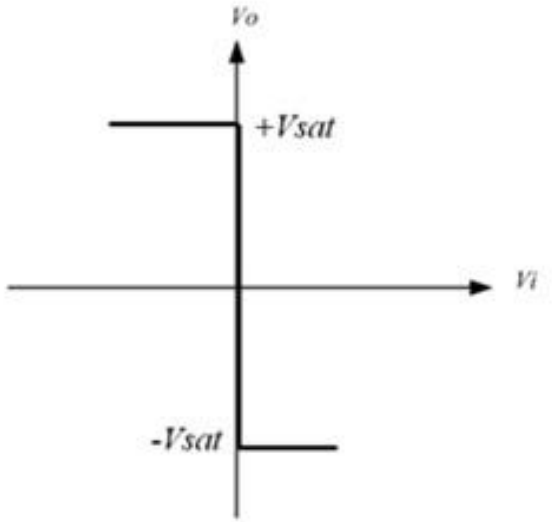


Mạch so sánh với tham chiếu zero

Mạch phát hiện mức zero

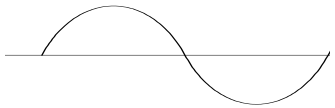


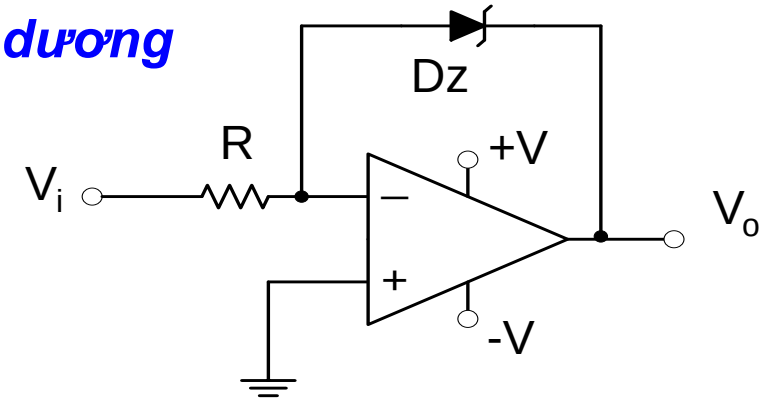


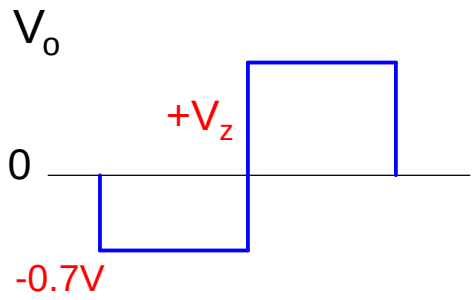


Mạch so sánh với tham chiếu zero có giới hạn

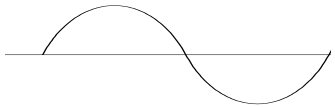
1. Giới hạn ở trị dương

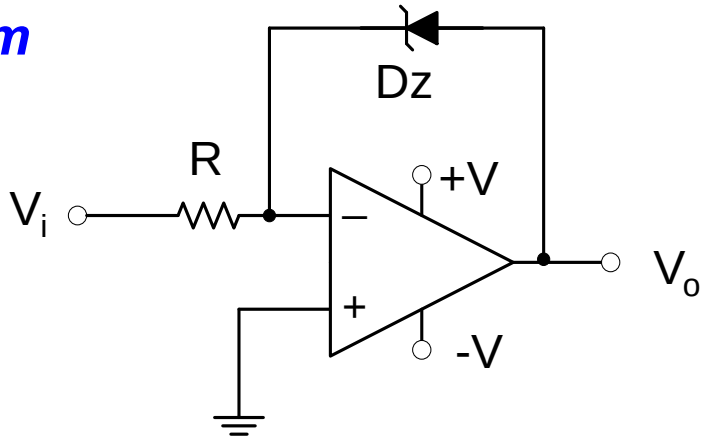


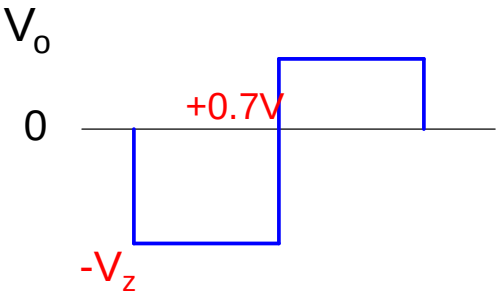




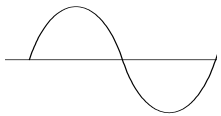
2. Giới hạn ở trị âm

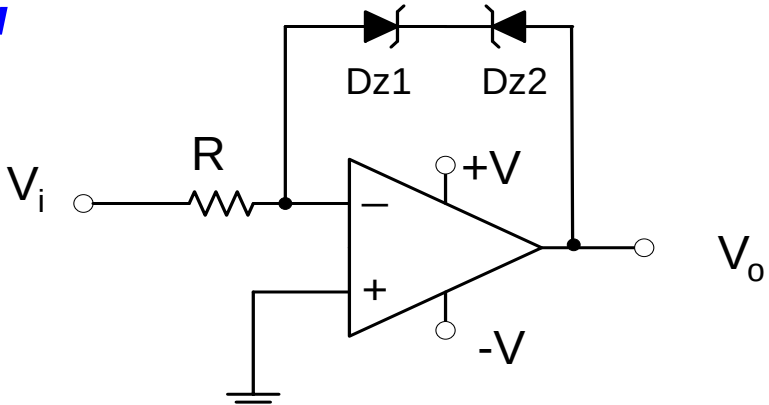


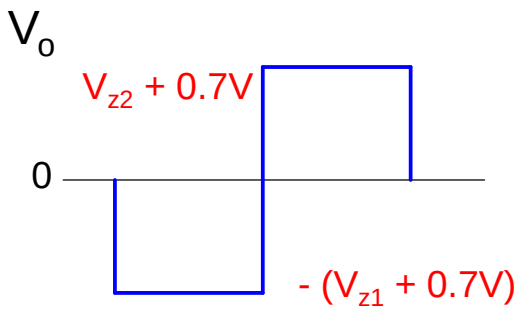




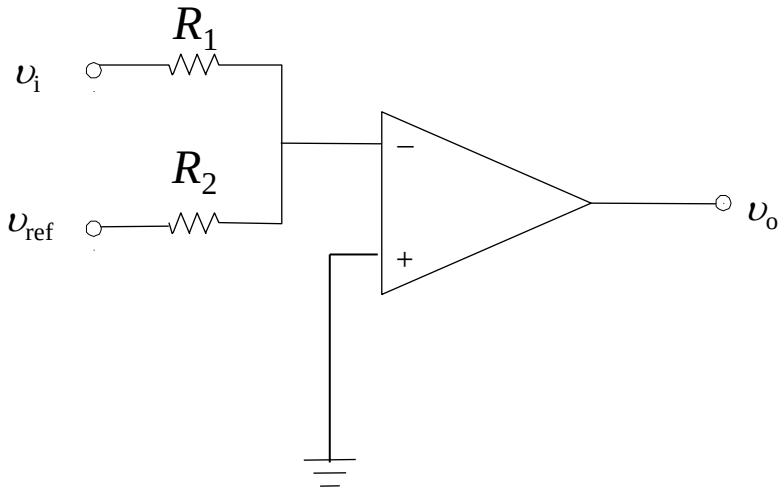
3. Giới hạn 2 đầu



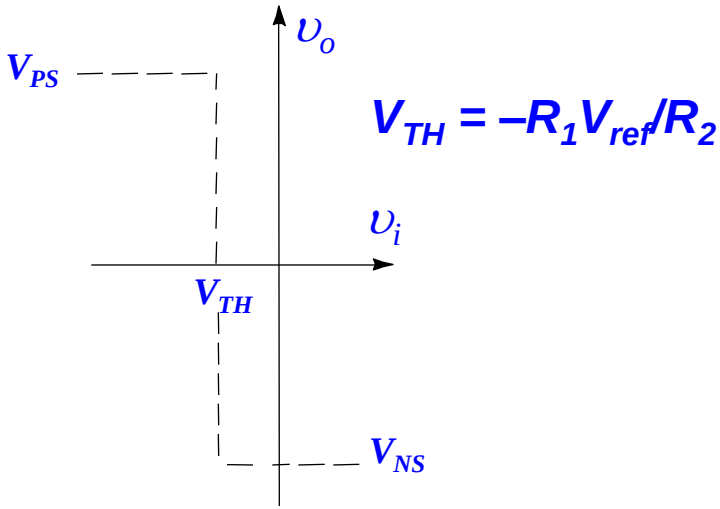




Mạch so sánh với mức ngưỡng V_{TH}



Mạch so sánh có ngưỡng



Đặc tuyến truyền đạt

- Điện thế tại ngõ đảo là (tổng quát thì V_{ref} có thể dương, âm hay 0)

$$V- = (R_2Vi + R_1V_{ref})/(R_1 + R_2)$$

- Ta xét dấu $V+ – V- = –(R_2Vi + R_1V_{ref})/(R_1 + R2)$

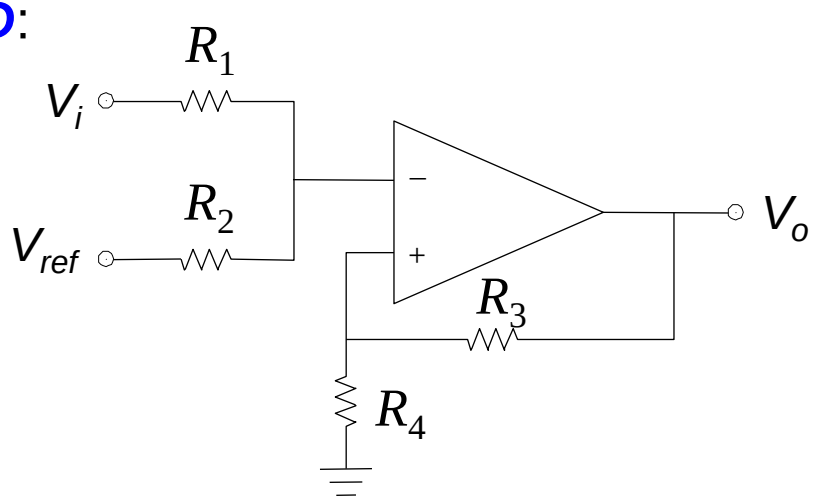
Vi	**< V_{TH}**	**V_{TH}**	**> V_{TH}**
$V_+ – V_-$	+	0	–
Opamp bão hòa	+		–
Ngõ ra Vo	$V_{PS} = +V_{SAT}$		$V_{NS} = –V_{SAT}$

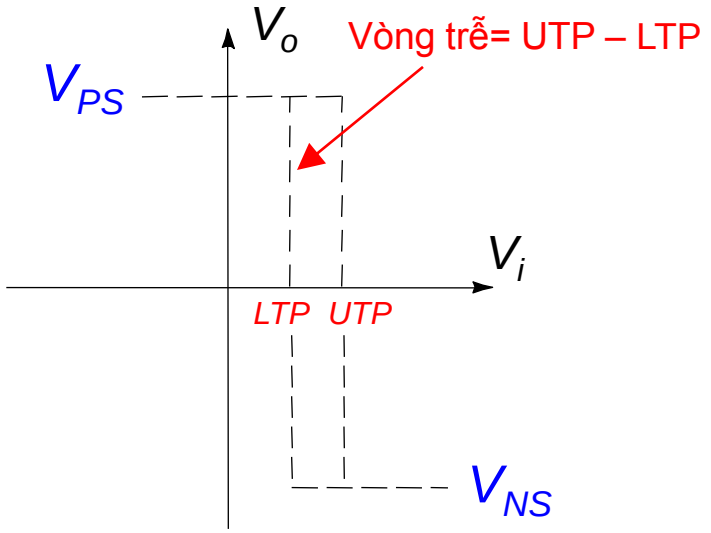
với điện áp ngưỡng (threshold voltage) $V_{TH} = –R_1V_{ref}/R_2$

Mạch so sánh có vòng trễ (hysteresis)

- Còn được gọi là mạch ***Schmitt trigger*** (có nhiều dạng mạch)
- Có hồi tiếp dương và đặc tuyến truyền đạt có vòng trễ.

❖ ***TD***:





- Xét dấu của V+ – V- với
- $V- = (R_2Vi + R_1Vref)/(R_1 + R_2)$
- $V+ = R_4V_o/(R_3 + R_4)$

$$UTP = -R_1V_{ref}/R_2 + (1 + R_1/R_2)R_4V_{SAT}/(R_3 + R_4)$$
$$LTP = -R_1V_{ref}/R_2 - (1 + R_1/R_2)R_4V_{SAT}/(R_3 + R_4)$$
$$UTP - LTP = 2(1 + R_1/R_2)R_4V_{SAT}/(R_3 + R_4)$$

- Khi V_i tăng trị từ trái qua phải, opamp bão hòa dương, $V_o = V_{PS}$; tại điểm UTP thì chuyển sang bão hòa âm.

$$UTP = -R_1V_{ref}/R_2 + (1 + R_1/R_2)R_4V_{SAT}/(R_3 + R_4)$$

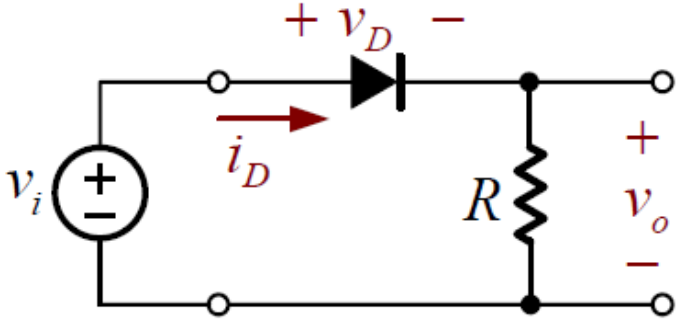
- Ngược lại, khi V_i giảm trị từ phải (từ điểm > UTP) ta có

$$LTP = -R_1V_{ref}/R_2 - (1 + R_1/R_2)R_4V_{SAT}/(R_3 + R_4)$$

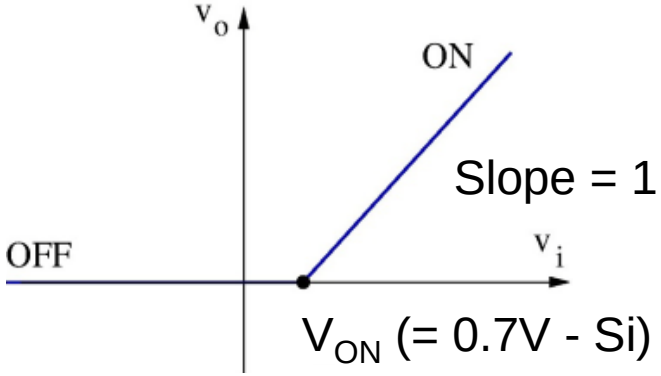
Chú ý: Còn nhiều dạng mạch so sánh khác!

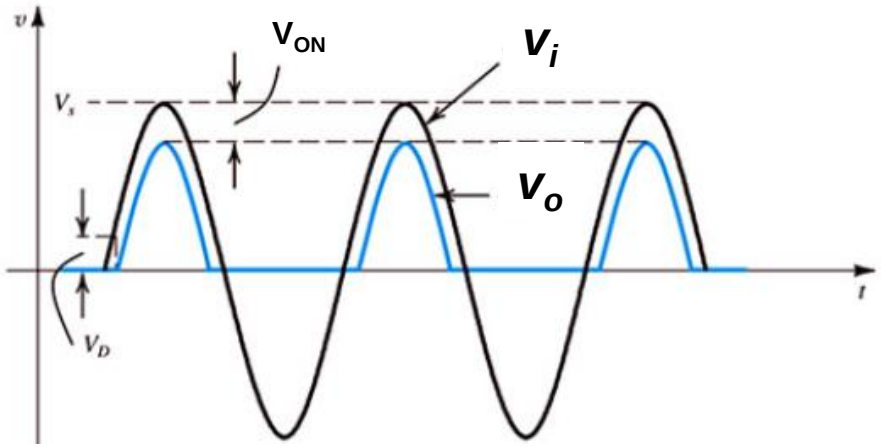
3.6 Rectifier

Normal diode

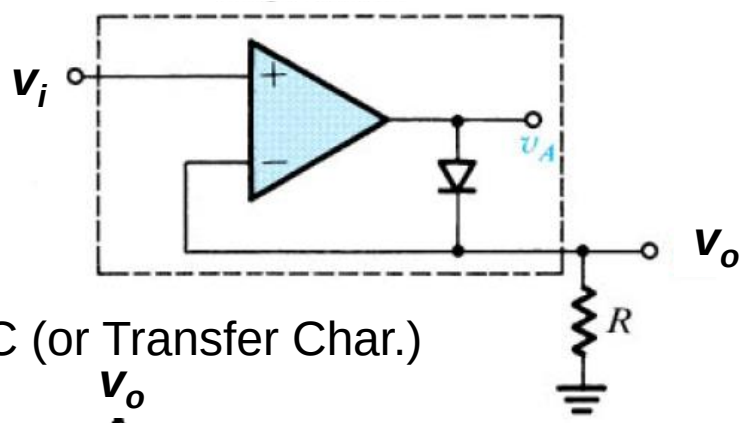


Voltage Transfer Curve (VTC)

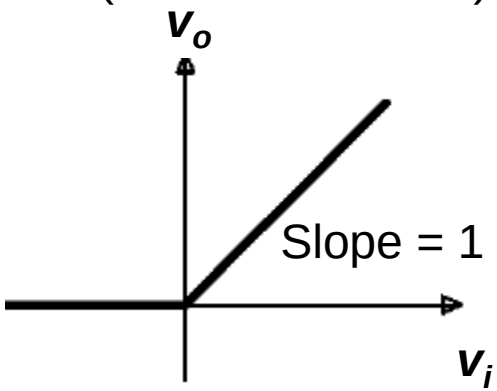


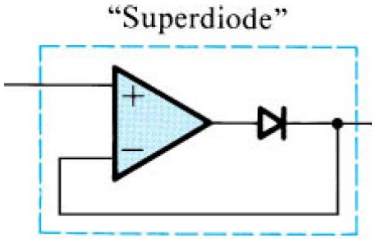


Super diode



VTC (or Transfer Char.)



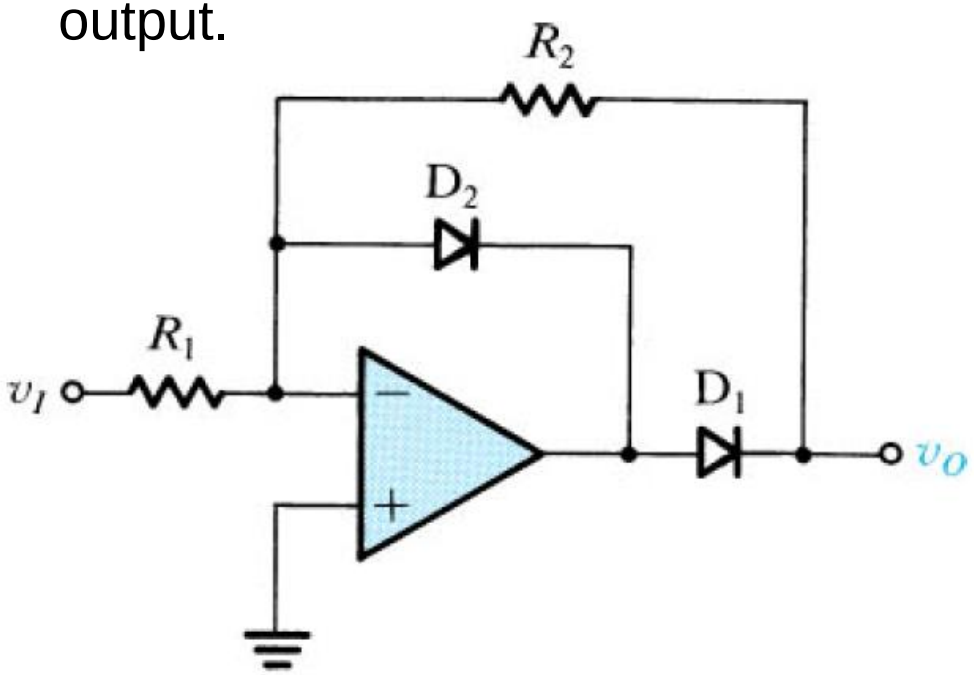


The circuit will not work well with high frequency signals.

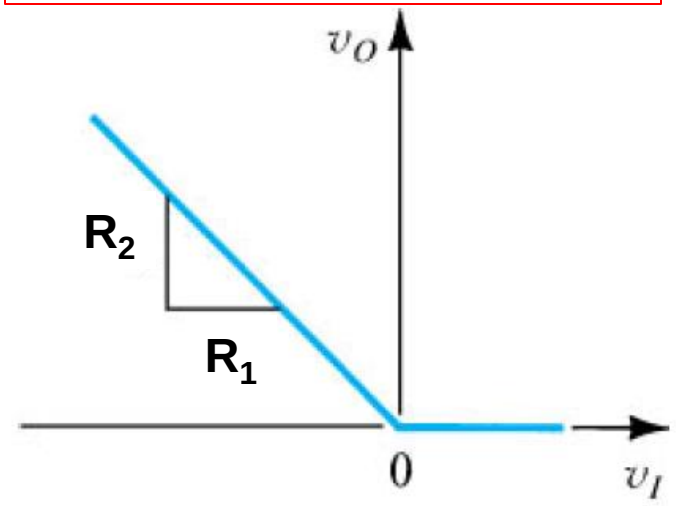
- When the input signal becomes negative, the op amp has no feedback at all, so the output pin of the op amp swings negative as far as it can.
- When the input signal becomes positive again, the op amp's output voltage will take a finite time to swing back to zero, then to forward bias the diode and produce an output. This time is determined by the op amp's slew rate

Another Circuit

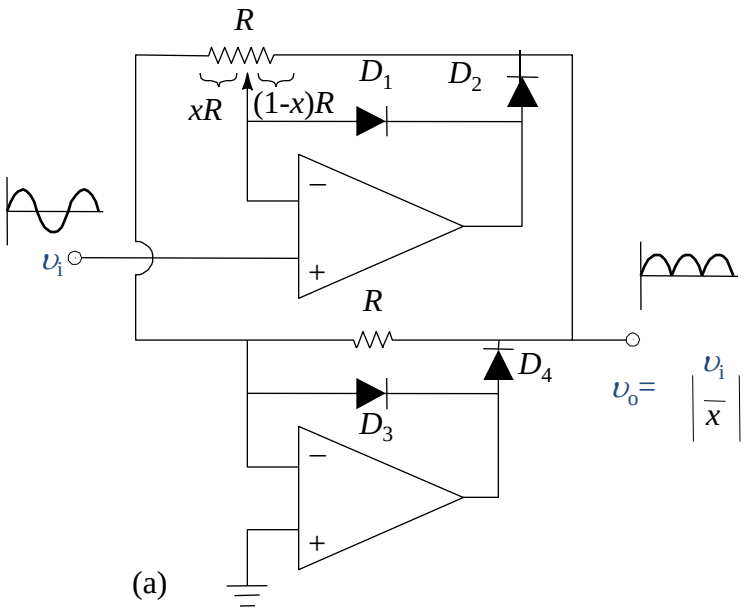
- The circuit below accepts an incoming waveform and as usual with op amps, inverts it. However, only the positive-going portions of the output waveform, which correspond to the negative-going portions of the input signal, actually reach the output.
- The direct feedback diode shunts any negative-going output back to the "-" input directly, preventing it from being reproduced. The slight voltage drop across the diode itself is blocked from the output by the second diode. D1 allows positive-going output voltage to reach the output.

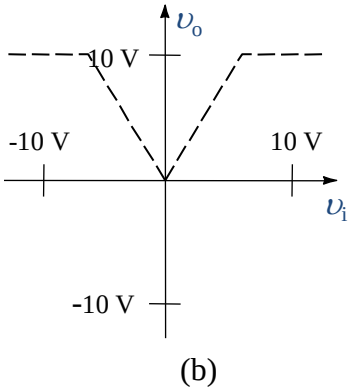


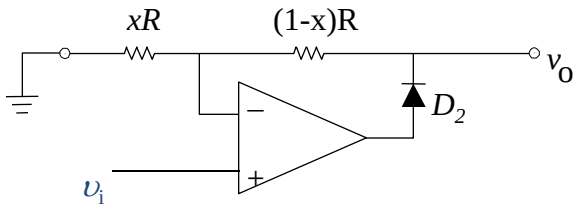
$V_O = -R_2V_i/R_1$ when $V_i < 0$
$V_O = 0$ when $V_i > 0$



Rectifier







(a)

V_O = $(1 + R_2/R_1)V_i$ when $V_i > 0$
$V_O = 0$ when $V_i < 0$
Therefore, when $V_i > 0$:
$V_O = (1 + (1-x)/x)V_i = V_i/x$

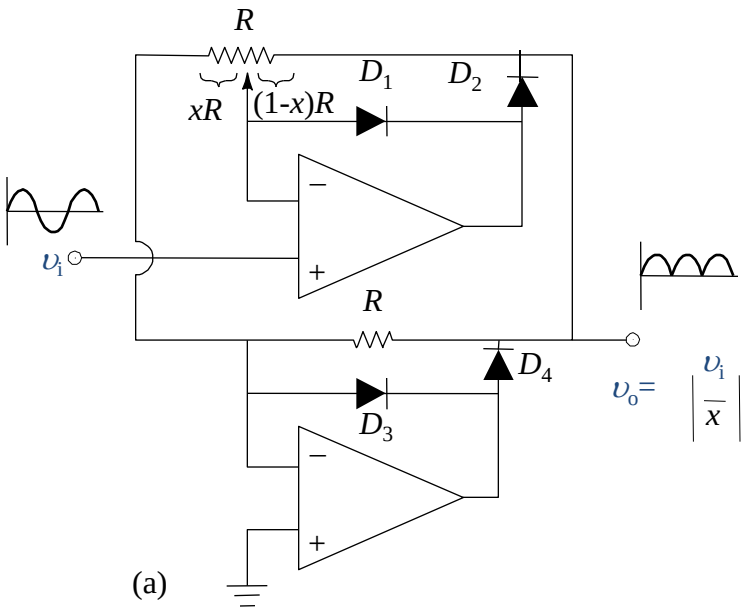
Full-wave precision rectifier:

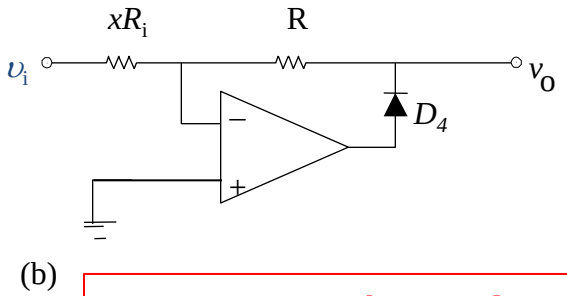
a) For $\upsilon_i > 0$,

D_2 and D_3 conduct, whereas D_1 and D_4 are reverse-biased.

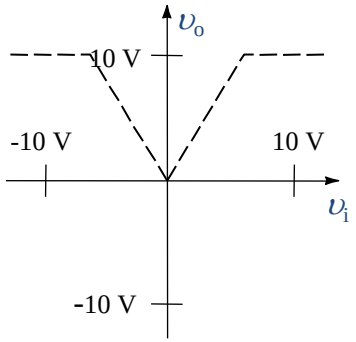
Noninverting amplifier at the top is active

Rectifier





$V_O = -R_2V_i/R_1$ when $V_i < 0$
$V_O = 0$ when $V_i > 0$
Therefore, when $V_i < 0$:
$V_O = -R/xR\ V_i = -V_i/x$



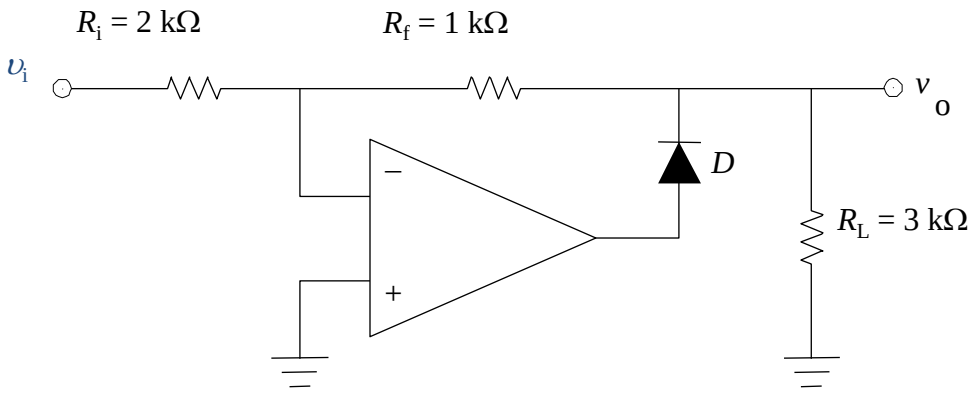
Full-wave precision rectifier:

b) For $\upsilon_i < 0$,

D_1 and D_4 conduct, whereas D_2 and D_3 are reverse-biased.

Inverting amplifier at the bottom is active

One-Op-Amp Full Wave Rectifier



(c)

For $\upsilon_i < 0$, the circuit behaves like the inverting amplifier rectifier with a gain of +0.5. For $\upsilon_i > 0$, the op amp disconnects and the passive resistor chain yields a gain of +0.5.

3.7 Mạch KĐ Logarithm

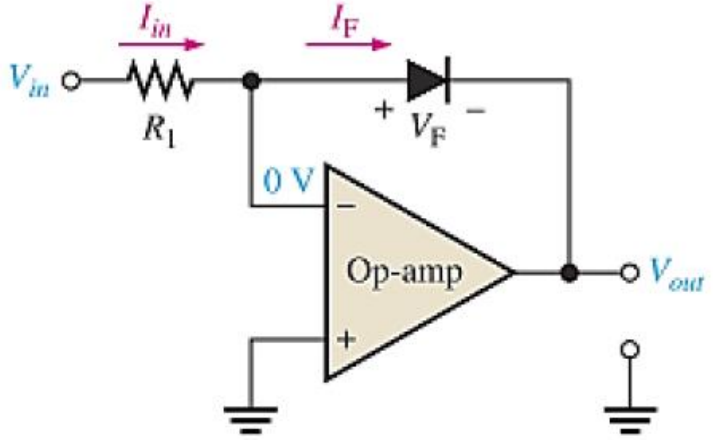
❖ Mạch KĐ Logarithm dùng diode

$$V_{out} = -V_F$$

$$I_F = I_{in} = \frac{V_{in}}{R_1}$$

$$V_{out} = -\left(\frac{kT}{q}\right)\ln\left(\frac{V_{in}}{I_R R_1}\right)$$

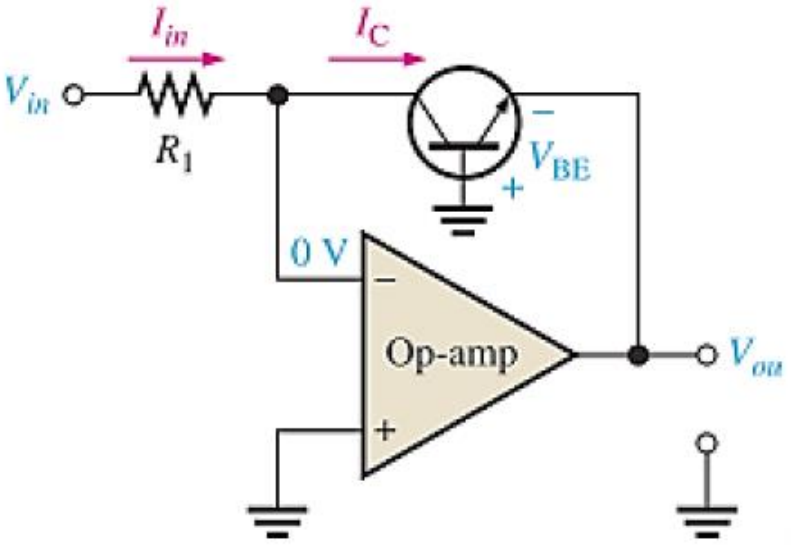
$$V_{out} \cong -(0.025\ \text{V})\ln\left(\frac{V_{in}}{I_R R_1}\right)$$



❖ Mạch KĐ Logarithm dùng BJT

$$I_C = I_{EBO}e^{qV_{BE}/kT}$$

$$V_{out} = -(0.025\ \text{V})\ln\left(\frac{V_{in}}{I_{EBO}R_1}\right)$$

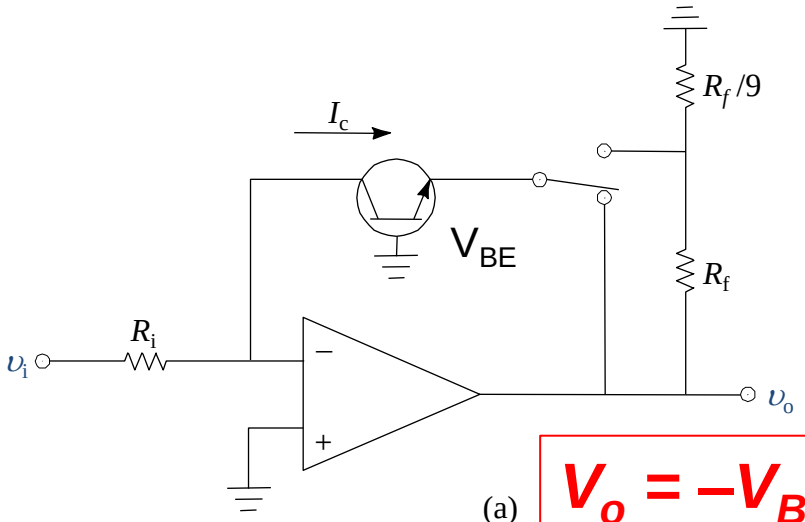


Logarithmic Amplifiers

Khi BJT ở chế độ tích cực:
$I_C = I_S \exp(V_{BE}/V_T)$
với $V_T = kT/q = 26mV$ ở $T = 300K$
Suy ra $V_{BE} = V_T \ln(I_C/I_S) = 2.303 V_T \log(I_C/I_S)$
Nếu $T = 300\ K \Rightarrow 2.303V_T \approx 0.06\ V$

Uses of Log Amplifier

1. Multiply and divide variables
2. Raise variable to a power
3. Compress large dynamic range into small ones
4. Linearize the output of devices



(a)

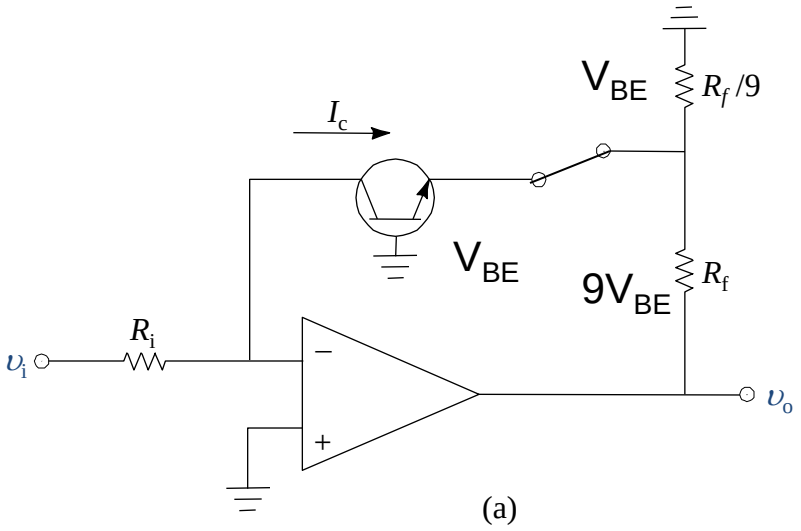
$$V_{BE} = 0.06 \log\left(\frac{I_C}{I_S}\right)$$

$$v_o = 0.06 \log\left(\frac{v_i}{R_i \cdot 10^{-13}}\right)$$

$V_o = -V_{BE} = -V_T \ln(I_C/I_S) = -V_T \ln(V_i/(R_i I_S))$

Figure 3.8 (a) A logarithmic amplifier makes use of the fact that a transistor's V_{BE} is related to the logarithm of its collector current. For range of I_c equal 10^{-7} to 10^{-2} and the range of v_o is -.36 to -0.66 V.

Logarithmic Amplifiers



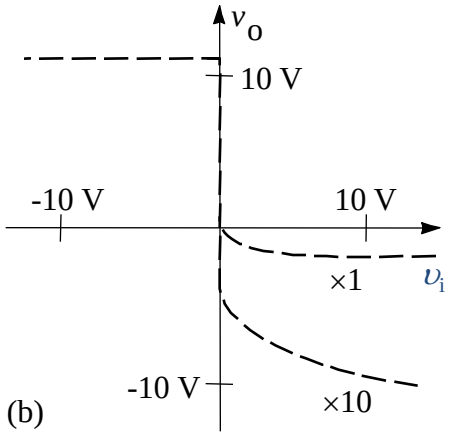


Figure 3.8 (a) With the switch thrown in the alternate position, the circuit gain is increased by 10. (b) Input-output characteristics show that the logarithmic relation is obtained for only one polarity; ×1 and ×10 gains are indicated.

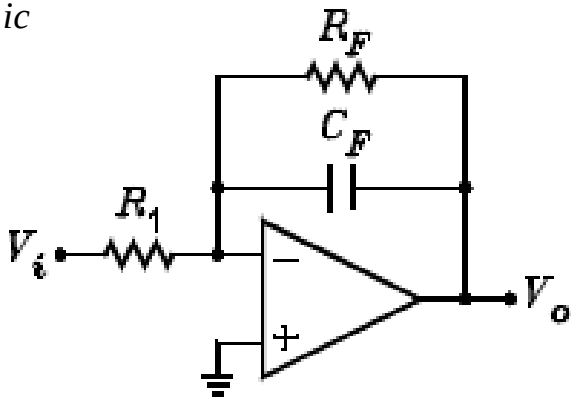
3.8 Integrators (Low-pass filter)

$$v_o = -\frac{1}{R_i C_f}\int_0^{t_1} v_i\,dt + v_{ic}$$

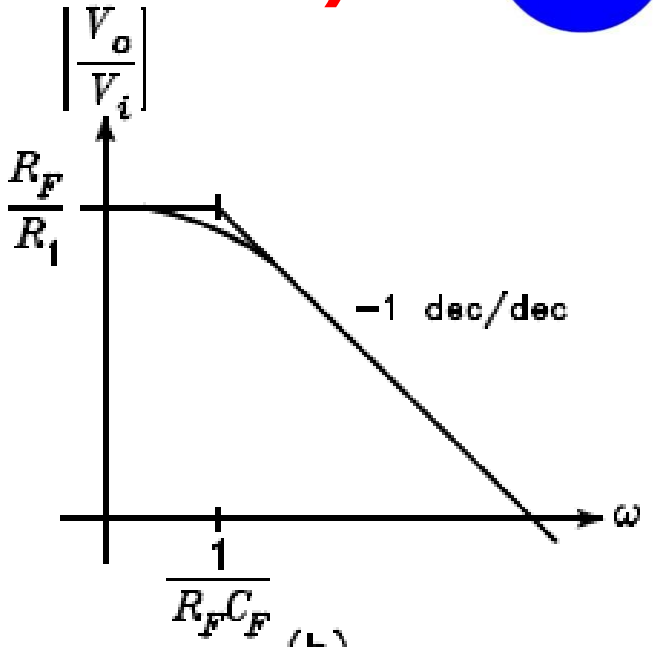
$$\frac{V_o(j\omega)}{V_i(j\omega)} = -\frac{Z_f}{Z_i}$$

$$Z_f = \frac{R_f}{1 + j\omega R_f C_f}$$

$$\frac{V_o(j\omega)}{V_i(j\omega)} = \frac{-R_f / R_i}{1 + j\omega R_f C_f}$$



(a)



(b)

$$\frac{v_o}{v_i} = \frac{-R_f}{R_i} \quad \text{for } f << f_c$$

$$\frac{v_o}{v_i} = \frac{-1}{j\omega R_i C_f} \quad \textbf{for } f >> f_c$$

$$f_c = \frac{1}{2\pi R_f C_f}$$

- Rf/Ri must be sufficiently small to minimize the effect of the offset
- RfCf must be sufficiently large so as to negligibly impact the input signal frequencies of interest

A large resistor R_f is used to prevent saturation

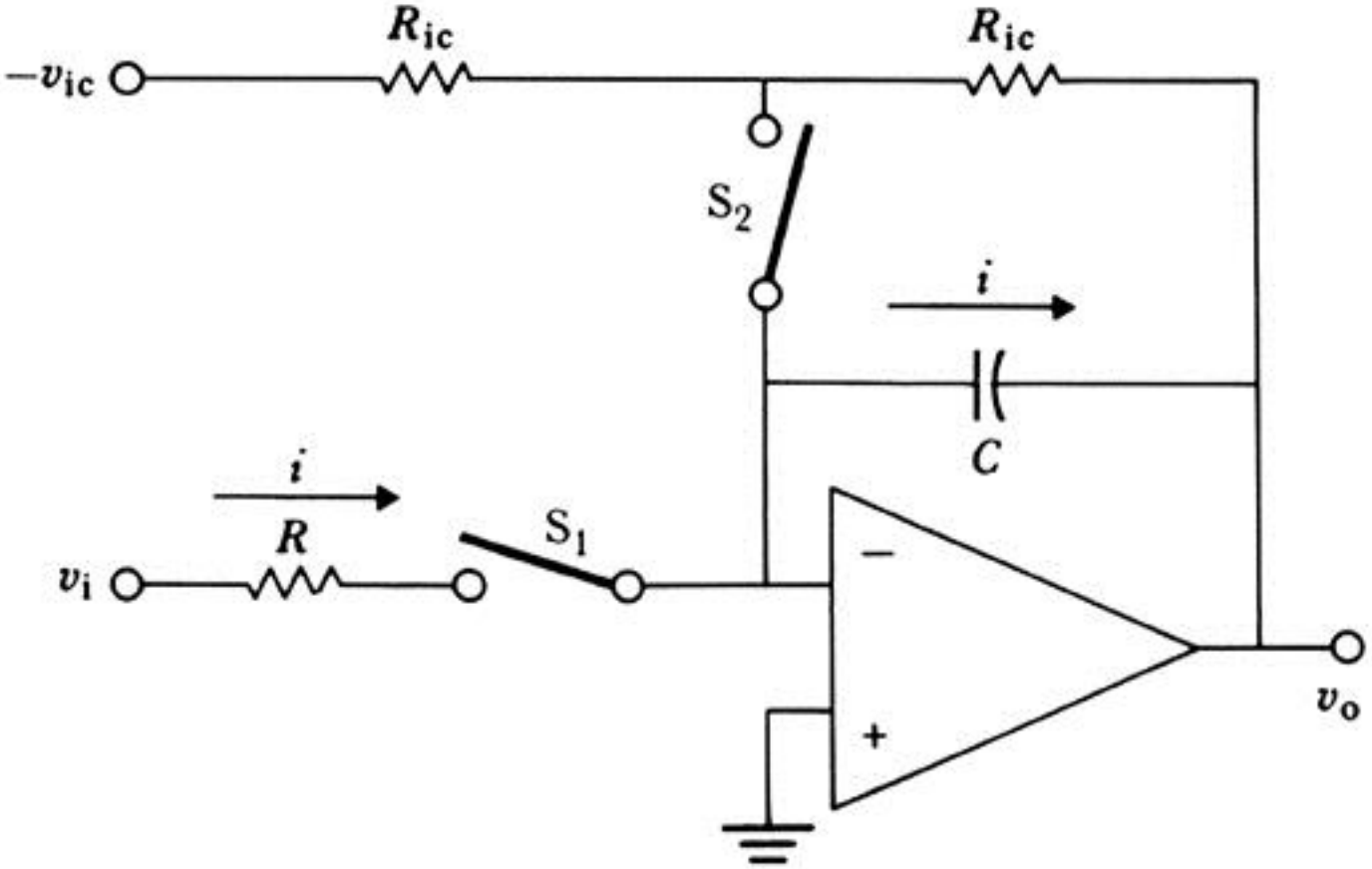


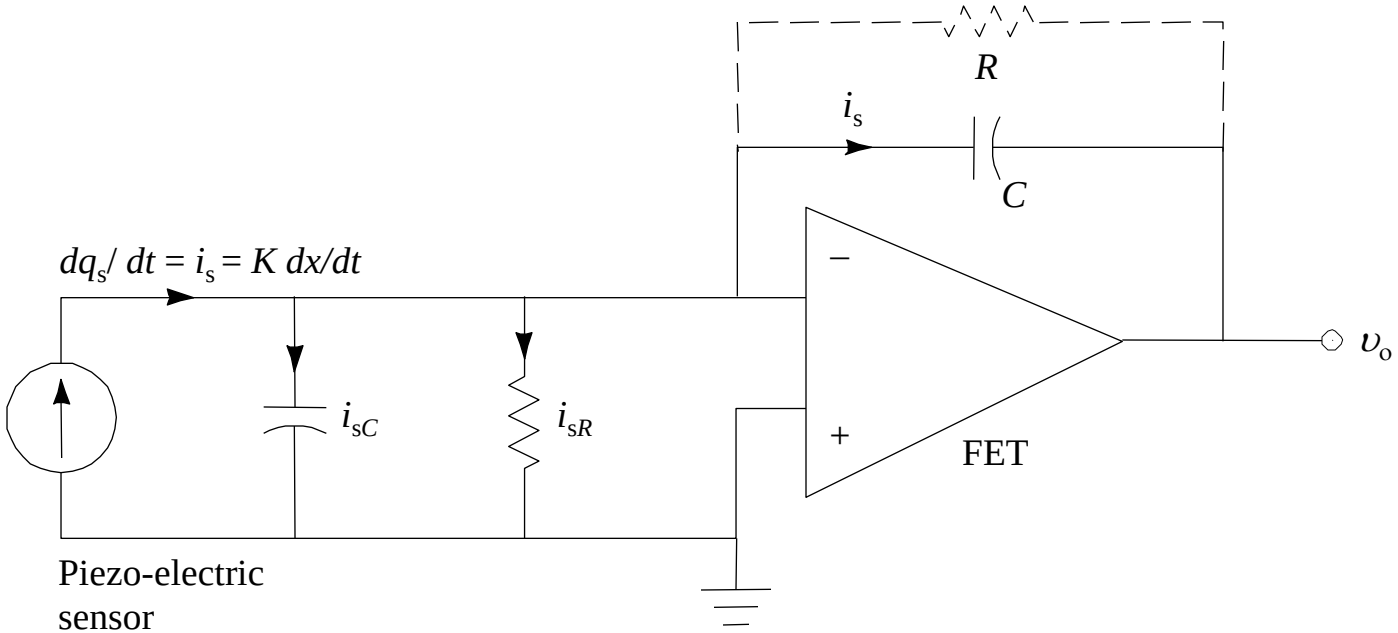
Figure 3.9 A three-mode integrator With S_1 open and S_2 closed, the dc circuit behaves as an inverting amplifier. Thus $\upsilon_o = \upsilon_{ic}$ and υ_o can be set to any desired initial conduction. With S_1 closed and S_2 open, the circuit integrates. With both switches open, the circuit holds υ_o constant, making possible a leisurely readout.

Example 3.2

The output of the piezoelectric sensor may be fed directly into the negative input of the integrator as shown below. Analyze the circuit of this charge amplifier and discuss its advantages.

$i_{sC} = i_{sR} = 0$

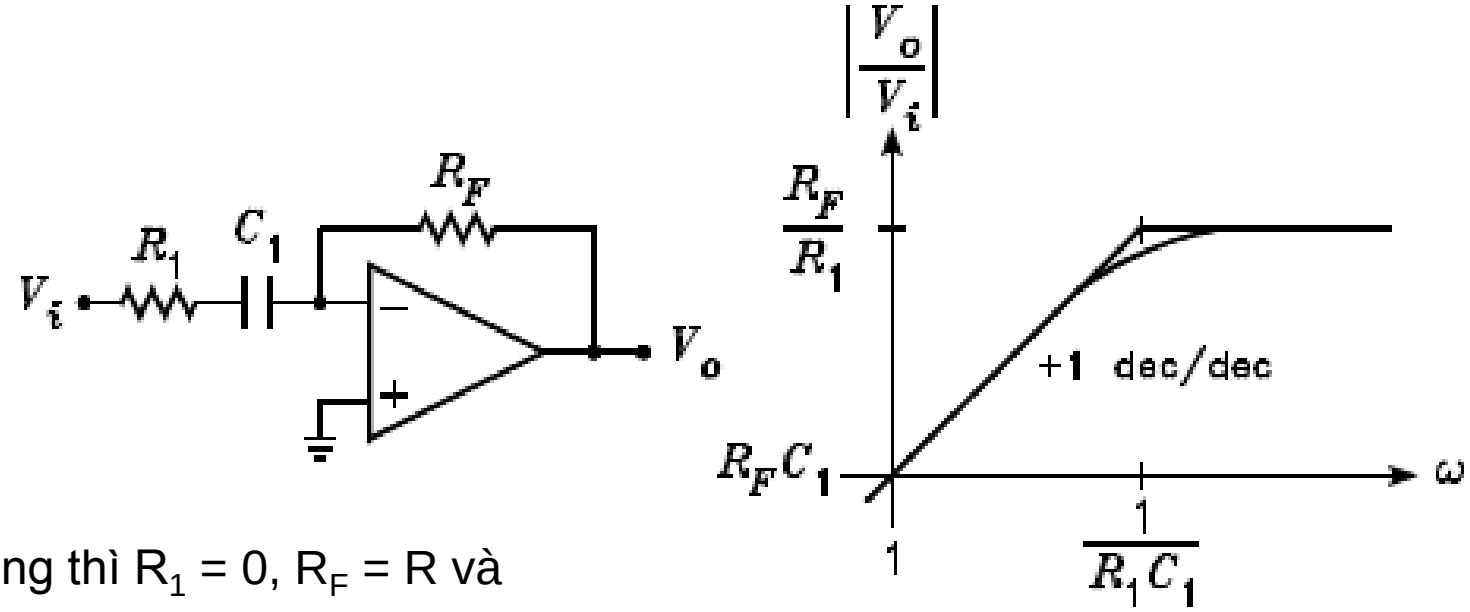
$v_o = -v_c$



$$v_o = -\frac{1}{C}\int_0^{t_1} \frac{Kdx}{dt}dt = -\frac{Kx}{C}$$

Long cables may be used without changing sensor sensitivity or time constant.

3.9 Differentiators (High-pass filter)



Lý tưởng thì $R_1 = 0$, $R_F = R$ và $C_1 = C$

$$v_o = -RC\frac{dv_i}{dt}$$

$$\frac{V_o(j\omega)}{V_i(j\omega)} = -\frac{Z_f}{Z_i} = -j\omega RC$$

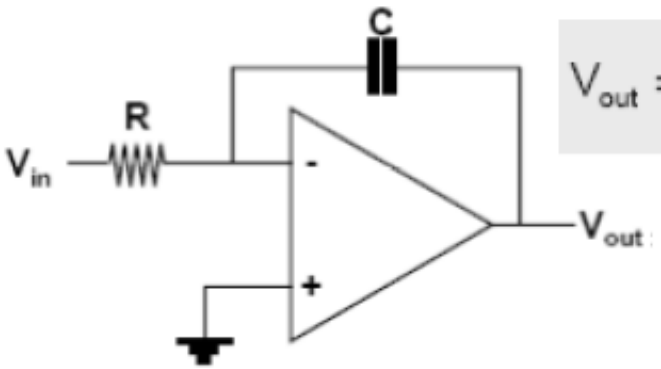
$$\frac{V_o}{V_i} = -\frac{R_F}{R_1 + 1/C_1 s} = -R_F C_1 s \times \frac{1}{1 + R_1 C_1 s}$$

Figure 3.11 A differentiator The dashed lines indicate that a small capacitor must usually be added across the feedback resistor to prevent oscillation.

Integrating/Differentiating Configurations

- Integrating Amp

$$v = \frac{1}{C}\int_{o}^{t} i\,dt$$

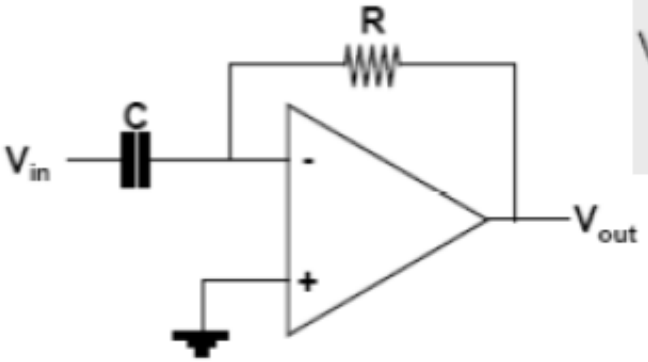


$$V_{out} = -\frac{1}{j\omega CR}V_{in} = -\frac{1}{RC}\int V_{in}\,dt$$

$$\omega = 2\pi f$$

- Differentiating Amp

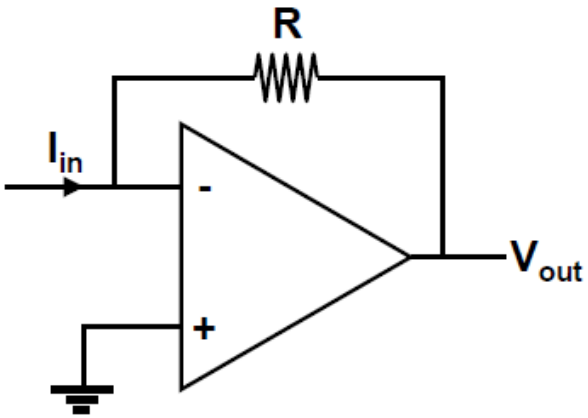
$$i = C\frac{dv}{dt}$$



$$V_{out} = -\frac{R}{\frac{1}{j\omega C}}V_{in} = -RC\frac{dV_{in}}{dt}$$

Converting Configurations

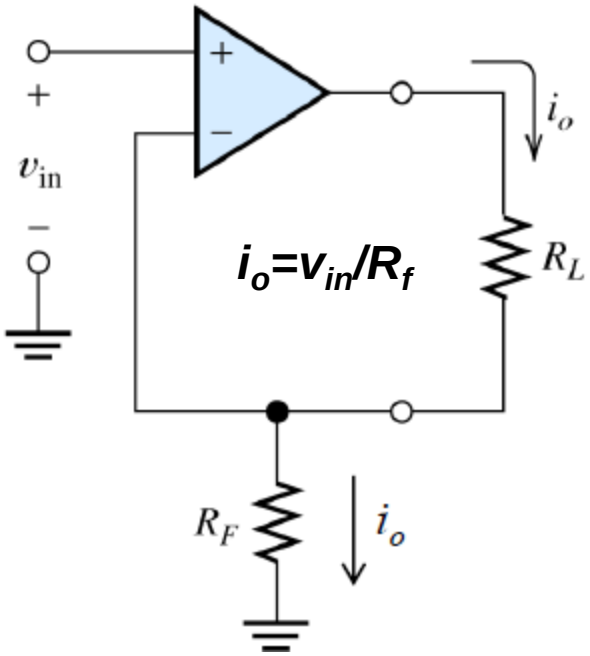
- Current-to-voltage



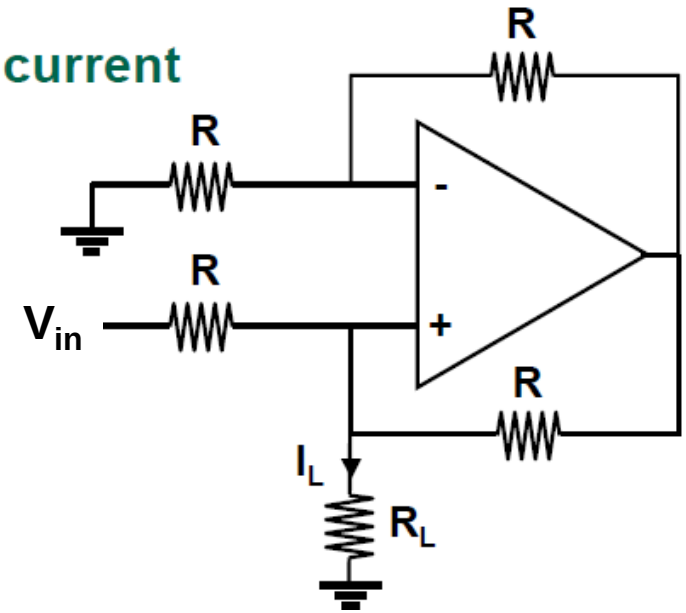
$$V_{out} = -I_{in}R$$

- Voltage to current

Tải thả nổi



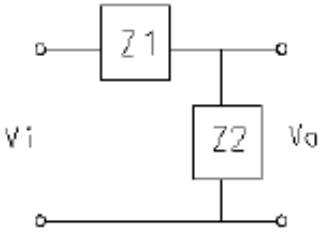
Tải nối đất



$$I_L = \frac{V_{in}}{R}$$

3.10 Active Filters

- Passive low pass filter

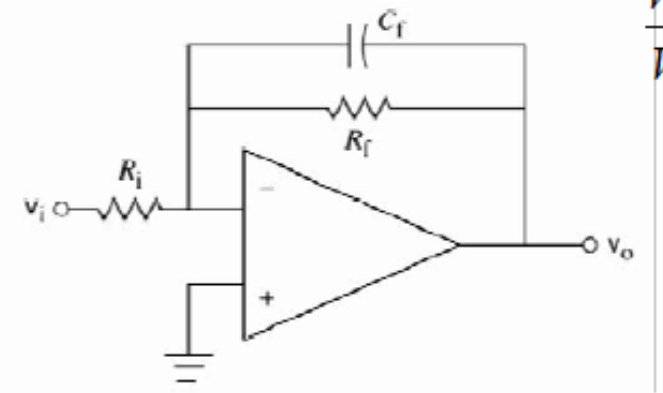


$$\frac{V_o}{V_i} = \frac{Z_2}{Z_1 + Z_2}$$

If Z1 is a resistor (R) and Z2 is a capacitor (1/sC) then

$$\frac{V_o}{V_i} = \frac{\frac{1}{sC}}{\frac{1}{sC} + R} = \frac{1}{1 + sCR}$$

- Active low pass filter



$$\frac{V_o(j\omega)}{V_i(j\omega)} = -\frac{Z_f}{Z_i} = -\frac{\frac{(R_f / j\omega C_f)}{[(1/j\omega C_f) + R_f]}}{R_i}$$

$$= -\frac{R_f}{(1 + j\omega R_f C_f) R_i} = -\frac{R_f}{R_i} \frac{1}{1 + s/\omega_0}$$

-3dB frequency

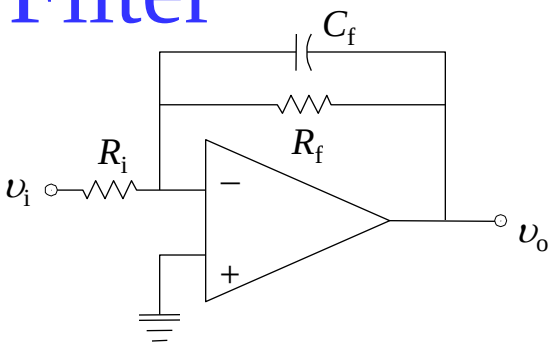
$$\omega_0 = 1/R_f C_f$$

$\omega = 2\pi f$

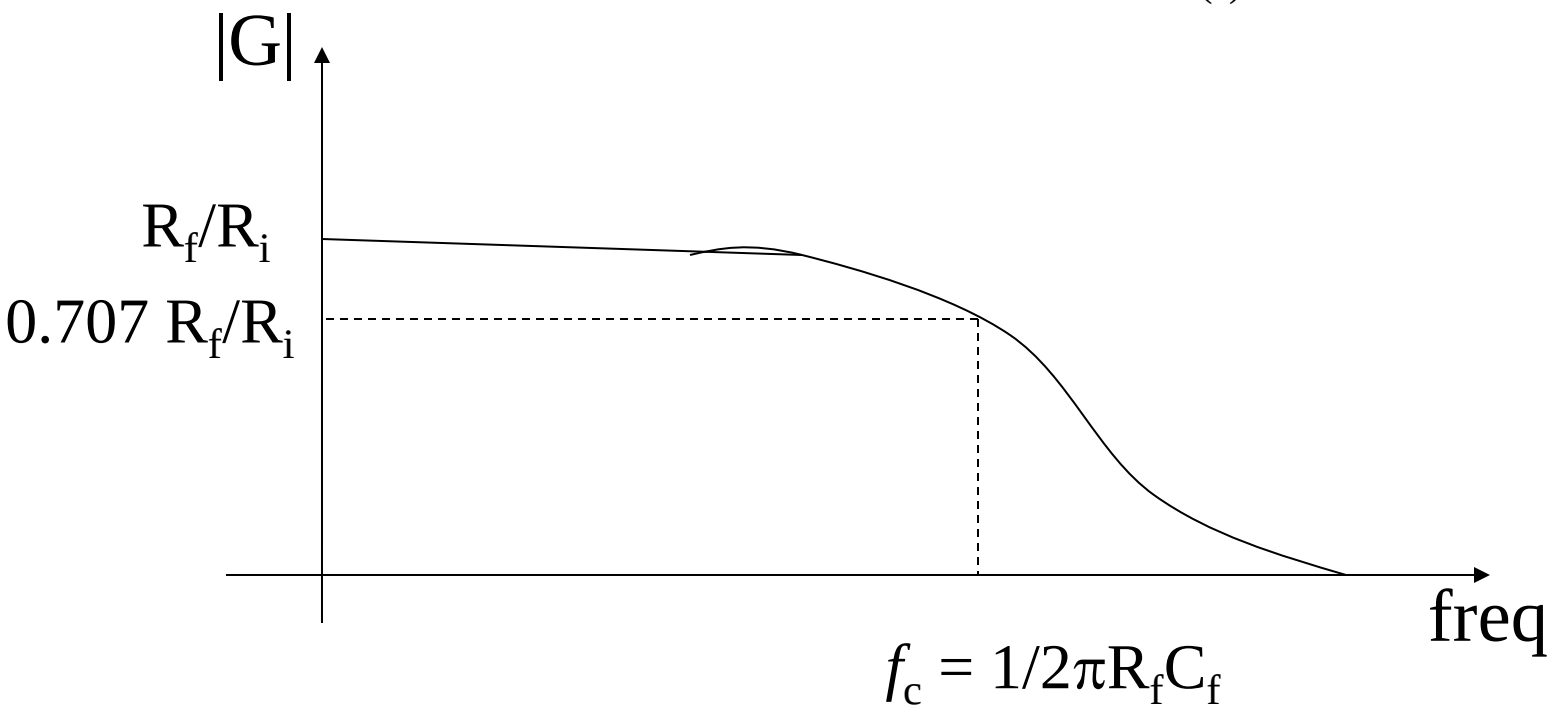
$$\frac{V_o}{V_i} = \frac{H_o \omega_o}{s + \omega_o} \qquad \frac{V_o(j\omega)}{V_i(j\omega)} = -\frac{R_f}{R_i} \frac{1}{1 + j\omega R_f C_f}$$

Active Filters- Low-Pass Filter

$$\text{Gain} = G = \frac{V_o(j\omega)}{V_i(j\omega)} = \frac{-R_f}{R_i}\,\frac{1}{1+ j\omega R_f C_f}$$



(a)

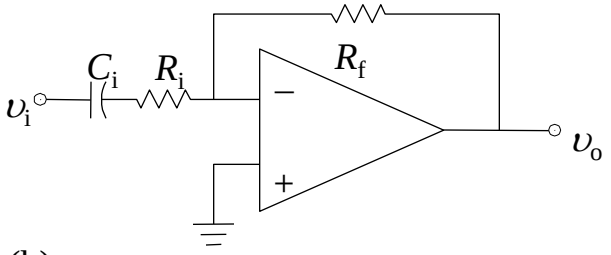


Active filters

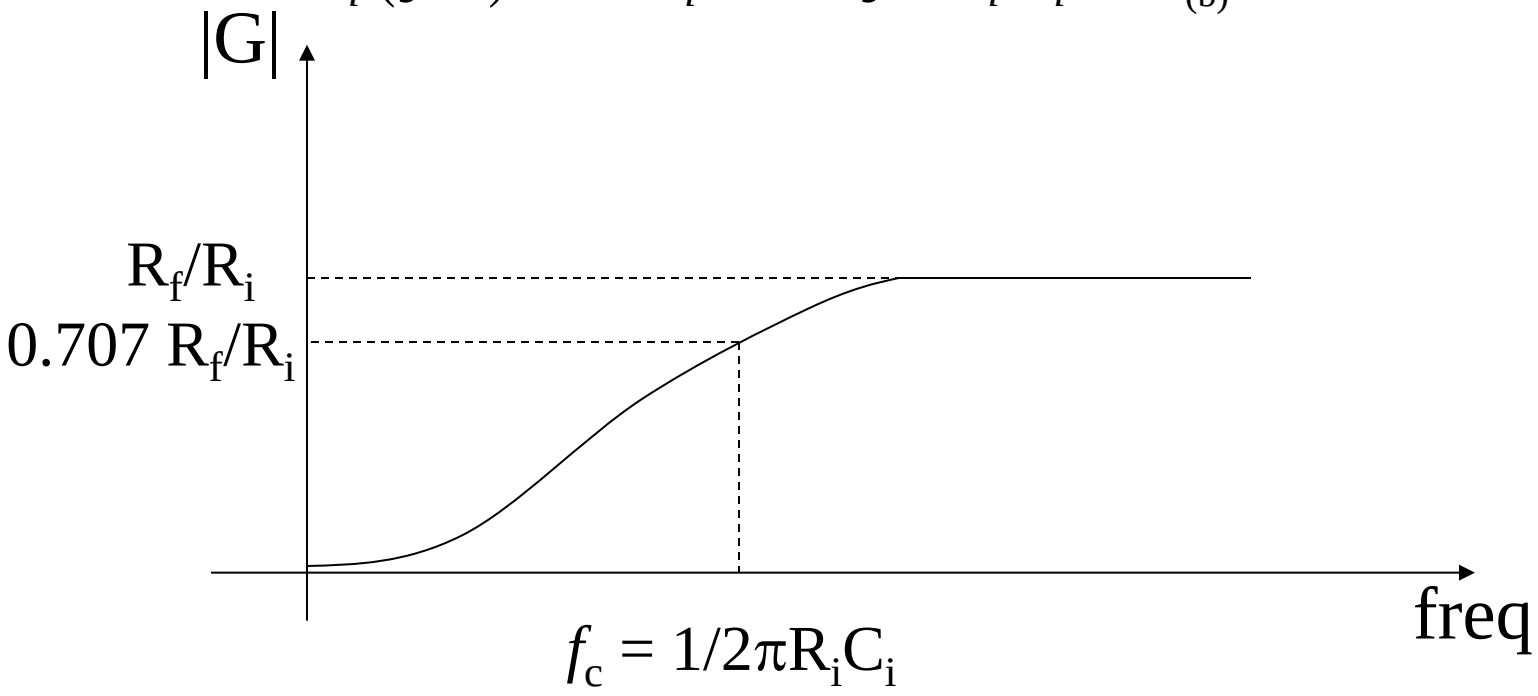
(a) A low-pass filter attenuates high frequencies

Active Filters (High-Pass Filter)

$$\text{Gain} = G = \frac{V_o(j\omega)}{V_i(j\omega)} = \frac{-R_f}{R_i}\,\frac{j\omega R_i C_i}{1 + j\omega R_i C_i}$$



(b)

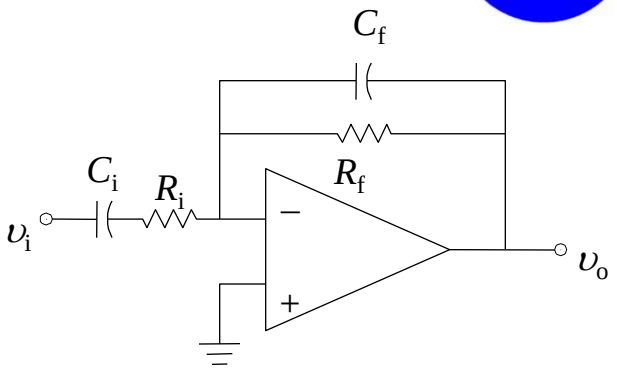


Active filters

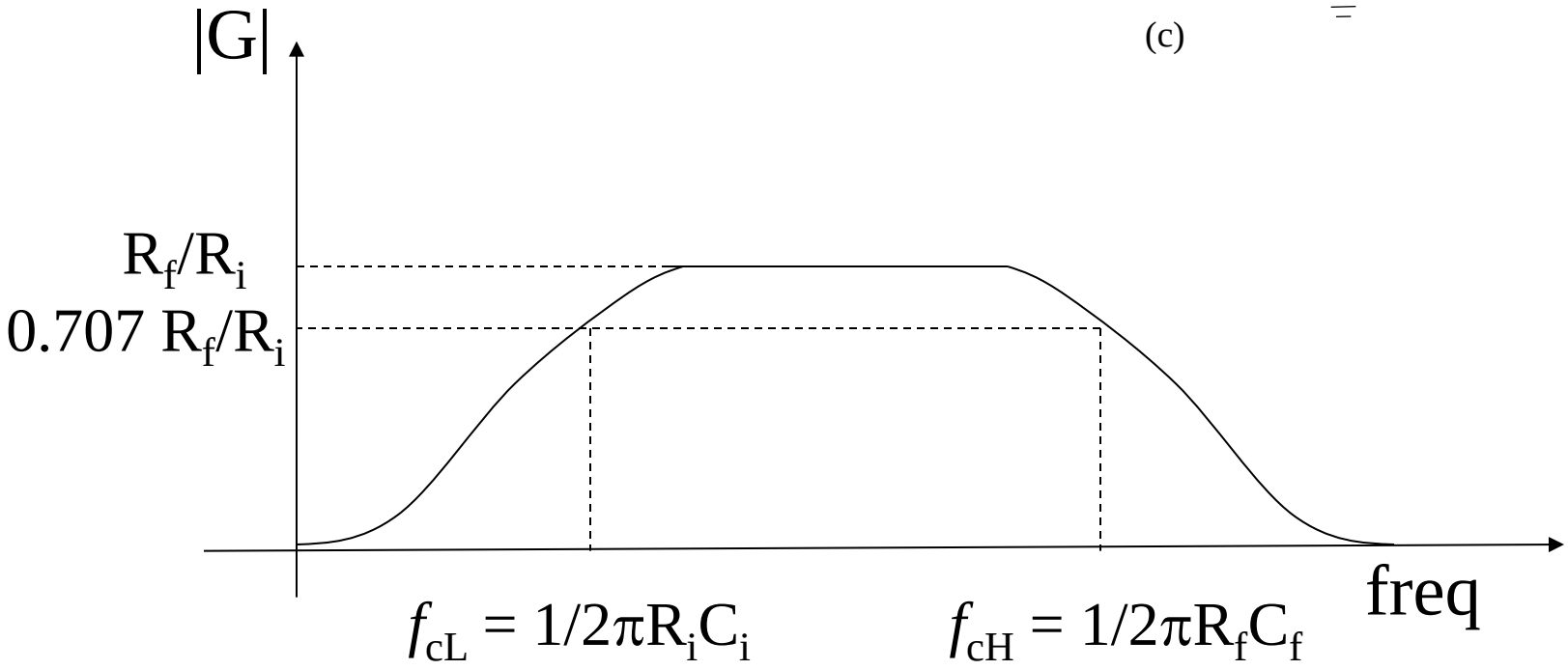
(b) A high-pass filter attenuates low frequencies and blocks dc.

Active Filters (Band-Pass Filter)

$$\frac{V_o(j\omega)}{V_i(j\omega)} = \frac{-j\omega R_f C_i}{(1+j\omega R_f C_f)(1+j\omega R_i C_i)}$$



(c)

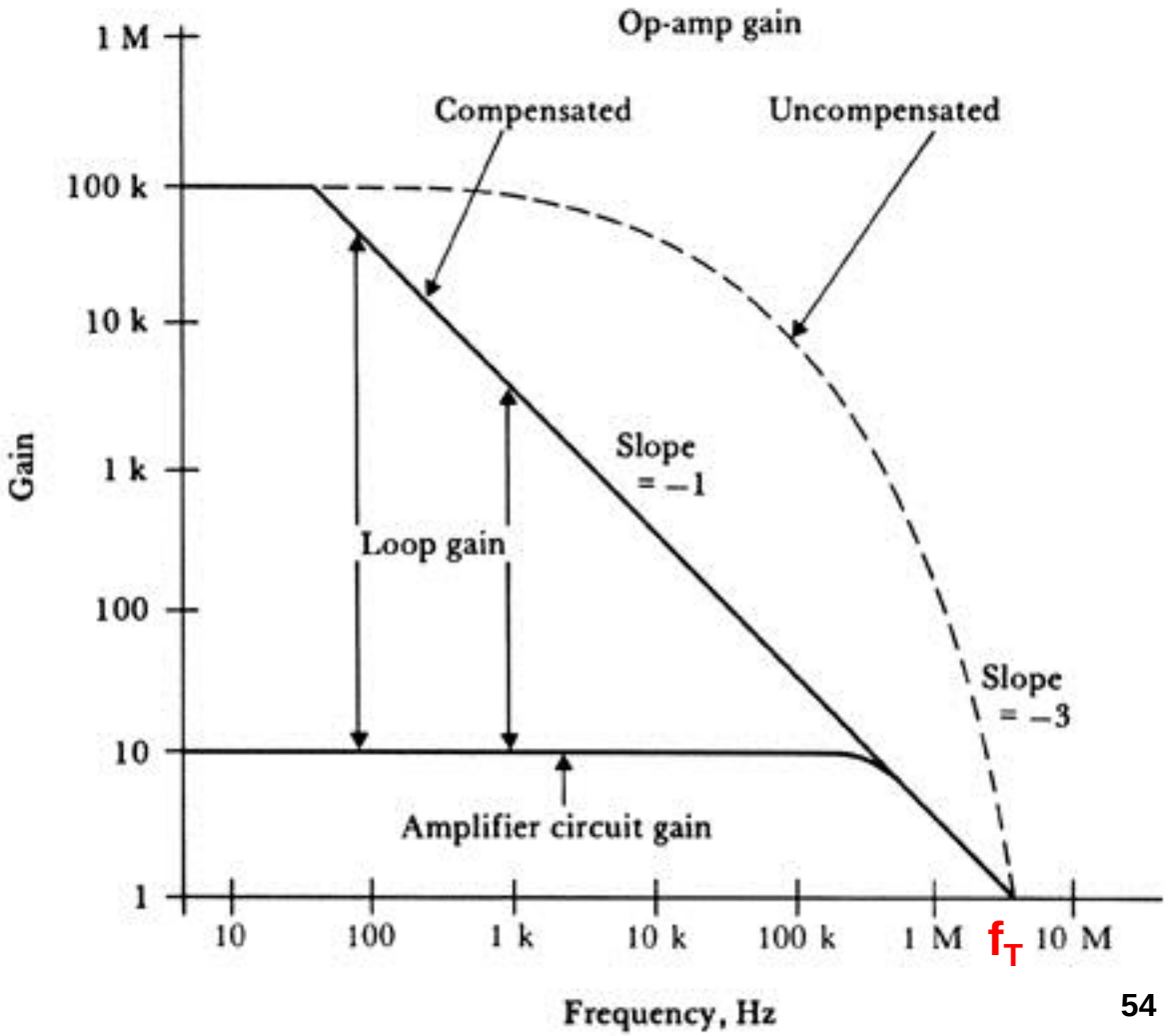


Active filters

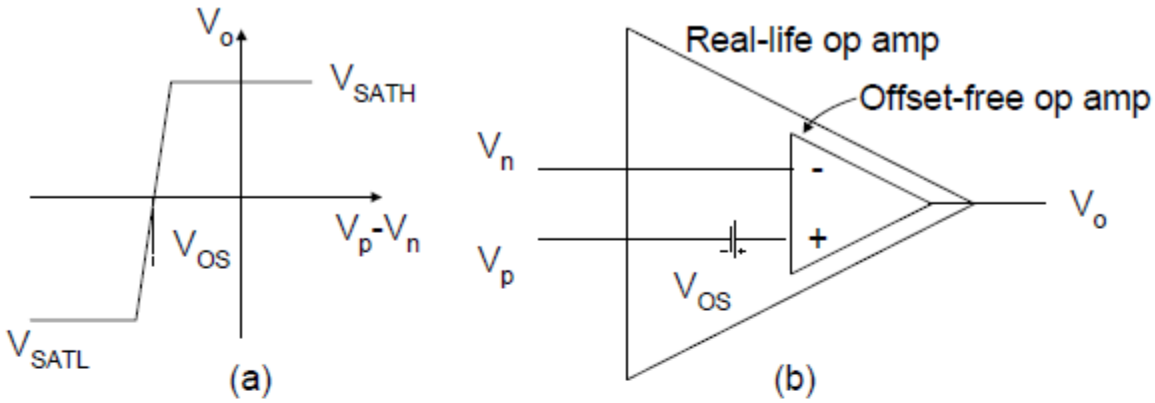
(c) A bandpass filter attenuates both low and high frequencies.

3.11 Frequency Response of op-amp and Amplifier

Open-Loop Gain
Compensation
Closed-Loop Gain
Loop Gain
Gain Bandwidth Product
Slew Rate



3.12 Offset Voltage (non-ideal characteristics)



(a) The VTC of an actual op amp is shifted because of the input offset voltage. (b) Op amp model to account for V_{OS}.

According to definition, shorting the inputs of an op amp together should yield 0 V at the output: $V_o = a(V_p - V_n) = a \times 0 = 0$ V. However, an actual op amp will yield a nonzero output even though the inputs are tied together. This is equivalent to saying that the VTC doesn't go through the origin, but is offset either to the right or to the left, depending on the direction of the mismatch. To force the output to zero, we must apply a suitable correcting voltage at the input. This voltage is called the ***input offset voltage***, V_{OS}.

$$V_n = V_p + V_{OS}$$

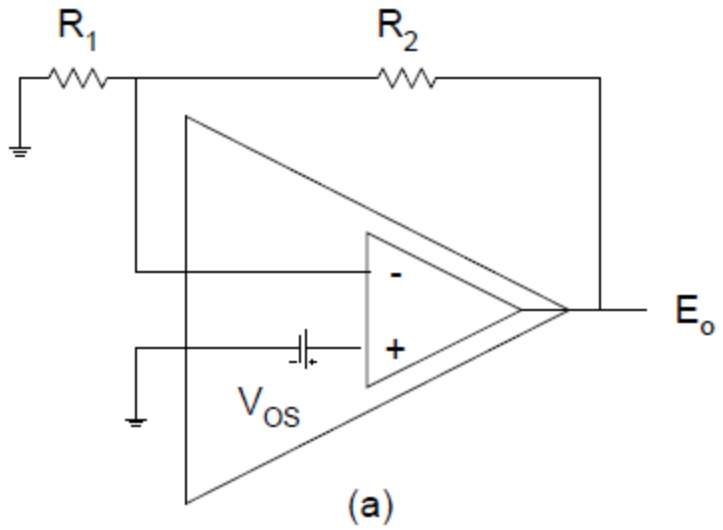
For the 741C, V_{OS}=2 mV (typical), 6 mV (max);

For the 741E, V_{OS}=0.8 mV (typical), 3 mV (max)

● Errors Caused by V_{OS}

The presence of V_{OS} may or may not be a drawback depend**ing** on the application (dc or ac). In audio application, where dc voltages are usually blocked out by capacitive coupling, offset voltages are seldom of major concern. Not so in low-level signal detection, such as thermocouple or strain gauge amplification, or in wide dynamic range applications, such as logarithmic compression and high-resolution A-D and D-A conversion.

1. Resistive feedback:



Estimating the output error caused by V_{OS}. (a) Resistive feedback configuration.

$$E_o = \left(1 + \frac{R_2}{R_1}\right) V_{os}$$

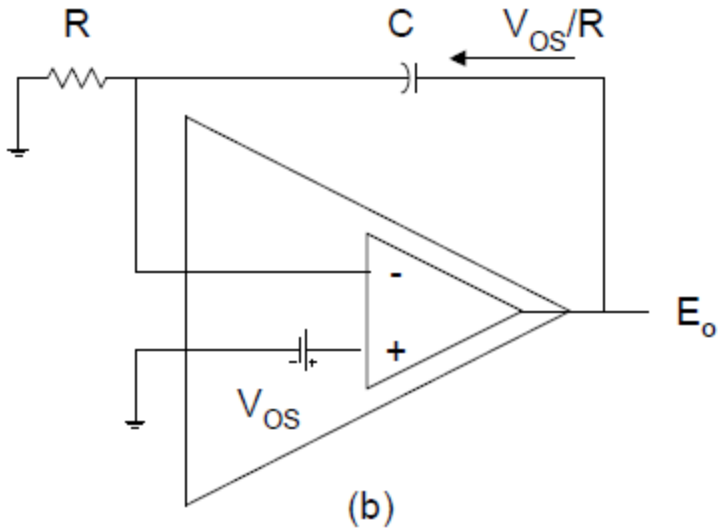
E_o is regarded as a form of *error*, more properly, ***dc noise***. Clearly, the larger the noise gain $1 + R_2 / R_1$, the larger the error. For a gain of 1000 yields

$$E_o = (1+1000)(\pm 2mV) = \pm 2V(typ), \quad \pm 6V(\max).$$

The circuit shown above can be used to measure V_{OS},

$$V_{os} = \frac{E_o}{1 + R_2 / R_1}$$

2. Integrator circuit:



(b)

Estimating the output error caused by V_{OS}. (b) Integrator configuration.

Since the offset-free op amp keeps $V_n = V_{os}$, the resistor conducts current

$I_R = V_n / R = V_{os} / R = I_c$.

➔ $E_o(t) = \frac{1}{RC}\int_0^t V_{os}\,dt + E_o(0)$ where $E_o(0)$ is the output voltage at $t=0$.

● Temperature Drift

V_{OS} is temperature-dependent. The dependence is expressed in terms of the average temperature coefficient of V_{OS}, $\Delta V_{OS}/\Delta T$. On the basis of the average temperature coefficient one can estimate the value of V_{OS} at a temperature other than 25℃ as

$$V_{os}(t) \approx V_{os}(25^oC) + \frac{\Delta V_{os}}{\Delta T}(T - 25^oC)$$

● Power Supply Rejection Ratio (PSRR)

Changing the supply voltages alters the operating point of the internal transistors, and this in turn induces a change in V_{OS} to supply voltage changes is expressed in term of the ***power supply rejection ratio***:

$$PSRR \triangleq \frac{\Delta V_{os}}{\Delta V_{\text{sup } ply}} \ (\mu V/V)$$

The PSRR ratings of most op amps tend to fall in the range of 80 to 120 dB.

Note: $\text{PSRR} = 20\log\left[\Delta V_{\text{sup } ply} / \Delta V_{os}\right]$ (dB)

When the op amp is powered from well-regulated and clean dual tracking supplies, the effect of finite PSRR is usually negligible in comparison with other source of error. This not so when the supply is poorly regulated or poorly filtered, for then any variation on the supply buses will induce a corresponding variation in V_{OS}, which in turn will be amplified by the noise gain of the circuit.

The op amp's ability to reject power supply changes deteriorates with frequency.

● Common-Mode Rejection Ratio (CMRR)

A real-life op amp is **also sensitive to the input common-mode component**, not just to the input difference. This behavior is expressed by means of the *common-mode rejection ratio*:

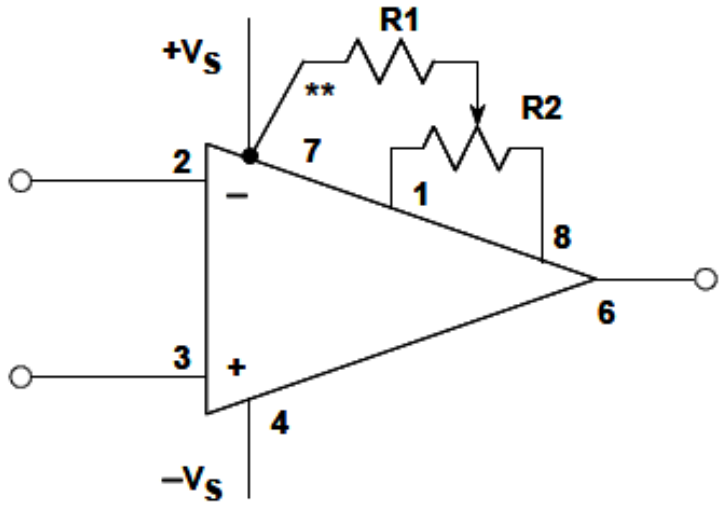
$$CMRR \triangleq \frac{\Delta V_{os}}{\Delta V_{cm}} \qquad (\mu V/V)$$

Note: $\text{CMRR} = 20\log[\Delta V_{cm} / \Delta V_{os}]$ (dB)

The ratings for the 741C are CMRR= 90 dB (typical), 70 dB (min). Usually the CMRR is of the same order of magnitude as the PSRR and starts to deteriorate with frequency in the 10 Hz to 100 Hz range.

In inverting-type applications the CMRR is irrelevant since V_p and V_n are kept fixed. However, in noninverting and in difference amplifier applications, V_p is allowed to float and the effect of finite CMRR is, therefore, felt at the output. Examples in which the CMRR can be critical are the precision voltage follower and the instrumentation amplifier, where sensitivity to common-mode signals is one the most crucial performance parameters.

OFFSET VOLTAGE ADJUSTMENT USING “OFFSET-NULL" PINS



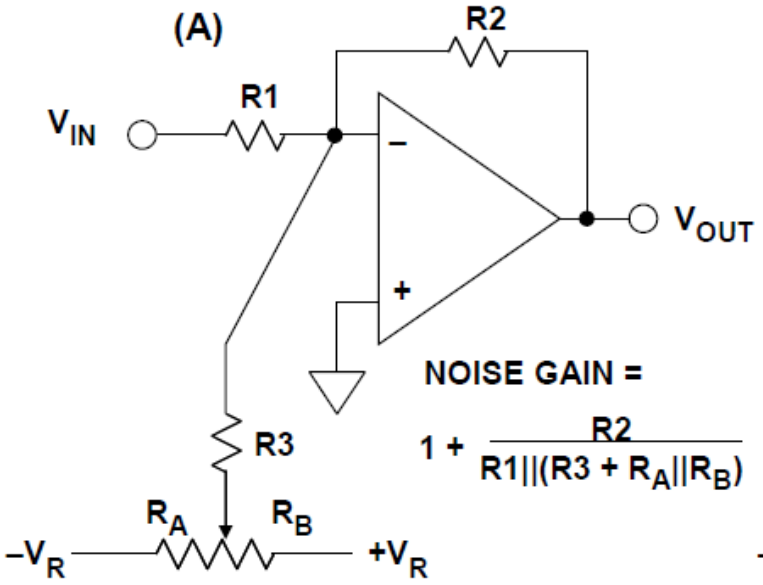
- ** Wiper connection may be to either $+V_S$ or $-V_S$ depending on op amp
- R values depend on op amp. Consult data sheet
- Use to null out input offset voltage, not system offsets!
- There may be high gain from offset pins to output — Keep them quiet!
- Nulling offset causes increase in offset temperature coefficient, approximately 4μV/°C for 1mV offset null for FET inputs

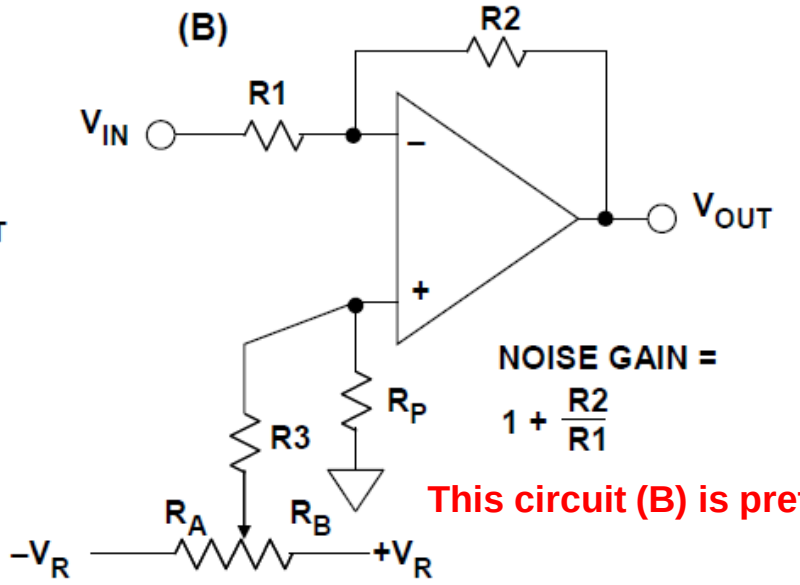
Ref: Analog Devices

OFFSET ADJUSTMENT (EXTERNAL METHODS) – 1/2

If an op amp doesn't have offset adjustment pins (popular duals and all quads do not), and it is still necessary to adjust the amplifier and system offsets, an external method can be used.

Inverting Op Amp External Offset Trim Methods





This circuit (B) is preferred.

$$V_{OUT} = -\frac{R2}{R1} V_{IN} \pm \underbrace{\frac{R2}{R3} V_R}_{\text{MAX OFFSET}}$$

$$V_{OUT} = -\frac{R2}{R1} V_{IN} \pm \underbrace{\left[1 + \frac{R2}{R1}\right] \left[\frac{R_P}{R_P + R3}\right] V_R}_{\text{MAX OFFSET}}$$

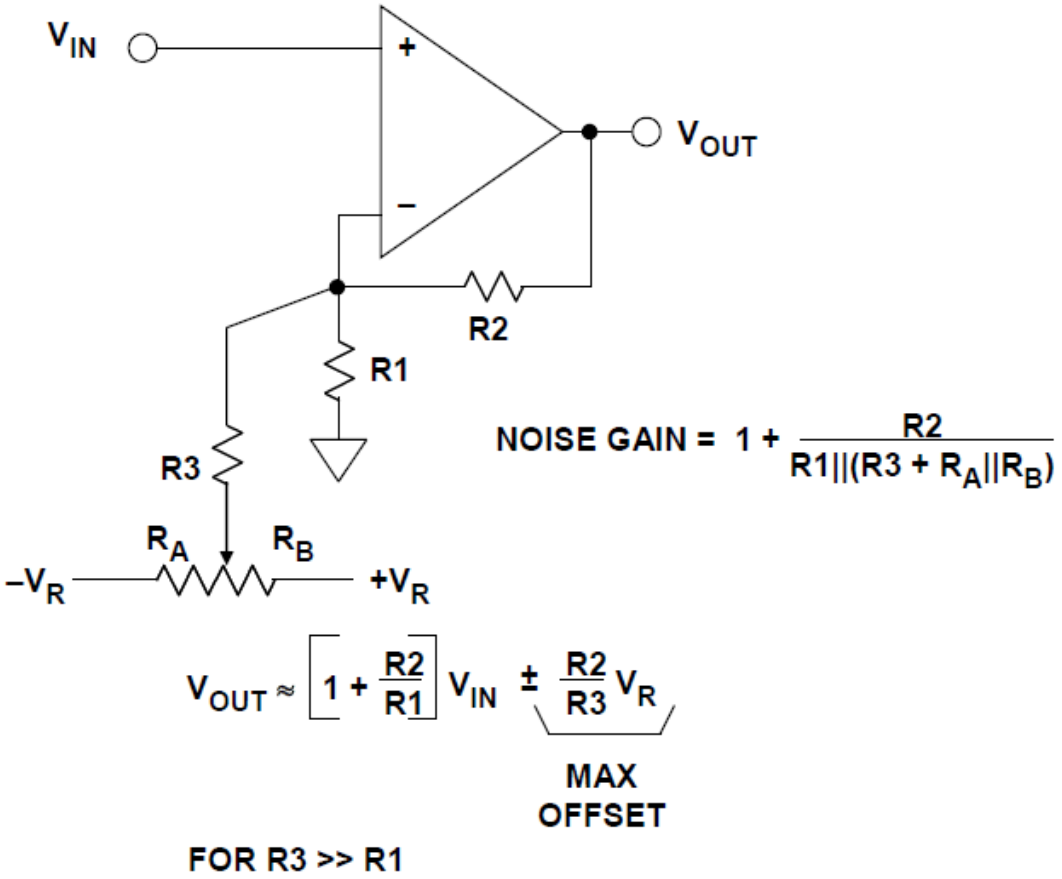
$R_P = R1||R2$ IF $I_{B+} \approx I_{B-}$

$R_P \leq 50\Omega$ IF $I_{B+} \neq I_{B-}$

Ref: Analog Devices

OFFSET ADJUSTMENT (EXTERNAL METHODS) – 2/2

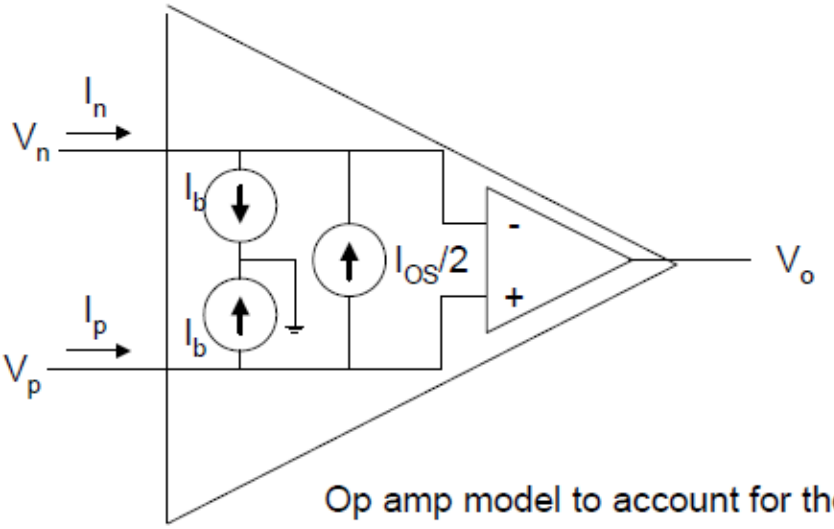
Non-Inverting Op Amp External Offset Trim Methods



The circuit can be used to inject a small offset voltage when using an op amp in the non-inverting mode. This circuit works well for small offsets, where R3 can be made much greater than R1. Note that otherwise, the signal gain might be affected as the offset potentiometer is adjusted. The gain may be stabilized, however, if R3 is connected to a fixed low impedance reference voltage sources, $\pm V_R$.

Ref: Analog Devices

3.13 Bias Current



Op amp model to account for the input currents.

Practical op amps do sink (or source) a tiny current at each input, and this may in turn cause unacceptable error in certain applications. Designate the current associated with the inverting input as I_n and that with the non-inverting input as I_p. Because of unavoidable mismatches between the two halves of the input stage, particularly between the betas (β) of Q1 and Q2, I_n and I_p will themselves be mismatched. The ***input bias current***, I_B, is then define as the average of the two:

$$I_B \triangleq \frac{I_p + I_n}{2}$$

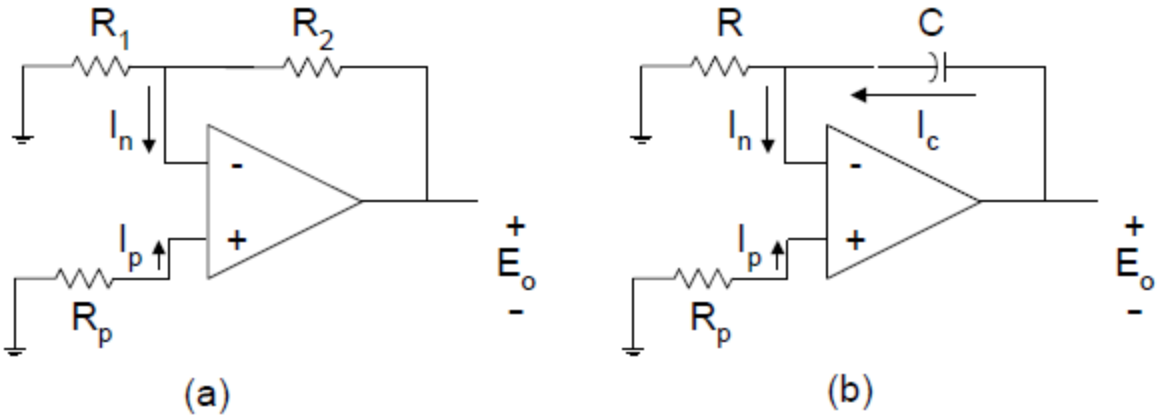
while their difference is called ***input offset current***:

$$I_{OS} \triangleq I_p - I_n$$

While the polarity of I_B can be determined once the input transistor type (*npn* or *pnp*) is known, the polarity of I_{OS} is depends on the direction of mismatch of the particular op amp sample. Usually I_{OS} is an *order of magnitude less* than I_B.

• Errors Caused by I_B and I_{OS}

A straightforward way of assessing the effect of nonzero input current upon circuit performance is to determine the *output with zero-input signal*.



Estimating the output error by the input bias current. (a) Resistive feedback configuration. (b) Integrator configuration.

(a) Resistive feedback configuration:

Ohm's law: $V_p = -R_p I_p$

KCL at the inverting input: $\dfrac{0 - V_n}{R_1} + \dfrac{E_o - V_n}{R_2} = I_n$

By op amp action: $V_n = V_p$

➔ $$E_o = \left(1 + \frac{R_2}{R_1}\right)\left[(R_1 // R_2) I_n - R_p I_p\right]$$

The circuit takes the difference between two input voltages, one due to I_n flowing through $R_1 // R_2$, the other due to I_p flowing through R_p. Gain $(1 + R_2 / R_1)$ is called the ***noise gain*** of the circuit. For ideal op amp we would have $E_o = 0$.

◆ If we apply a useful signal V_i at input side, then

$$V_o = \left(1 + \frac{R_2}{R_1}\right) V_i + E_o \text{ for the noninverting}$$

$$V_o = -\frac{R_2}{R_1} V_i + E_o \text{ for the inverting one}$$

◆ If $R_p = (R_1 // R_2)(I_n / I_p)$ then $E_o = 0$

◆ In practical situations, using a fixed dummy resistor of value $R_p = R_1 // R_2$. The output error

is then reduced to $$E_o = \left(1 + \frac{R_2}{R_1}\right)\left[-(R_1 // R_2) I_{OS}\right]$$

(b) Integrator configuration:

KCL at the inverting node, $$\frac{0 - V_n}{R} + I_c = I_n$$

➔ $$I_c = I_n - \frac{R_p}{R} I_p \qquad \text{(imposing } V_n = V_p = -R_p I_p\text{)}$$

Using the capacitor I-V relationship, $V_c = \frac{1}{C}\int I_c dt$, we obtain

$$E_o(t) = \frac{1}{C}\int_0^t \left[I_n - \frac{R_p}{R} I_p \right] dt + E_o(0)$$

The circuit is integrating an error signal consisting of the difference $I_n - (R_p / R) I_p$. This difference, when integral over prolonged time, will cause the op amp to saturate.

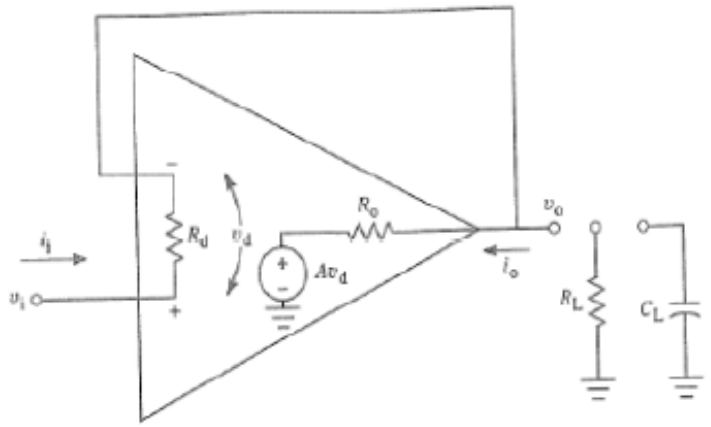
- It is good practice to install a dummy resistor R_p in series with the noninverting input such that $R_p = R$, ➔ $E_o(t) = \frac{1}{C}\int_0^t (-I_{OS})dt + E_o(0)$

Summary: To minimize the errors due to I_B and I_{OS}

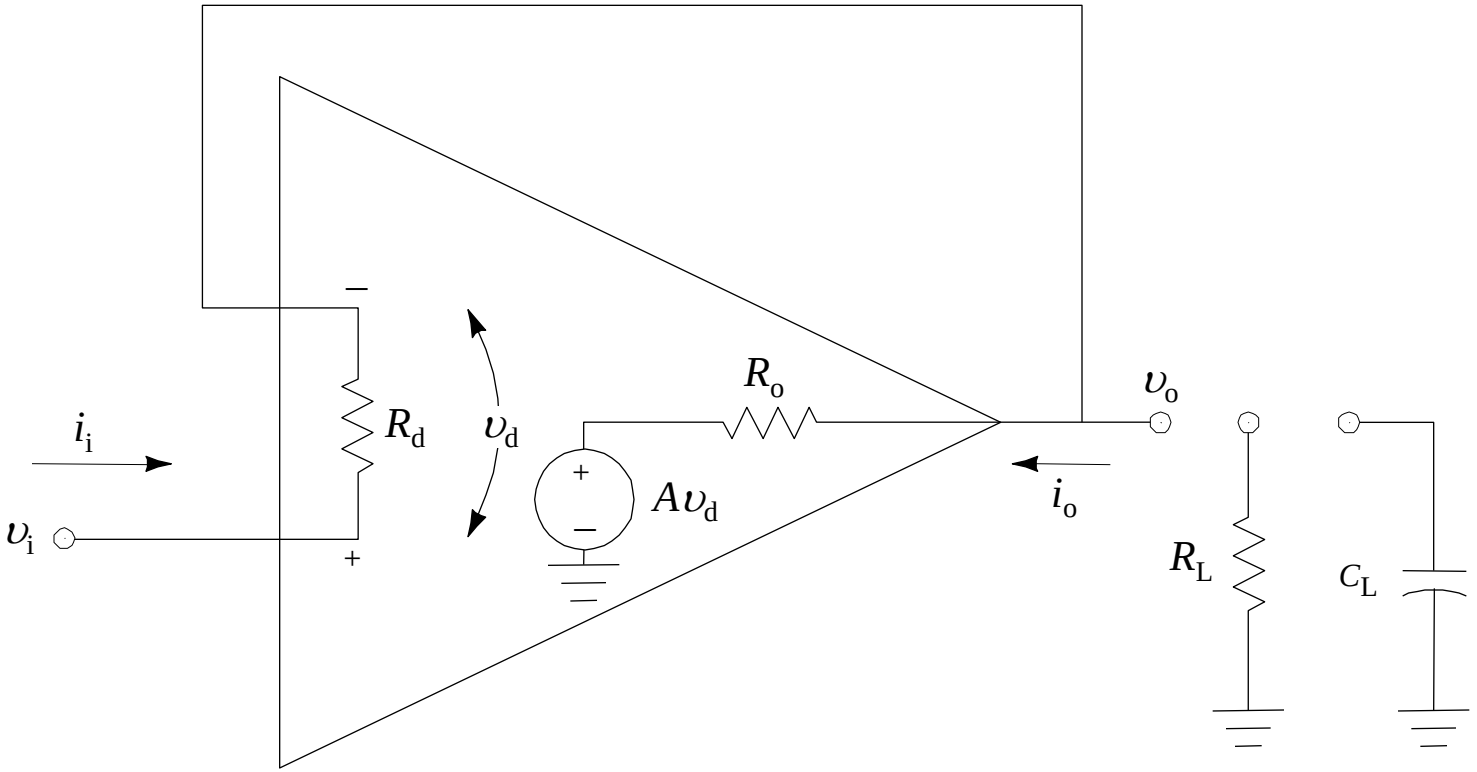
1. Using dummy resistor, R_p.
2. Keep resistance values as low as the application allows.
3. Select an op amp type with lower I_{OS}.

Non-ideal Characteristics

- Offset voltage
  - output not zero when the inputs to the amplifiers are equal
    - could be in order of millivolts
  - cancel offset voltage by adding an external "nulling" potentiometer
- Temperature Drift
  - offset voltage can drift by 0.1 microvolts over one degree variation
- Finite (lower than infinite) input impedance
  - can cause errors at input
- High output impedance
  - limits load driving capabilities
- Noise
  - Thermal noise or high-frequency noise
  - Flicker noise: low-frequency noise



3.14 Input and Output Resistance



$$R_{ai} = \frac{\Delta v_i}{\Delta i_i} = (A+1)R_d$$

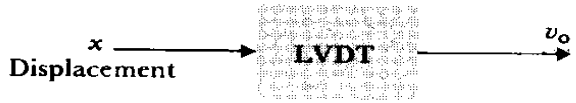
$$R_{ao} = \frac{\Delta v_o}{\Delta i_o} = \frac{R_o}{A+1}$$

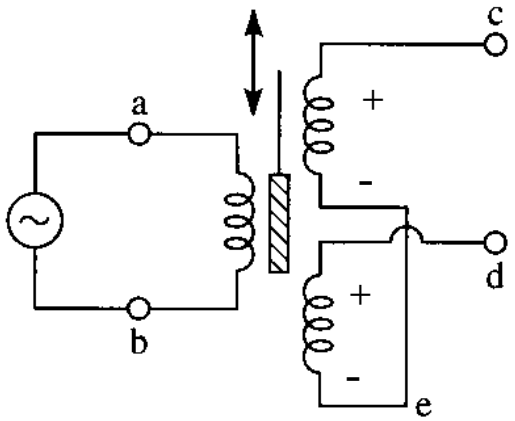
Typical value of R_d = 2 to 20 MΩ

Typical value of R_o = 40 Ω

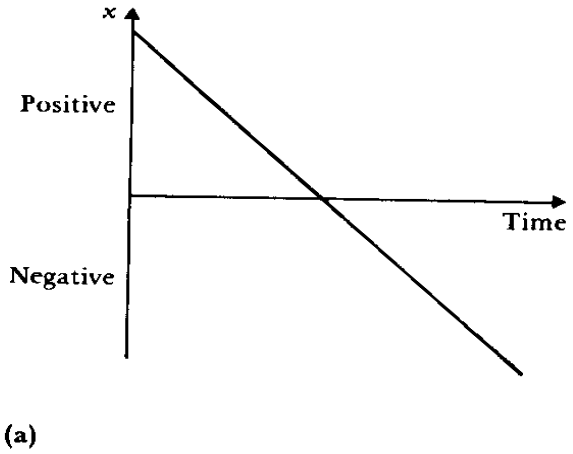
3.15 PHASE-SENSITIVE DEMODULATORS

Phase Modulator for Linear variable differential transformer LVDT

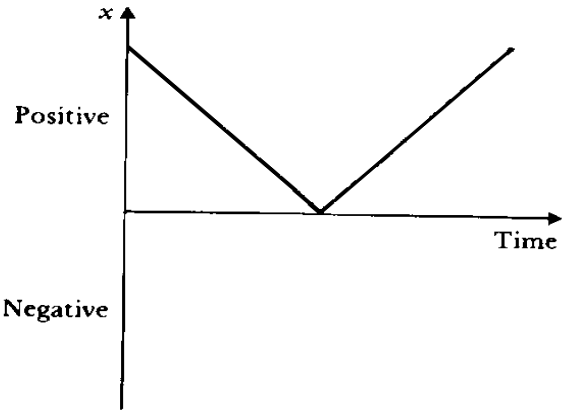




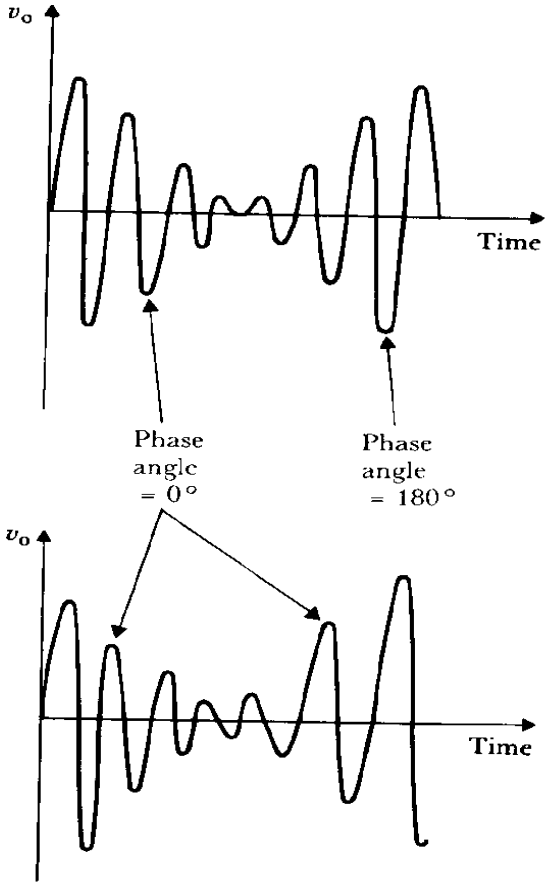
(c)



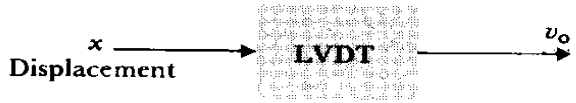
(a)

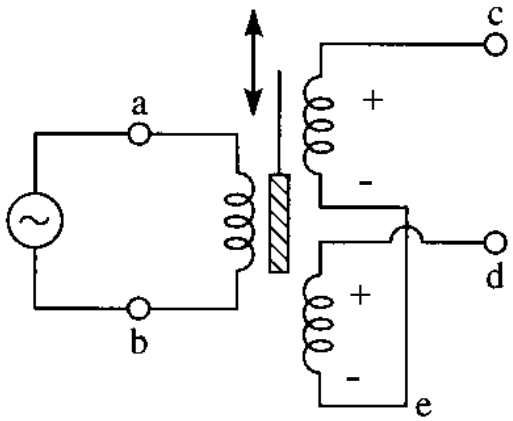


(b)

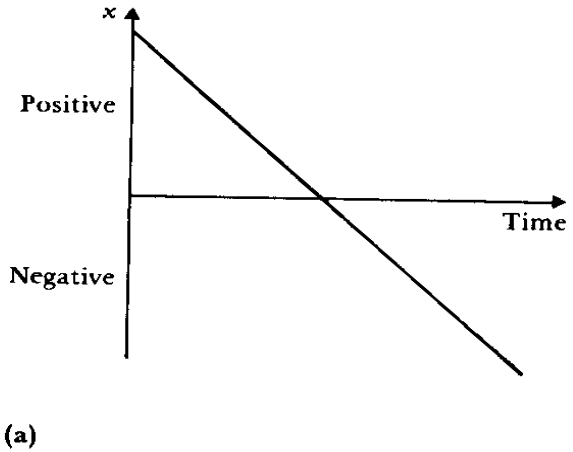


Phase Modulator for Linear variable differential transformer LVDT

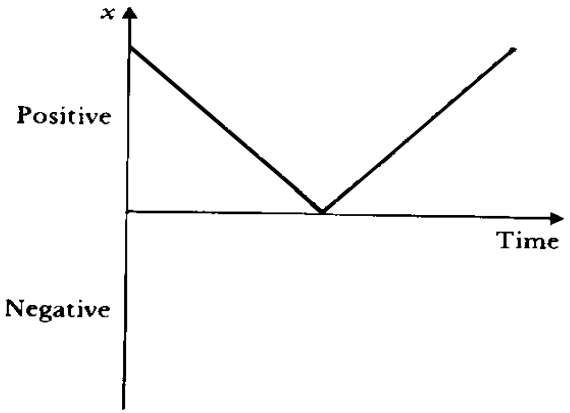




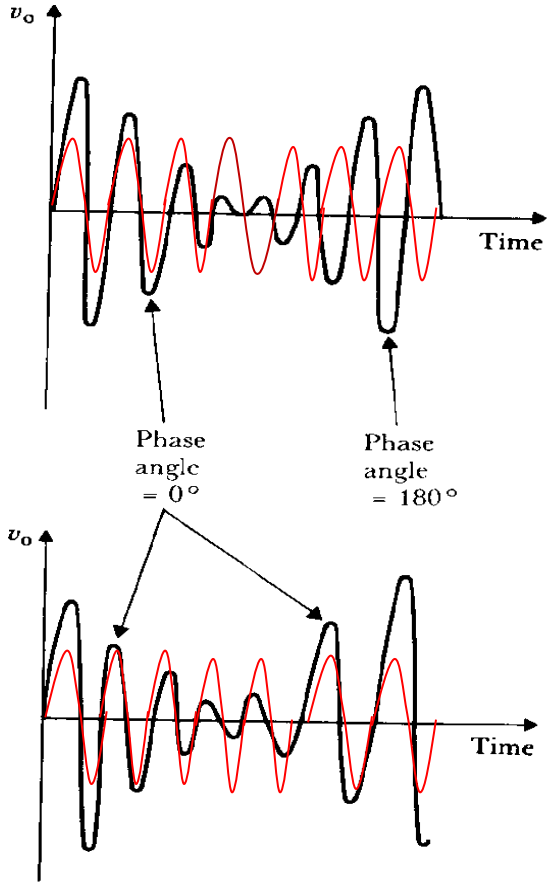
(c)



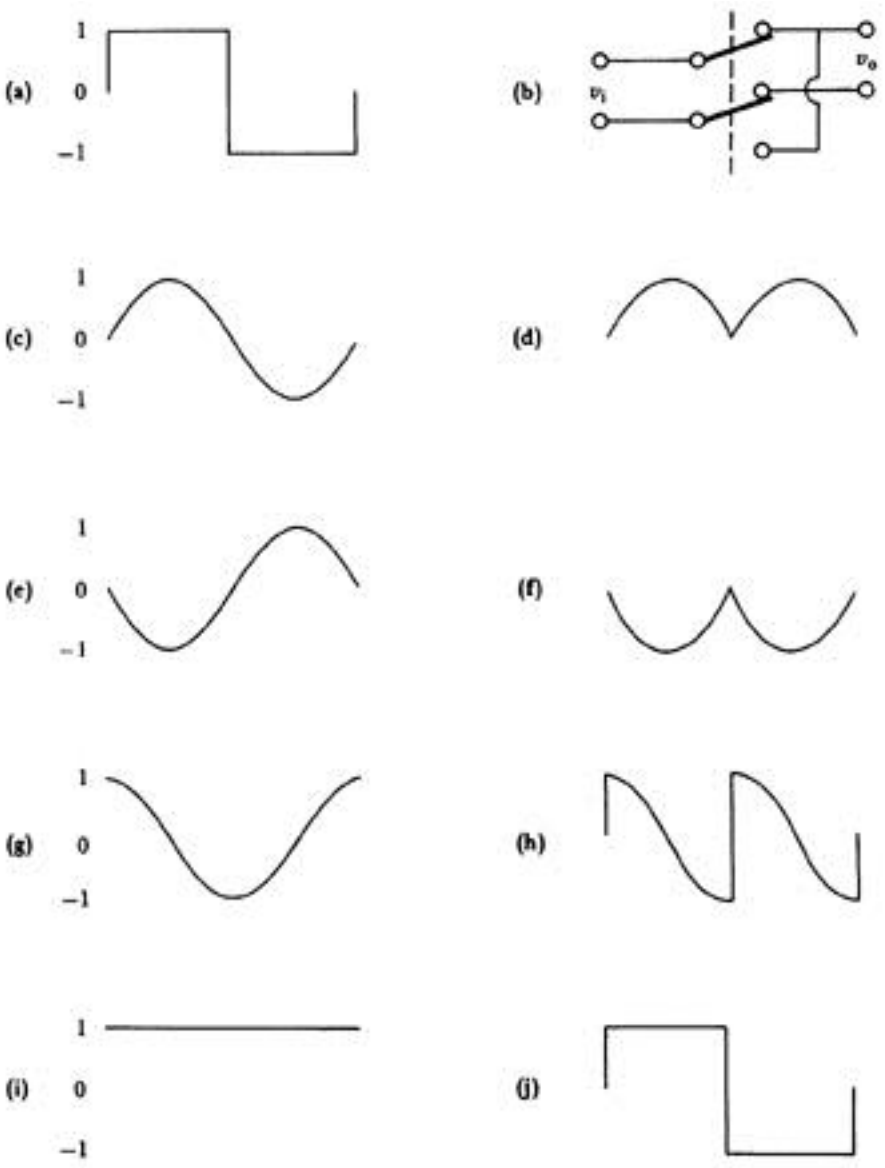
(a)



(b)



Phase-Sensitive Demodulator

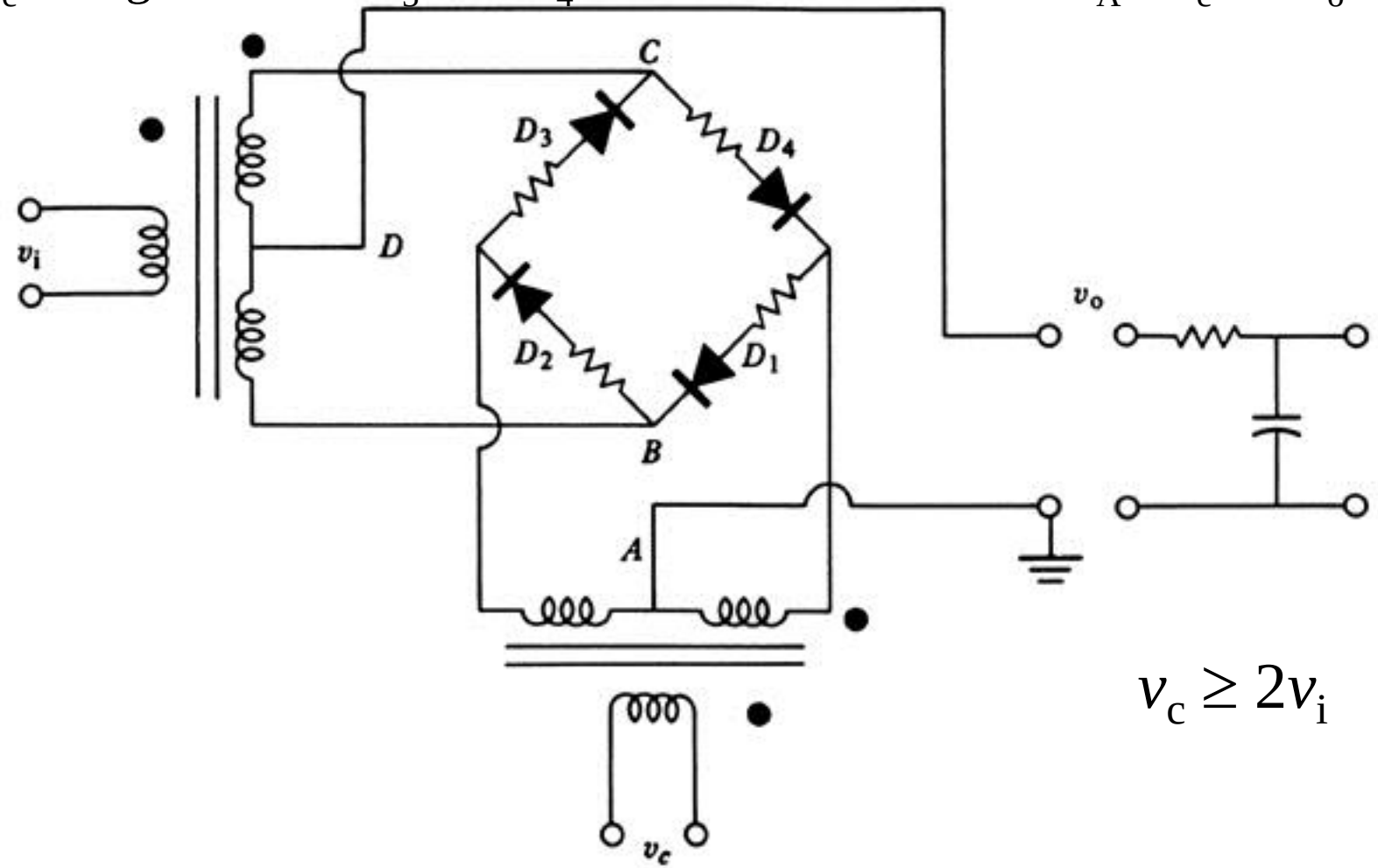


Used in many medical instruments for signal detection, averaging, and Noise rejection

The Ring Demodulator

If v_c is positive then D_1 and D_2 are forward-biased and $v_A = v_B$. So $v_o = v_{DB}$

If v_c is negative then D_3 and D_4 are forward-biased and $v_A = v_c$. So $v_o = v_{DC}$



$$v_c \geq 2v_i$$

Figure 3.17 A ring demodulator This phase-sensitive detector produces a full-wave-rectified output vo that is positive when the input voltage vi is in phase with the carrier voltage vc and negative when vi is 180o out of phase with vc.