Quiz CEA201 at FPTU

Computer Architecture (Trường Đại học FPT)

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01. Computer architecture refers to (Select all correct answers):

A. Design idea
B. Install specific hardware
C. The operational units in the computer and their interconnections
D. The attributes that have a direct impact on the logical execution of a program

02. Computer organization refers to (Select all correct answers):

A. Design idea
B. Install specific hardware
C. The operational units in the computer and their interconnections
D. The attributes that have a direct impact on the logical execution of a program

03. When considering whether a computer has a multiply instruction, we are referring to:

A. Computer organization
B. Computer architecture
C. Computer hardware
D. Computer software

04. When considering the memory technology used, we are referring to:

A. Computer hardware
B. Computer software
C. Computer organization
D. Computer architecture

05. Software compatibility, in point of view of the architecture, want to mention that:

A. Ability to use old software on new machines
B. Ability to use new software on old machines
C. Ability to use old software on new machines that belong to the same architecture as the old one
D. Ability to use new software on old machines that belong to the same architecture with new machines

06. Who are interested in computers with architectural look?

A. Application Programmer
B. System Programmer
C. HLL Programmers
D. All of the others

07. Who are interested in computers with organizational look?

A. Computer Designer
B. Compiler Designer
C. System Programmer
D. None of the others

08. - **Statement I**: Structure is the way in which the components are interrelated.
- **Statement II**: Function is the operation of each individual component as part of the structure.
Which of the above statements are true?

A. Statement I is true
B. Statement II is true
C. Both the statements are true
D. Both the statements are false

09. The basic functions of the computer:

A. Data storage, run programs, connect to peripherals, access memory
B. Data movement, control, execute instructions, data processing
C. Data storage, data movement, data processing, control
D. Control, data storage, perform calculations, connect to the internet

10. The basic components of the computer:

A. RAM, CPU, hard drive, system interconnection
B. Memory system, system interconnection, ROM, keyboard
C. Memory system, CPU, monitor, mouse
D. Memory system, CPU, I/O, system interconnection

11. The main structured components of a processor (Not including internal interconnection):

A. Control unit, registers, I/O ports
B. Control unit , ALU, registers
C. Registers, DACs, control unit
D. ALU, registers, I/O ports

12. The memory system of computers include:

A. Cache, external memory
B. External memory, ROM
C. Optical disc, internal memory
D. Internal memory, external memory

13. The computer input/output system do not include simultaneously the following devices:

A. ROM, RAM, registers
B. Monitor, RAM, printer
C. CPU, mouse, photo scanner
D. Magnetic discs, speakers, CD-ROM

14. A common example of system interconnection is by means of a ……., consisting of a number of conducting wires to which all the other components attach.

A. Address Bus
B. Data Bus
C. System Bus
D. Control Bus

15. In the computer, there are the following types of system interconnections:

A. Instruction, function, control
B. Control, data, address
C. Data, dependen, control
D. Data, control, auxiliary

01. Another word for the CPU is …

A. Executer
B. Microprocessor
C. Microchip
D. Decoder

02. Which was an early mainframe computer?

A. ENIAC
B. UNIC
C. BRAINIA
D. FUNTRIA

03. In the concept of "stored program", the computer fetches instructions from:

A. Memory
B. The opening/closing of electrical switches made by the operator
C. Hard disk
D. Program

04. The concept of "stored program" allows:

A. Many algorithms can be implemented inside the machine without having to rewiring
B. The program can be altered directly through the values stored in memory
C. Reduce time of program execution
D. All of the others

05. So far, computers have grown through:

A. 6 generations
B. 5 generations
C. 4 generations
D. 3 generations

06. During the development process of the computer, which of the following statements is true:

A. The first generation uses transistors
B. The third generation uses transistor
C. The first generation uses vacuum tube
D. The fourth generation uses SSI and MSI

07. During the development process of the computer, which of the following statements is false:

A. The second generation uses transistors
B. The third generation uses transistor
C. The first generation uses vacuum tube
D. The fourth generation uses integrated circuit

08. Circuit consisting of different electronic components and connections in them is called as:

A. Integrated circuit
B. Interrelated circuit
C. Inverting circuit
D. Reversing circuit

09. A silicon piece with a circuit on it is called:

A. Chip
B. Circuit
C. Logical gate
D. Circuit network

10. According to Moore's Law, the number of transistors will double after each:

A. 16 months
B. 18 months
C. 20 months
D. 22 months

11. Which parameters in a computer family are similar or identical? (Select all correct answers)

A. Instruction set
B. Operating system
C. Speed
D. Number of I/O ports

12. Which parameters in a computer family are increased from old to new machines?

A. Speed
B. Memory size
C. Cost
D. All of the others

13.The key factor/s in commercial success of a computer is/are ……. (Select all correct answers)

A. Performance
B. Cost
C. Speed
D. All of the others

14. The main objective of the computer system is:

A. To provide optimal power operation.
B. To provide best performance at low cost.
C. To provide speedy operation at low power consumption.
D. All of the others.

15. To continue to increase performance, what is the current processor development trend? (Select all correct answers)

A. Increasing clock rate
B. Increasing number of transistors on a single chip
C. Building a more complex processor
D. Multicore (placing multiple processors on the same chip)

01. The main structured components of a processor (not including internal interconnection):

A. Control unit, registers, I/O ports
B. Control unit , ALU, registers
C. Registers, DACs, control unit
D. ALU, registers, I/O ports

02. Hardware devices that are not part of the main computer system and are often added later to the system:

A. Peripheral
B. Clipart
C. Highlight
D. Execute

03. The device which is used to connect a peripheral to a bus is called:

A. Control Register
B. Interface
C. Communication Protocol
D. None of the others

04. The internal components of the processor are connected by …

A. Processor intra-connectivity circuitry
B. Processor bus
C. Memory bus
D. Rambus

05. The CPU of a computer takes instructions from memory and executes them. This process is called:

A. Load
B. Time Sequence
C. Execution
D. Fetch-Execute Cycle

06. A basic instruction that can be interpreted by computer has:

A. Operand and opcode
B. Decoder and Accumulator
C. Sequence register and decoder
D. None of the others

07. Instruction for computer should specify:

A. What operation to be performed
B. Where to fetch instructions and operands
C. Where to store results
D. All of the others

08. In which cycle the memory is read and the contents of memory at the address contained in the PC regtister are loaded into into IR?

A. Execution Cycle
B. Memory Cycle
C. Fetch Cycle
D. Decode Cycle

09. The decoded instruction is stored in …

A. IR
B. PC
C. Registers
D. MDR

10. If any instruction consists any arithmetic operation, data is transferred to:

A. Quantitative unit
B. Qualitative unit
C. Arithmetic and logical unit
D. Central processing unit

11. Interrupts can be generated in response to …

A. Detected program errors such as arithmetic overflow or division by zero
B. Detected hardware faults
C. Input/Output activities
D. All of the others

12. When the processor is executing the program, if there are interrupts (not prohibited) sent to it, then it:

A. Complete the program, then execute the interrupt
B. Interrupt rejection, not serving
C. Serve interrupts immediately, then execute the program
D. Complete the current instruction, then execute the interrupt, finally return to continue the program

13. Types of transfers are supported by a computer's interconnection structure:

A. Memory to memory, memory to or from processor, I/O to or from processor
B. Memory to or from processor, I/O to or from processor, I/O to or from memory
C. I/O to or from processor, I/O to I/O, memory to or from processor
D. None of the others

14. The main advantage of multiple bus organisation over single bus is:

A. Reduction in the number of cycles for execution
B. Increase in size of the registers
C. Better Connectivity
D. None of the others

15. …….. are used to over come the difference in data transfer speeds of various devices.

A. Speed enhancing circuitory
B. Bridge circuits
C. Multiple Buses
D. Buffer registers

Explanation: By using buffer registers, the processor sends the data to the I/O device at the processor speed and the data gets stored in the buffer. After that the data gets sent to or from the buffer to the devices at the device speed.

01. Cache memory refers to:

A. A cheap memory that can be plugged into the mother board to expand main memory
B. A fast memory that is used to store recently accessed data
C. A reserved portion of main memory used to save important data
D. A special area of memory on the chip that is used to save frequently used constants

02. The reason for the implementation of the cache memory is:

A. To increase the internal memory of the system
B. The difference in speeds of operation of the processor and memory
C. To reduce the memory access and cycle time
D. All of the others

03. The effectiveness of the cache memory is based on the property of …

A. Locality of reference
B. Memory localisation
C. Memory size
D. None of the others

Explanation: This means that the cache depends on the location in the memory that is referenced often.

04. The temporal aspect of the locality of reference means:

A. That the recently executed instruction wont be executed soon
B. That the recently executed instruction is temporarily not referenced
C. That the recently executed instruction will be executed soon again
D. None of the others

05. The spatial aspect of the locality of reference means:

A. That the recently executed instruction is executed again next
B. That the recently executed wont be executed again
C. That the instruction executed will be executed at a later time
D. That the instruction in close proximity of the instruction executed will be executed in future

Explanation: The spatial aspect of locality of reference tells that the nearby instruction is more likely to be executed in future.

06. An address in main memory is called:

A. Physical address
B. Logical address
C. Memory address
D. Word address

07. The cache bridges the speed gap between ……. and …….

A. RAM and ROM
B. RAM and Secondary memory
C. Processor and RAM
D. None of the others

Explanation: <numeric> The Cache is a hardware implementation to reduce the access time for processor operations.

08. The virtual memory bridges the size and speed gap between ……. and …….

A. RAM and ROM
B. RAM and Secondary memory
C. Processor and RAM
D. None of the others

Explanation: <numeric> The virtual memory basically works as an extension of the RAM.

09. To get the physical address from the logical address generated by CPU we use …….

A. MAR
B. MMU
C. Overlays
D. TLB

Explanation: Memory Management Unit, is used to add the offset to the logical address generated by the CPU to get the physical address.

10. The correspondence between the main memory blocks and the cache memory lines is given by …

A. Hash function
B. Mapping function
C. Locale function
D. Assign function

Explanation: The mapping function is used to map the contents of the memory to the cache.

11. The method of mapping the consecutive memory blocks to consecutive cache lines is called …….

A. Set associative
B. Associative
C. Direct
D. Indirect

Explanation: This method is most simple to implement as it involves direct mapping of memory blocks.

12. The method of mapping each block of main memory to any line of the cache is called …….

A. Set associative
B. Associative
C. Direct
D. Indirect

13. In direct mapping the presence of the block in memory is checked with the help of …... field.

A. Tag
B. Line
C. Block
D. Word

Explanation: The tag field is usd to check the presence of a mem block.

14. The algorithm to remove and place new contents into the cache is called …

A. Replacement algorithm
B. Renewal algorithm
C. Updation
D. None of the others

Explanation: As the cache gets full, older contents of the cache are swapped out with newer contents. This decision is taken by the algorithm.

15. The write-through procedure is used:

A. To write onto the memory directly
B. To write and read from memory simultaneously

C. To write directly on the memory and the cache simultaneously
D. None of the others
Explanation: When write operation is issued then the corresponding operation is performed.

01. What are the key properties of the semiconductor memory cell?

A. They exhibit two states, which can be represented by 0 or 1
B. They are capable of being written into to set the state
C. They can be read to sense the state
D. All of the others

02. With RAM, which of the following statements is true:

A. It is not volatile
B. DRAM is made from flip-flops
C. SRAM is made from capacitors
D. A place to store information that the computer is processing

03. With RAM, which of the following statements is false:

A. DRAM is made from flip-flops
B. DRAM is made from capacitors
C. SRAM is made from flip-flops
D. SRAM does not need to be refreshed

04. RAM is called DRAM (Dynamic RAM) when …

A. It is always moving around data
B. It requires periodic refreshing
C. It can do several things simultaneously
D. None of the others

05. DRAM is used for:

A. Internal memory
B. External Memory
C. Cache memory
D. Main memory

06. The standard SRAM chips are costly as …

A. They use highly advanced micro-electronic devices.
B. They house 6 transistor per chip.
C. They require specially designed PCB's.
D. None of the others

Explanation: As they require a large number of transistors, their cost per bit increases.

07. With the SRAM memory 64Kx4bit, which of the following statements is true:

A. The address lines are: A_0 -> A_{15}
B. The address lines are: D_0 -> D_{15}
C. The data lines are: A_0 -> A_3
D. The data lines are: D_0 -> D_8

08. With SRAM memory chips 16Kx8bit, which of the following statements is wrong:

A. There are 14 address lines
B. There are 8 data lines
C. The address lines are: A_0 – A_{13}
D. The address lines are: A_0 – A_{14}

09. SRAM is used for:

A. Main memory
B. Cache memory
B. Internal memory
C. External Memory

10. ROMs are used to ...

A. Record large size data, unchanged over time
B. Record small size data, updated regularly
C. Record the system subroutine
D. Contain the computer control program

11. Part of the operating system is usually stored in ROM so that it can be used to boot up the computer. ROM is used rather than RAM because:

A. ROM chips are faster than RAM
B. ROM chips are not volatile
C. ROM chips are cheaper than RAM chips
D. None of the others

12. With ROM, which of the following statements is true:

A. Can use electricity to erase PROM
B. PROM is a type of ROM that can be erased and recorded many times
C. EPROM is a type of ROM that can be erased and recorded many times
D. Can use electricity to erase EPROM

13. With ROM, which of the following statements is false:

A. There are all 5 types of ROMs
B. Can be use ultraviolet light to erase EPROM
C. EEPROM be written into without erasing prior contents
D. EPROM be written into without erasing prior contents

14. If the syndrome for the Hamming code contains one and only one bit set to 1:

A. No error has been detected
B. An error has occurred in one of the 4-check bits, and no correction is necessary
C. An error is occurred and the numerical value of the syndrome indicates the position of the data bit in error
D. None of the others

15. If the syndrome for the Hamming code contains more than one bit set to 1:

A. No error has been detected
B. An error has occurred in one of the 4-check bits, and no correction is necessary
C. An error is occurred and the numerical value of the syndrome indicates the position of the data bit in error
D. None of the others

16. The maximum addressing capacity of a microprocessor which uses 8 bit data & 16 bit address is

A. 64 KB
B. 4 GB
C. 16 MB
D. None of the others

17. An 16 bit address generates an address space of ……. locations

A. 1024
B. 65,356
C. 2 ^ 32
D. 16,777,216

Explanation: The number of addressable locations in the system is called as address space.

18. If a system is 32 bit machine, then the length of each word will be …….

A. 4 bytes
B. 8 bytes
C. 16 bytes
D. 12 bytes

Explanation: A 32 bit system means, that at a time 32 bit instruction can be executed.

19. A computer's memory is composed of 4K words of 64 bits each. How many total bits in memory?

A. 128000
B. 256000
C. 262144
D. 131072

20. In order to execute a program instructions must be transferred from memory along a bus to the CPU. If the bus has 8 data lines, at most one 8 bit byte can be transferred at a time. How many memory access would be needed in this case to transfer a 16 bit instruction from memory to the CPU.

A. 1
B. 2
C. 3
D. 4

01. If a magnetic disc drive has 100 cylinders, each containing 10 tracks of 10 sectors, and each sector can contain 128 bytes, what is the maximum capacity of the disc drive in KB?

A. 160,000
B. 1,280
C. 1,250
D. 1,280,000

02. According to the specifications of a particular hard disk, a seek time takes 0.3 milliseconds between adjacent tracks. If the disk has 100 cylinders how long will it take for the head to move from the innermost cylinder to the outermost cylinder.

A. 30 milliseconds
B. 300 microseconds
C. 3000 microseconds
D. 0.3 seconds

03. A computer that is advertised as having a 96K byte DRAM memory and a 2.1 Gigabyte hard drive has

A. 96K bytes of secondary memory and 2.1 Gigabytes of primary memory
B. 2.1 Gigabytes of auxiliary memory and 96 K bytes of primary memory
C. 96K bytes of cache, 2.1 Gigabytes of primary memory
D. 2.1 Gigabytes of auxiliary memory, 96 K bytes of primary memory and 96 bytes of cache

04. The average time required to reach a storage location in memory and obtain its contents is called the

A. Seek time
B. Turnaround time
C. Access time
D. Transfer time

05. The amount of time required to read a block of data from a disk into memory is composed of seek time, rotational latency, and transfer time. Rotational latency refers to

A. The time it takes for the platter to make a full rotation
B. The time it takes for the read-write head to move into position over the appropriate track
C. The time it takes for the platter to rotate the correct sector under the head
D. None of the others

06. The method of placing the heads and the discs in an air tight environment is called as ……..

A. RAID Arrays
B. ATP tech
C. Winchester technology
D. Fleming reduction

Explanation: <numeric> The Disks and the heads operate faster due to the absence of the dust particles.

07. Which of the following is a component of the disk system?

A. Disk
B. Disk drive
C. Disk controller
D. All of the others

08. If the drive has 20 surfaces, how many heads will it have?

A. 1
B. 5
C. 10
D. 20

Explanation: <numeric> Each surface will have its own head to perform read/write operation.

09. The ……. process divides the disk into sectors and tracks.

A. Creation
B. Initiation
C. Formatting
D. Modification

Explanation: <numeric> The formatting process deletes the data present and does the creation of sectors and tracks.

10. The data can be accessed from the disk using …….

A. Surface number
B. Sector number
C. Track number
D. All of the others

11. The …… is the minimum storage unit of a hard drive.

A. Track
B. Sector
C. Cluster
D. Cylinder

12. To distinguish between two sectors we make use of …….

A. Inter sector gap
B. Splitting bit
C. Numbering bit
D. None of the others

Explanation: <numeric> This means that we leave <để lại> a little gap between each sectors to differentiate between them.

13. …….. is used to deal with the difference in the transfer rates between the drive and the bus.

A. Data repeaters
B. Enhancers
C. Data buffers
D. None of the others

Explanation: <numeric> The buffers are added to store the data from the fast device and to send it to the slower device at its rate.

14. What common characteristics are shared by all RAID levels?

A. Set of physical disk drives viewed by the operating system as a single logical drive
B. Data are distributed across the physical drives of an array in a scheme known as striping
C. Redundant disk capacity is used to store parity information, which guarantees data recoverability in case of a disk failure
D. All of the others

15. The solution to the problem of reliability is the introduction of …….

A. Aging
B. Scheduling
C. Redundancy
D. Disks

16. RAID splits file(s) into many segments, and sends the segments to several disks. Files that have been segmented in this way are called:

A. Striped File
B. Striped Data
C. Striped Array
D. None of the others

17. Which of the following is the RAID level no redundant?

A. 0
B. 1

C. 2 D. 3

18. Which of the following is the RAID level refers to memory-style ECC organization?

A. 1 B. 2
C. 3 D. 4

19. Which of the following is the RAID level distributes parity and data across all the disks?

A. 3 B. 4
C. 5 D. 6

20. RAID level 1+0 is used because RAID level 1 provides ……. whereas RAID level 0 provides …….

A. Performance, Redundancy B. Performance, Reliability
C. Redundancy, Performance D. Reliability, Performance

01. ……. register keeps tracks of the instructions stored in program stored in memory.

A. AR (Address Register) B. XR (Index Register)
C. PC (Program Counter) D. AC (Accumulator)

02. An interface that provides a method for transferring binary information between internal storage and external devices is called as …

A. I/O interface B. Input interface
C. Output interface D. I/O bus

03. An interface that provides I/O transfer of data directly to or form the memory unit and peripheral is termed as …

A. DDA B. Serial interface
C. BR D. DMA

04. External, or peripheral, devices include:

A. Human readable B. Machine readable
C. Communication D. All of the others

05. With the functions of an I/O module, which of the following statements is false:

A. Control and timing
B. A module only connects to a peripheral device
C. Exchange information with the processor, with peripherals
D. Data buffers, error detection

06. I/O addressing methods:

A. Memory-mapped I/O
B. Isolated I/O
C. Both memory-mapped I/O and isolated I/O
D. None of the others

07. In memory-mapped I/O…

A. The I/O devices and the memory share the same address space
B. The I/O devices have a seperate address space
C. The memory and I/O devices have an associated address space
D. A part of the memory is specifically set aside for the I/O operation

Explanation: It's the different modes of accessing the i/o devices.

08. With isolated I/O, ...

A. The I/O devices and the memory share the same address space

B. The I/O devices have a seperate address space
C. The memory and I/O devices have an associated address space
D. A part of the memory is specifically set aside for the I/O operation

Explanation: It's the different modes of accessing the i/o devices.

09. There are three methods for performing I/O:

A. Interrupt-driven I/O, System-driven I/O, DMA
B. Interrupt-driven I/O, System-driven I/O, Programmed I/O
C. Programmed I/O, Interrupt-driven I/O, DMA
D. Programmed I/O, System-driven I/O, DMA

10. The method of accessing the I/O devices by repeatedly checking the status flags is …

A. Programmed I/O
B. Memory-mapped I/O
C. I/O mapped
D. None of the others

Explanation: In this method the processor constantly checks the status flags , and when it finds that the flag is set it performs the appropriate operation.

11. The method of synchronising the processor with the I/O device in which the device sends a signal when it is ready is …

A. Exceptions
B. Signal handling
C. Interrupt-driven I/O
D. DMA

Explanation: This is a method of accessing the I/O devices which gives the complete power to the devices, enabling them to intimate the processor when they're ready for transfer.

12. The process where in the processor constantly checks the status flags is called as …

A. Polling
B. Inspection
C. Reviewing
D. Echoing

13. With Programmed I/O, which of the following statements is false:

A. Use input/output commands in the program to exchange data with the I/O ports
B. Peripherals are active objects in data exchange
C. When executing the program, encountering input/output commands, the CPU controls data exchange with peripherals
D. Peripherals are passive objects in data exchange

14. With Programmed I/O, which of the following statements is true:

A. This is the simplest method to exchange data
B. This is the fastest method to data exchange
C. Complex circuit design
D. None of the others

15. With Interrupt-driven I/O, which of the following statements is false:

A. Peripherals are the active object in data exchange
B. CPU does not have to wait for the availability of peripherals
C. CPU have to wait for the availability of I/O module
D. I/O module interrupt CPU when it is in ready state

16. With Interrupt-driven I/O, which of the following statements is true:

A. Peripherals are the active object in data exchange
B. The method is fully processed by hardware
C. CPU is an active object in data exchange

D. The method is fully processed by software

17. The DMA differs from the interrupt mode by …

A. The involvement of the processor for the operation
B. The method accessing the I/O devices
C. The amount of data transfer possible
D. Both the involvement of the processor for the operation and the amount of data transfer possible

Explanation: DMA is an approach of performing data transfers in bulk between memory and the external device without the intervention of the processor.

18. The DMA transfers are performed by a control circuit called as …

A. Device interface
B. DMA controller
C. Data controller
D. Overlooker

Explanation: The Controller performs the functions that would normally be carried out by the processor.

19. In DMA transfers, the required signals and addresses are given by the …

A. Processor
B. Device drivers
C. DMA controller
D. The program itself

Explanation: The DMA controller acts like a processor for DMA transfers and overlooks <bỏ qua> the entire process.

20. The technique whereby the DMA controller steals the access cycles of the processor to operate is called as …

A. Fast conning
B. Memory Con
C. Cycle stealing
D. Memory stealing

Explanation: The controller takes over the processor's access cycles and performs memory operations.

01. The operating system is an example of a computer …….

A. Object
B. File system
C. Program
D. Desktop

02. Which of the following is the primary purpose of an operating system?

A. To make the most efficient use of the computer hardware
B. To allow people to use the computer
C. To keep systems programmers employed
D. To make computers easier to use

03. The key services provided by an OS:

A. Create and execute programs
B. Control access to I/O devices, files and system resources
C. Accounting, error detection and response
D. All of the others

04. One of the function of operating system is it serves an interface between user and …….

A. Software
B. Hardware
C. Utilities
D. Data ware

05. In an ……. system the user/programmer interacts directly with the computer, usually through a keyboard/display terminal to request the execution of a job or to perform a transaction.

A. Batch
B. Multiprogramming
C. Interactive
D. None of the others

06. Which of the following is NOT a function of operating system?

A. Resource Manager
B. Storage Manager
C. Process Manager
D. Software Manager

07. Long-term scheduling is:

A. The decision to add which programs to the system for processes
B. The decision to add to the number of processes that are partially or fully in main memory
C. The decision as to which available process will be executed by the processor.
D. The decision as to which process's pending I/O request shall be handled by an available I/O device.

08. Medium-term scheduling is:

A. The decision as to which process's pending I/O request shall be handled by an available I/O device.
B. The decision as to which available process will be executed by the processor.
C. The decision to add to the number of processes that are partially or fully in main memory
D. The decision to add which programs to the system for processes

09. Short-term scheduling is:

A. The decision to add which programs to the system for processes
B. The decision as to which available process will be executed by the processor.
C. The decision to add to the number of processes that are partially or fully in main memory
D. The decision as to which process's pending I/O request shall be handled by an available I/O device.

10. What is a process?

A. A program in execution
B. A *.exe file
C. A executable file stored in external memory
D. None of the others

11. What is the purpose of the process?

A. Multiprocessing
B. Multiprogramming
C. Multicore
D. All of the others

12. In the process state transition diagram, which state corresponding to a program is admitted by the Long-term scheduler?

A. New
B. Ready
C. Running
D. Halted

13. In the process state transition diagram, ... will initialize the process, moving it to the ready state.

A. Long-term scheduler
B. Medium-term scheduler
C. Short-term scheduler
D. None of the others

14. In the process state transition diagram, the transition from the READY state to the RUNNING state indicates that:

A. A process was preempted by another process
B. A process has blocked for a semaphore or other operation
C. A process is done waiting for an I/O operation
D. A process was just created

15. The state corresponding to the process has terminated and will be destroyed by the OS is called:

A. New
B. Ready

C. Running
D. Halted

16. Copying a process from memory to disk to allow space for other processes is called?

A. Page Fault
B. Deadlock
C. Demand Paging
D. Swapping

17. The purpose of swapping is:

A. To remove processes not in a ready state
B. To provide for efficient use of main memory for processes execution
C. To add processes in a ready state to main memory
D. None of the others

18. Swapping is executed by .....

A. Long-term scheduler
B. Medium-term scheduler
C. Short-term scheduler
D. None of the others

19. If a process may be dynamically assigned to different locations in main memory, what is implication for the addressing mechanism?

A. The addressing mechanism must keep track of the physical addresses of the process
B. The addressing mechanism must keep track of the logical addresses used for swapping out the process
C. The addressing mechanism must keep track of the physical addresses of the process, as well as the logical addresses used for swapping out the process
D. None of the others

20. The purpose of a TLB is:

A. To cache page translation information
B. To cache frequently used data
C. To hold register values while a process is waiting to be run
D. To hold the start and length of the page table

01. The _____ approach is essentially the ability to execute instructions independently and simultaneously in different pipelines.

A. Scalar
B. Branch
C. Superscalar
D. Flow dependency

02. Which of the following is a situation which parallel executions can not apply?

A. Procedural dependency
B. Resource conflicts
C. Anti-dependency
D. All of the others

03. The situation in which the second instruction needs data produced by the first instruction to execute is referred to as _____.

A. True data dependency
B. Output dependency
C. Procedural dependency
D. Anti-dependency

04. The instructions following a branch have a _____ on the branch and cannot be executed until the branch is executed.

A. Anti-dependency
B. Procedural dependency
C. Output dependency
D. True data dependency

05. _____ refers to the process of initiating instruction execution in the processor's functional units.

A. Instruction issue
B. In-order issue
C. Out-of-order issue
D. Procedural issue

06. Instead of the first instruction producing a value that the second instruction uses, with _____ the second instruction destroys a value that the first instruction uses.

A. In-order issue
B. Resource conflict
C. Anti-dependency
D. Out-of-order completion

07. _____ exists when instructions in a sequence are independent and thus can be executed in parallel by overlapping.

A. Flow dependency
B. Instruction-level parallelism
C. Machine parallelism
D. Instruction issue

08. _____ is determined by the number of instructions that can be fetched and executed at the same time and by the speed and sophistication of the mechanisms that the processor uses to find independent instructions.

A. Machine parallelism
B. Instruction-level parallelism
C. Output dependency
D. Procedural dependency

09. Which of the following is a hardware technique that can be used in a superscalar processor to enhance performance?

A. Duplication of resources
B. Out-of-order issue
C. Renaming registers
D. All of the others

10. - Statement I : Register renaming eliminates anti-dependencies and output dependencies.
- Statement II : Out-of-order completion requires more complex instruction issue logic than in-order completion.
Which of the above statements are true?

A. Both the statements are true
B. Statement I is true
C. Statement II is true
D. Both the statements are false

11. Uniprocessors fit into which category of computer systems?

A. MIMD
B. SIMD
C. SISD
D. MISD

12. Vector and array processors fit into which category of computer systems?

A. MIMD
B. SIMD
C. SISD
D. MISD

13. Symmetric multiprocessors (SMPs) fall into which category of computer systems?

A. MIMD
B. SIMD
C. SISD
D. MISD

14. In an SMP computer, the largest disadvantage of the bus organization is _____.

A. Reliability
B. Performance
C. Cache coherence
D. All of the others

15. A cache coherence problems can occur when _____.

A. A word is altered in one cache
B. Processors are allowed to update their own copies
C. Processors are allowed to update their own copies freely
D. None of the others

16. - Statement I : The cache coherence problem is typically addressed in hardware.
- Statement II : Snoopy protocols are suitable for a bus-based multiprocessor.
Which of the above statements are true?

A. Both the statements are true
B. Statement I is true
C. Statement II is true
D. Both the statements are false

17. A _____ is an instance of a program running on a computer.

A. Thread
B. Multithreading
C. Process
D. SMT

18. With _____ the instruction stream is divided into several smaller streams, known as threads, such that the threads can be executed in parallel.

A. Process switch
B. Multithreading
C. Thread
D. Process

19. With _____ instructions are simultaneously issued from multiple threads to the execution units of a superscalar processor.

A. SMT
B. Single-threaded scalar
C. Coarse-grained multithreading
D. Chip multiprocessing

20. Replicating the entire processor on a single chip with each processor handling separate threads is _____.

A. Interleaved multithreading
B. Blocked multithreading
C. Simultaneous multithreading
D. Chip multiprocessing

01. Which representation is most efficient to perform arithmetic operations on the numbers?

A. Sign-magnitude
B. 1's complement
C. 2's complement
D. None of the others

02. When we perform the addition on -7 and 1 the answer in 2's complement form is _____.

A. 1010
B. 1110
C. 0110
D. 1000

03. When we perform the multiplication on 110101 and 1111 the result of the operation is _____.

A. 1100011011
B. 1100111011
C. 1101001011
D. 1101011011

04. When 1101 is used to divide 1110110 the remainder is _____ .

A. 0
B. 1
C. 10
D. 100

05. _____ registers enable the machine or assembly language programmer to minimize main memory references by optimizing use of registers.

A. General purpose
B. Control and status
C. User-visible
D. None of the others

06. Which register of the following connects to the address bus directly?

A. PC
B. MAR
C. MBR
D. None of the others

07. Addressing mode used in instruction SUB r1, r2 is _____.

A. Immediate
B. Indirect
C. Base
D. Register

08. In immediate addressing mode the operand is placed _____.

A. In the CPU register

B. After OP code in the instruction
C. In memory
D. In stack

09. How many address lines are needed to address each memory location in a 2048 X 4 memory chip?

A. 10 B. 11
C. 8 D. 12

10. A processor performing fetch or decoding of different instruction during the execution of another instruction is called _____ .

A. Super-scaling B. Pipe-lining
C. Parallel Computation D. None of the others

Explanation: Pipe-lining is the process of improving the performance of the system by processing different instructions at the same time, with only one instruction performing one specific operation.

11. The periods of time when the pipeline, or some portion of the pipeline, is idle is called as _____.

A. Hazards B. Stalls
C. Bubbles D. Stalls or Bubbles

Explanation: <numeric> The stalls are a type of hazards that affect a pipelined system.

12. Which computer architecture aimed at reducing the number of instructions per program?

A. CISC B. RISC
C. ISA D. ANNA

13. Which computer architecture aimed at reducing the time of execution of instructions?

A. ANNA B. RISC
C. CISC D. ISA

Explanation: <numeric> The Risc machine aims at reducing the instruction set of the computer.

14. Which computer architecture was the first to implement pipe-lining?

A. ISA B. CISC
C. RISC D. ANNA

Explanation: <numeric> The RISC machine architecture was the first to implement pipe-lining.

15. The Sun microsystems processors usually follow _____ architecture.

A. CISC B. ISA
C. ULTRA SPARC D. RISC

16. Which of the following is typical distinguishing characteristics of RISC organization?

A. A limited instruction set with a fixed format
B. A large number of registers or the use of a compiler that optimizer register usage
C. An emphasis on optimizing the instruction pipeline
D. All of the others

17. Both CISC and RISC architectures have been developed to minimize what?

A. Cost B. Time delay
C. Semantic gap D. All of the others

18. - Statement I : The major cost in the life cycle of a system is hardware.
- Statement II : Almost all RISC instructions use simple register addressing. Which of the above statements are true?

A. Both the statements are true
B. Statement I is true
C. Statement II is true
D. Both the statements are false

19. _____ is a way of increasing the efficiency of the pipeline by making use of a branch that does not take effect until after execution of the following instruction.

A. Delayed branch
B. Delayed load
C. Unrolling
D. None of the others

20. _____ can improve performance by reducing loop overhead, increasing instruction parallelism by improving pipeline performance, and improving register, data cache, or TLB locality.

A. Delayed branch
B. Delayed load
C. Unrolling
D. None of the others

21. _____ is the fastest available storage device.

A. Main memory
B. Cache
C. Register storage
D. HLLs

22. The essence of the _____ approach is the ability to execute instructions independently and concurrently in different pipelines.

A. Scalar
B. Branch
C. Superscalar
D. Flow dependency

23. Which of the following is a fundamental limitation to parallelism with which the system must cope?

A. Procedural dependency
B. Resource conflicts
C. Anti-dependency
D. All of the others

24. The situation where the second instruction needs data produced by the first instruction to execute is referred to as _____.

A. True data dependency
B. Output dependency
C. Procedural dependency
D. Anti-dependency

25. The instructions following a branch have a _____ on the branch and cannot be executed until the branch is executed.

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B. Procedural dependency
C. Output dependency
D. True data dependency

26. _____ refers to the process of initiating instruction execution in the processor's functional units.

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C. Anti-dependency
D. Out-of-order completion

28. _____ exists when instructions in a sequence are independent and thus can be executed in parallel by overlapping.

A. Flow dependency
B. Instruction-level parallelism
C. Machine parallelism
D. Instruction issue

29. _____ is determined by the number of instructions that can be fetched and executed at the same time and by the speed and sophistication of the mechanisms that the processor uses to find independent instructions.

A. Machine parallelism
B. Instruction-level parallelism
C. Output dependency
D. Procedural dependency

30. Which of the following is a hardware technique that can be used in a superscalar processor to enhance performance?

A. duplication of resources
B. out-of-order issue
C. renaming
D. all of the others

01. Microprocessors that are used for one particular job are classified as

A. Dedicated microprocessors
B. Dedicated computers
C. Dedicated microcomputers
D. Dedicated mega computers

02. At the integrated circuit level, what are the three principal constituents of a computer system?

A. Wafers, chips, and interconnections among them
B. Chips, memory cells, and interconnections among them
C. Gates, memory cells, and interconnections among them
D. None of the others

03. CISC stands for ...

A. Complete Instruction Sequential Compilation
B. Computer Integrated Sequential Compiler
C. Complex Instruction Set Computer
D. Complex Instruction Sequential Compilation

04. Which types of programmers should be aware of instruction set architecture? (Select all correct answers)

A. Application Programmer
B. System Programmer
C. Compiler Designer
D. HLL Programmers

05. Compact discs, (according to the original CD specifications) hold how many minutes of music?

A. 74 mins
B. 56 mins
C. 60 mins
D. 90 mins

06. During the execution of a program which gets initialized first?

A. MBR
B. IR
C. PC
D. MAR

07. The fetch and execution cycles are interleaved with the help of …

A. Modification in processor architecture
B. Clock
C. Special unit
D. Control unit

08. Any computer must at least consist of:

A. Data bus
B. Address bus
C. Control bus
D. All of the others

09. The main virtue <ưu điểm, tính hấp dẫn, …> **for using single bus structure is:**

A. Fast data transfers
B. Cost effective connectivity and speed
C. Cost effective connectivity and ease of attaching peripheral devices
D. None of the others

Explanation: By using single BUS structure we can minimize the amount hardware (wire) required and thereby reducing the cost.

10. To extend the connectivity of the processor bus we use …

A. PCI bus
B. SCSI bus
C. Controllers
D. Multiple bus

Explanation: PCI bus is used to connect other **peripheral devices** which require **a direct connection** with the processor.

11. PCI stands for …

A. Peripheral Component Interconnect
B. Peripheral Computer Interconnect
C. Peripheral Component In circuit
D. None of the others

12. Memory system of computers includes:

A. Cache, External Memory
B. External Memory, ROM
C. Optical Disk, Internal Memory
D. Internal Memory, External Memory

13. The fastest data access is provided using …

A. Cache memory
B. DRAM
C. SRAM
D. Registers

Explanation: The fastest data access is provided using registers as these memory locations are situated inside the processor.

14. The last on the hierarchy scale of memory devices is …

A. Cache memory
B. Secondary memory
C. Registers
D. RAM

Explanation: The secondary memory is the slowest memory device.

15. A memory management technique used to improve computer performance is:

A. Selecting memory chips based on their cost
B. Storing as much data as possible on disk
C. Using the cache to store data that will most likely be needed soon
D. Preventing data from being moved from the cache to primary memory

16. The technique of searching for a block by going through all the tags is ……

A. Linear search
B. Binary search
C. Associative search
D. None of the others

17. What is a Flash memory?

A. Is intermediate between EPROM and EEPROM
B. Uses an electrical erasing technology
C. Does not provide byte-level erasure
D. All of the others

18. Which of the following is non-volatile memory?

A. SRAM
B. EEPROM
C. DRAM
D. None of the others

19. A computer's memory is composed of 8K words of 32 bits each. How many bits are required for memory address if the smallest addressable memory unit is a word?

A. 13
B. 8
C. 10
D. 6

20. The digital information is stored on the hard disk by …….

A. Applying a suitable electric pulse.
B. Applying a suitable magnetic field.
C. Applying a suitable nuclear field.
D. By using optic waves.

Explanation: <numeric> The digital data is sorted on the magnetized discs by magnetizing <sự từ hóa> the areas.

21. For the synchronization of the read head, we make use of a …….

A. Framing bit
B. Synchronization bit
C. Clock
D. Dirty bit

Explanation: <numeric> The clock makes it easy to distinguish between different values red by head.

22. The set of corresponding tracks on all surfaces of a stack of disks form a …….

A. Cluster
B. Cylinder
C. Group
D. Set

Explanation: <numeric> The data is stored in the these sections called as cylinders.

23. The data can be accessed from the disk using …….

A. Surface number
B. Sector number
C. Track number
D. All of the others

24. ……. is used to detect and correct the errors that may occur during data transfers.

A. ECC
B. CRC
C. Checksum
D. None of the others

Explanation: <numeric> ECC stands for Error Correcting Code.

25. RAID level ……. refers to disk arrays with striping but without any redundancy.

A. 0
B. 1
C. 2
D. 3

26. RAID level …….. consists of byte-level striping with dedicated parity.

A. 0
B. 1
C. 2
D. 3

27. RAID level …….. is also known as block-interleaved parity organisation and uses block-level striping and keeps a parity block on a seperate disk.

A. 1
B. 2
C. 3
D. 4

28. RAID level 5 is also known as :

A. Bit-interleaved parity organization
B. Block-interleaved parity organization
C. Block-interleaved distributed parity
D. Memory-style ECC organization

29. It is the represented abbreviations of an Opcode which also indicates the operation.

A. Control
B. Mnemonics
C. Increment
D. Logical

30. It is the bitwise operation and also includes AND, OR and NOT, XOR, and XNOR gates.

A. Operands
B. Arithmetic
C. Characters
D. Logical

31. This is the common form of data which is text or character strings.

A. Addresses
B. Numbers
C. Characters
D. Conversion

32. It's all about the instruction length (in bits), number of addresses, size of various fields, and so on.

A. Operation Repertoire
B. Instruction Format
C. Opcodes
D. Logic Instructions

33. It is a collection of different instructions that the processor can execute, it also provides the commands to the processor, to tell it what it needs to do.

A. Instruction Set
B. Operation Code
C. Immediate
D. Processor Register

34. The one which is inputted in an operation and are also represented symbolically.

A. Numbers
B. Absolute
C. Mnemonics
D. Operands

35. It's an operation that adds 1 to the operand.

A. Increment
B. Negate
C. Decrement
D. Registers

36. Which category of microprocessor instructions detect the status conditions in registers and accordingly exhibit the variations in program sequence on the basis of detected results?

A. Transfer Instructions
B. Operation Instructions
C. Control Instructions
D. All of the others

37. The push and pop instructions belonging to the category of transfer instructions of microprocessor perform data transformation between _____.

A. Two registers
B. Processor register and memory stack
C. Processor register and interface register
D. Interface register and memory word

38. The addressing mode, which uses the PC instead of a general purpose register is _____

A. Indexed with offset
B. Relative
C. Direct
D. Both Indexed with offset And Direct

Explanation: In this the contents of the PC are directly incremented.

39. The addressing mode, where you directly specify the operand value is _____ .

A. Immediate
B. Direct
C. Definite
D. Relative

40. The addressing mode which makes use of in-direction pointers is _____

A. Indirect addressing mode
B. Index addressing mode
C. Relative addressing mode
D. Offset addressing mode

Explanation: In this addressing mode, the value of the register serves as another memory location and hence we use pointers to get the data.

41. Which addressing mode execute its instructions within CPU without the necessity of reference memory for operands?

A. Implied Mode
B. Immediate Mode
C. Direct Mode
D. Register Mode

42. Which register holds the address for a stack whose value is supposed to be directed at the topmost position?

A. Stack Pointer
B. Stack Register
C. Both Stack Pointer & Stack Register
D. None of the others

43. What is another name of memory stack especially given for the fundamental function performed by it?

A. Last-in-first-out (LIFO)
B. First-in-last-out (FILO)
C. First-in-first-out (FIFO)
D. Last-in-last-out (LILO)

44. What does the last instruction of each subroutine that transfer the control to the instruction in the calling program with temporary address storage , called as?

A. Jump to subroutine
B. Branch to subroutine
C. Return from subroutine
D. Call subroutine

45. _____ converts the programs written in assembly language into machine instructions

A. Machine compiler
B. Interpreter
C. Assembler
D. Converter

Explanation: The assembler is a software used to convert the programs into machine instructions.

46. Programs written in assembly language

A. Are not portable
B. Make use of mnemonics
C. Run faster and require less storage space than those written in HLLs
D. All of the others

47. In the Assembly Language instruction LDA X

A. LDA is the opcode and X is the operand
B. LDA is the operand and X is the opcode
C. LDA is a symbolic address
D. X is a direct address

48. Consider the program segment:

Age DB 100
MOV Age,123

What is the memory-addressing mode of the first operand in the MOV instruction?

A. Immediate addressing mode
B. direct addressing mode
C. Indirect addressing mode
D. None of the others

49. The instruction DEC N inform the assembler to

A. Decrement the content of N
B. Decrement the data addressed by N
C. Convert signed decimal number to binary
D. None of the others

50. The assembler stores the object code in _____

A. Main memory
B. Cache
C. RAM
D. Magnetic disk

Explanation: After compiling the object code, the assembler stores it in the magnetic disk and waits for further execution.

01. Which of the following has a variable ability to conduct electricity depending on conditions?

A. Conductor
B. Insulator
C. Semiconductor
D. None of the others

The semiconductive material silicon is used to make most microchips because changes in conditions (such as current and voltage) can be used to control how conductive of electrons it is at a given moment, allowing controlled flow of electricity.

02. Which of the following is the fundamental conceptual unit in a computer?

A. CPU
B. Hard Drive
C. Operating System
D. Transistor

03. There's a concept that states: the number of transistors that manufacturers can pack into a chip of the same size doubles every years. What is it called?

A. Godwin's Law
B. Moore's Law
C. Fermat's Last Theorem
D. None of the others

More of an estimate that has held somewhat true than a law, the idea was first put forth in 1965 by Gordon E. Moore, co-founder of Intel, who at first predicted the number would double every year. The term is still used in computing circles, but the time frame gets revised periodically.

04. What does a transistor do?

A. Stores electricity
B. Acts as a switch to control the flow of electric current
C. Reduces the flow of electric current
D. All of the others

A processor contains many millions of transistors etched right into the silicon. Electrical signals are applied to make the transistor either allow or disallow the flow of electricity.

05. Which of the following is a component of a computer systems that executes programs, communicates with and usually controls the operation of other computer components?

A. CPU
B. Control Unit
C. ALU
D. None of the others

06. What is a CPU's clock speed?

A. The accuracy of time-keeping function
B. The number of times a second it refreshes its memory
C. The rate at which it can execute instructions
D. None of the others

The clock speed indicates how quickly the CPU can execute instructions. The frequency is measured in megahertz or gigahertz.

07. What part of the CPU performs arithmetic and logic operations?

A. The logic gate
B. The ALU
C. The system bus
D. None of the others

The arithmetic logic unit (ALU) performs arithmetic operations like addition, subtraction, multiplication and division and logic operations such as AND, OR, NOT, NAND, NOR and XOR.

08. When was the first commercial microprocessor introduced?

A. 1958
B. 1965
C. 1971
D. 1981

The first commercial microprocessor, the Intel 4004, was introduced in 1971. Although it couldn't do much -- it could only add and subtract four bits at a time -- it powered one of the first portable calculators.

09. Computer chips made from what materials?

A. Plastic
B. Silicon
C. Olestra
D. All of the others

Computer chips are small pieces of silicon onto which transistors are etched. Much of the microprocessor-producing industry is located in the San Francisco Bay Area in Southern California and has earned the nickname of "Silicon Valley."

10. Which of the following is not part of a job of computer chips?

A. Performing mathematical operations
B. Moving data from one memory location to another
C. Starting up the computer
D. All of the others are jobs of computer chips

Although CPUs have many complicated tasks to run, they do three basic things: perform mathematical operations, move data between memory locations and follow sets of instructions. The job of starting up the computer specifically involves the bootstrap loader.

11. The main purpose of having memory hierarchy is to _____.

A. Reduce access time
B. Provide large capacity
C. Reduce propagation time
D. Both Reduce access time And Provide large capacity

12. The main reason for the discontinuation of semiconductor based storage devices for providing large storage space is _____.

A. Lack of sufficient resources
B. High cost per bit value
C. Lack of speed of operation
D. None of the others

Explanation: <numeric> In case of semiconductor based memory technology, we get speed but the increase in the integration of various devices the cost is high.

13. ROM stands for _____.

A. Read only memory
B. Random only memory
C. Readily oral memory
D. Random available memory

14. On the PC, ROM BIOS is used to do what?

A. Load the operating system
B. Test hardware in the machine
C. Both Load the operating system And Test hardware in the machine
D. None of the others

When the microprocessor starts up, it looks towards the BIOS for several instructions. Among other things such as storing the boot sector in RAM after it's read, BIOS instructions check the machine's hardware for errors and then load the operating system.

15. The memory that a CPU can use directly is _____.

A. Cache memory
B. Clock memory
C. Direct access memory
D. All of the others

However instantanous the actions of a computer seem to be sometimes, every little operation takes time. Retrieving data from the cache, however, is much faster than retreiving from system memory.

16. About how much address space that a 64-bit processor can access?

A. 4 GB
B. 1,000 GB
C. One milion GB
D. One billion GB

While 32-bit microprocessors can only address between 2 and 4 gigabytes of RAM, 64-bit microprocessors can address as much as one billion gigabytes of RAM if needed. Although that may seem excessive for something like home computers, such extra space may be necessary in the future for overloaded servers.

17. What is another name for a microchip?

A. Integrated circuit
B. SCSI card
C. Circuit board
D. None of the others

Integrated circuits were conceived of in the late 1950s when engineers realized you could make computing components smaller by etching transistors, resistors and capacitors into a solid block of silicon rather than stringing them together with wires. And thus the modern microchip was born.

18. What is the term for a single chip that integrates all the computing components necessary to run a device?

A. System-on-a-chip
B. Nanochip
C. Multi-core processor
D. None of the others

Many of our smaller computing devices, such as smartphones and smart watches, use system-on-a-chip (SoC) processors to pack a ton of computing capability into a tiny package. These chips may include the CPU, GPU, RAM, ROM and other components all on one integrated circuit.

19. During transfer of data between the processor and memory we use _____ .

A. Cache
B. TLB
C. Buffers
D. Registers

20. What part of the CPU stores the location of the instruction to be executed?

A. Cache
B. Program counter
C. Data bus
D. None of the others

The program counter is a type of register that contains the address of either the current or next instruction to be executed.

21. Which registers of the following connects to data and address buses directly?

A. MBR and MAR
B. MAR and MBR
C. MBR and PC
D. MAR and PC

22. For converting virtual address into physical address, the programs are divided into _____.

A. Pages
B. Frames
C. Segments
D. Blocks

Explanation: <numeric> On the physical memory side the memory is divided into pages.

23. The starting address of the page table is stored in _____.

A. TLB
B. R0
C. Page table base register
D. None of the others

Explanation: <numeric> The register is used to hold the address which is used to access the table.

24. The area in the main memory that can hold one page is called as _____.

A. Page entry
B. Page frame
C. Frame
D. Block

25. The pages size shouldn't be too small, as this would lead to _____.

A. Transfer errors
B. Increase in operation time
C. Increase in access time
D. Decrease in performance

Explanation: <numeric> The access time of the magnetic disk is much longer than the access time of the memory.

26. The page length shouldn't be too long because

A. It reduces the program efficiency
B. It increases the access time
C. It leads to wastage of memory
D. None of the others

Explanation: <numeric> If the size is more than the required size then the extra space gets wasted.

27. _____ is a process in which memory is divided into groups of variable length.

A. Paging
B. Overlays
C. Segmentation
D. Paging with segmentation

28. - Statement I : When the processor executes a process it automatically converts from logical to physical address by adding the current starting location of the process, called its base address, to each logical address.

- Statement II : "Demand paging" means that each page of a process is brought in only when it is needed.

Which of the above statements are true?

A. Both the statements are true
B. Statement I is true
C. Statement II is true
D. Both the statements are false

29. - Statement I : TLB is an hardware including some registers. A part of page table is copied to them in order to increase performance of translating virtual addresses to physical addresses.

- Statement II : The purpose of a TLB is to avoid, most of the time, having to go to disk to retrieve a page table entry.

Which of the above statements are true?

A. Both the statements are true
B. Statement I is true
C. Statement II is true
D. Both the statements are false

30. Which addressing mode of the following is most suitable to change the normal sequence of execution of instructions.

A. Relative
B. Indirect
C. Index with Offset
D. Immediate

Explanation: The relative addressing mode is used for this since it directly updates the PC.

31. The addressing mode used in PUSH B is _____.

A. Direct
B. Register
C. Register Indirect
D. Index

32. What is the content of Stack Pointer?

A. Address of the current instruction
B. Address of the next instruction
C. Address of the top element of the stack
D. None of the others

33. The instructions based on the stack operations are also known as 'zero address' or 'implied instructions', because _____.

A. Address gets updated automatically in stack pointer
B. Processor can refer a memory stack without specifying the address
C. Address gets updated automatically in stack pointer And Processor can refer a memory stack without specifying the address
D. None of the others

34. What is the difference between a compiler and an interpreter?

A. Compilers are used for Special Purpose Languages while interpreters are used for General Purpose Langauges
B. Compilers are written for translating LLLs and Interpreters for translating HLLs.
C. Compilers are written for translating HLLs and Interpreters for translating LLLs.
D. Compilers translate a whole program before starting execution while interpreters translate and execute line by line.

35. Which of the following is/are used in translating HLLs?

A. Compilers only
B. Compilers, Interpreters and Assemblers
C. Compilers and Interpreters
D. Compilers and Assemblers

36. If a HLL program is to be run a number of times, _____.

A. An interpreter can produce object code that may be saved and run straight away
B. An interpreter would have to translate it each time it is run
C. It is best to use an assembler
D. An interpreter would translate it once and then produce object code that can be saved and afterwards run directly (without needing further translation)

37. What is the advantage of using Assembly language rather than HLLs?

A. Assembly programs are simpler to translate and occupy less storage space
B. Assembly languages are easier to code in
C. Assembly language programs are portable
D. Assembly is simpler to translate and easier to code in

38. Which parameter of computer determines its power to do various operations on data items?

A. Instruction set
B. Memory size
C. Assembly language
D. Application language

39. Which category in the following architectures, the CPU is designed to perform tasks using a small, simple computer instruction set.

A. CISC
B. RISC
C. RAID
D. None of the others

As opposed to CISC (Complex Instruction Set Computer) architecture, in which the hardware has a large set of more complex instructions, RISC (Reduced Instruction Set Computer) architecture includes a more optimized

set of simple instructions, each requiring fewer transistors and executing in only one clock cycle. These instructions can be strung together via software to perform more complex operations.

40. What processor design company came to dominate the mobile device market with their low-power RISC based architecture?

A. Intel
B. AMD
C. ARM
D. None of the others

The company Advanced RISC Machines (ARM) developed processors using RISC architecture that allowed for small chips with high-speed performance at low-power, making them ideal for small devices like smartphones, tablets and wearable devices.

41. The type of processing where multiple instructions are sent to more than one processor to execute at the same time is called _____.

A. Word processing
B. Data processing
C. Parallel processing
D. None of the others

Many of today's CPUs include multiple processing cores, allowing the divvying up of instructions to speed up processing. It should be noted that two cores don't double speed, as there are other factors at play.

42. Systems that do not have parallel processing capabilities are _____.

A. SISD
B. SIMD
C. MIMD
D. None of the others

43. Which factors of the following led to the development of multicore organizations?

A. The increase of logic density
B. The hardware performance
C. The software challenges
D. None of the others

44. To control the power density we can use more of the chip area for _____.

A. Multicore
B. Cache memory
C. Silicon
D. Resistors

45. The memory, inside the CPU, is used to store the copy of data or instructions stored in larger memories is called _____.

A. Level 1 cache
B. Level 2 cache
C. Registers
D. TLB

Explanation: These memory devices are generally used to map onto the data stored in the larger memories.

46. The larger memory, inside the CPU, placed between the primary cache and the memory is called _____.

A. Level 1 cache
B. Level 2 cache
C. EEPROM
D. TLB

Explanation: This is basically used to provide effective memory mapping.

47. Applications are characterized by having a small number of highly threaded processes called _____.

A. Multithreaded native
B. Multi-instance
C. Multiprocess
D. None of the others

48. Applications are characterized by the presence of many single-threaded processes called _____.

A. Multi-instance
B. Multi-process
C. Multi-threaded native
D. None of the others

49. Applications can be run multiple instances of them in parallel called _____.

A. Multi-threaded native
B. Multi-process
C. Multi-instance
D. None of the others

50. Which applications of the following are supported effectively by multicore organizations?

A. Multi-threaded native applications
B. Multi-process applications
C. Multi-instance applications
D. All of the others