Vô là có hết, nên là cứ vô xem. Môn này là Cea201 :v

Computer Architecture (Trường Đại học FPT)

QN=1	The instructions, after being retrieved from memory, are decoded and stored in the ....
a.	IR
b.	MAR
c.	MBR
d.	PC
ANSWER:	a
MARK:	1
UNIT:	3
MIX CHOICES	Yes

QN=2	If an instruction which contains arithmetic operations, the data will be passed to:
a.	Control unit
b.	ALU
c.	I/O ports
d.	Registers
ANSWER:	b
MARK:	1
UNIT:	3
MIX CHOICES	Yes

QN=3	Interrupts can be generated in response to ....
a.	Detected program errors such as arithmetic overflow or division by zero
b.	Detected hardware faults
c.	Input/Output activities

d.	All of the others
ANSWER:	d
MARK:	1
UNIT:	3
MIX CHOICES	Yes

QN=4	When the processor is executing the program, if there are interrupts (not prohibited) sent to it, then it:
a.	Serve interrupts immediately, then execute the program
b.	Complete the program, then execute the interrupt
c.	Complete the current instruction, then execute the interrupt, finally return to continue the program
d.	Interrupt rejection, not serving
ANSWER:	c
MARK:	1
UNIT:	3
MIX CHOICES	Yes

QN=5	Which types of transfers are supported by the connection structure of the computer?
a.	Memory to memory, memory to or from processor, I/O to or from processor
b.	Memory to or from processor, I/O to or from processor, I/O to or from memory
c.	I/O to or from processor, I/O to I/O, memory to or from processor
d.	None of the others
ANSWER:	b

MARK:	1
UNIT:	3
MIX CHOICES	Yes

QN=1	What is cache memory?
a.	A cheap memory that can be plugged into the mother board to expand main memory
b.	A fast memory that is used to store recently accessed data
c.	A reserved portion of main memory used to save important data
d.	A special area of memory on the chip that is used to save frequently used constants
ANSWER:	b
MARK:	1
UNIT:	4
MIX CHOICES	Yes

QN=2	The cache is used to narrow the speed gap between .... and ....
a.	RAM and ROM
b.	RAM and HDD
c.	CPU and RAM
d.	None of the others
ANSWER:	c
MARK:	1
UNIT:	4
MIX CHOICES	Yes

QN=3	.... maps each block of main memory to only one possible cache line.
a.	Direct mapping
b.	Associative mapping
c.	Set associative mapping
d.	Indirect mapping
ANSWER:	a
MARK:	1
UNIT:	4
MIX CHOICES	Yes

QN=4	.... permits each main memory block to be loaded into any line of the cache.
a.	Direct mapping
b.	Associative mapping
c.	Set associative mapping
d.	Indirect mapping
ANSWER:	b
MARK:	1
UNIT:	4
MIX CHOICES	Yes

QN=5	In direct mapping, the presence of a data block in the cache is checked with the help of what?
a.	Line
b.	Block
c.	Word

d.	Tag
ANSWER:	d
MARK:	1
UNIT:	4
MIX CHOICES	Yes

QN=1	With RAM, which of the following statements is true:
a.	It is not volatile
b.	DRAM is made from flip-flops
c.	SRAM is made from capacitors
d.	A place to store information that the computer is processing
ANSWER:	d
MARK:	1
UNIT:	5
MIX CHOICES	Yes

QN=2	With RAM, which of the following statements is false:
a.	DRAM is made from flip-flops
b.	DRAM is made from capacitors
c.	SRAM is made from flip-flops
d.	SRAM does not need to be refreshed
ANSWER:	a
MARK:	1
UNIT:	5
MIX CHOICES	Yes

QN=3	With SRAM memory chips 64Kx4bit, which of the following statements is false:
a.	There are 16 address lines
b.	There are 4 data lines
c.	The address lines are: D0 -> D15
d.	The address lines are: A0 -> A15
ANSWER:	c
MARK:	1
UNIT:	5
MIX CHOICES	Yes

QN=4	With the SRAM memory 16Kx8bit, which of the following statements is true:
a.	The address lines are: D0 -> D13
b.	The address lines are: A0 -> A13
c.	The data lines are: A0 -> A7
d.	The data lines are: D0 -> D8
ANSWER:	b
MARK:	1
UNIT:	5
MIX CHOICES	Yes

QN=5	An 16 bit address generates an address space of ………. locations
a.	65,536
b.	256
c.	2 ^ 32

d.	1,048,576
ANSWER:	a
MARK:	1
UNIT:	5
MIX CHOICES	Yes

QN=6	A computer's memory is composed of 8K words of 32 bits each. How many total bytes in memory?
a.	32,000
b.	32,768
c.	262,144
d.	256,000
ANSWER:	b
MARK:	1
UNIT:	5
MIX CHOICES	Yes

QN=1	If the drive has 20 surfaces, how many heads will it have?
a.	1
b.	5
c.	10
d.	20
ANSWER:	d
MARK:	1

UNIT:	6
MIX CHOICES	Yes

QN=2	The average time required to reach a storage location in memory and obtain its contents is called the ....
a.	Access time
b.	Transfer time
c.	Seek time
d.	Turnaround time
ANSWER:	a
MARK:	1
UNIT:	6
MIX CHOICES	Yes

QN=3	The data can be accessed from the disk using ....
a.	Surface number
b.	Sector number
c.	Track number
d.	All of the others
ANSWER:	d
MARK:	1
UNIT:	6
MIX CHOICES	Yes

QN=4	A computer that is advertised as having a 8GB DRAM memory and a 256GB SSD

	has:
a.	8GB of auxiliary memory and 256GB of primary memory
b.	256GB of secondary memory and 8GB of primary memory
c.	8GB of cache, 256GB of primary memory
d.	None of the others
ANSWER:	b
MARK:	1
UNIT:	6
MIX CHOICES	Yes

QN=5	A hard disk takes 0.25 milliseconds to move between adjacent tracks. If the disk has 100 cylinders, how long will it take for the head to move from the outermost cylinder to the innermost cylinder?
a.	12.5 milliseconds
b.	2500 microseconds
c.	12500 microseconds
d.	0.025 seconds
ANSWER:	d
MARK:	1
UNIT:	6
MIX CHOICES	Yes

QN=1	There are three methods for performing I/O:
a.	Interrupt-driven I/O, System-driven I/O, DMA
b.	Interrupt-driven I/O, System-driven I/O, Programmed I/O
c.	Programmed I/O, Interrupt-driven I/O, DMA

d.	Programmed I/O, System-driven I/O, DMA
ANSWER:	c
MARK:	1
UNIT:	7
MIX CHOICES	Yes

QN=2	With Interrupt-driven I/O, which of the following statements is true?
a.	Peripherals are the active object in data exchange
b.	The method is fully processed by hardware
c.	CPU is an active object in data exchange
d.	The method is fully processed by software
ANSWER:	a
MARK:	1
UNIT:	7
MIX CHOICES	Yes

QN=3	I/O addressing methods include:
a.	Memory-mapped I/O
b.	Isolated I/O
c.	Both memory-mapped I/O and isolated I/O
d.	None of the others
ANSWER:	c
MARK:	1
UNIT:	7

MIX CHOICES	Yes

QN=4	With memory-mapped I/O, which of the following statements is true?
a.	The I/O devices and the memory share the same address space
b.	The I/O devices have a seperate address space
c.	The memory and I/O devices have an associated address space
d.	A part of the memory is specifically set aside for the I/O operation
ANSWER:	a
MARK:	1
UNIT:	7
MIX CHOICES	Yes

QN=5	With isolated I/O, which of the following statements is true?
a.	The I/O devices and the memory share the same address space
b.	The I/O devices have a seperate address space
c.	The memory and I/O devices have an associated address space
d.	A part of the memory is specifically set aside for the I/O operation
ANSWER:	b
MARK:	1
UNIT:	7
MIX CHOICES	Yes

QN=1	Long-term scheduling is:
a.	The decision to add which programs to the system for processes
b.	The decision to add to the number of processes that are partially or fully in main

	memory
c.	The decision as to which available process will be executed by the processor
d.	The decision as to which process's pending I/O request shall be handled by an available I/O device
ANSWER:	a
MARK:	1
UNIT:	8
MIX CHOICES	Yes

QN=2	Medium-term scheduling is:
a.	The decision as to which process's pending I/O request shall be handled by an available I/O device
b.	The decision as to which available process will be executed by the processor
c.	The decision to add to the number of processes that are partially or fully in main memory
d.	The decision to add which programs to the system for processes
ANSWER:	c
MARK:	1
UNIT:	8
MIX CHOICES	Yes

QN=3	Short-term scheduling is:
a.	The decision to add which programs to the system for processes
b.	The decision as to which available process will be executed by the processor
c.	The decision to add to the number of processes that are partially or fully in main memory
d.	The decision as to which process's pending I/O request shall be handled by an

	available I/O device
ANSWER:	b
MARK:	1
UNIT:	8
MIX CHOICES	Yes

QN=4	The purpose of swapping is:
a.	To remove processes not in a ready state
b.	To provide for efficient use of main memory for processes execution
c.	To add processes in a ready state to main memory
d.	None of the others
ANSWER:	b
MARK:	1
UNIT:	8
MIX CHOICES	Yes

QN=5	Swapping is executed by ……..
a.	Long-term scheduler
b.	Medium-term scheduler
c.	Short-term scheduler
d.	None of the others
ANSWER:	b
MARK:	1
UNIT:	8
MIX CHOICES	Yes

QN=1	An OR gate can be seen as ....
a.	Switches connected in parallel
b.	Switches connected in series
c.	MOS transistors connected in series
d.	None of the others
ANSWER:	a
MARK:	1
UNIT:	11
MIX CHOICES	Yes

QN=2	The output of a NAND gate is low if ....
a.	All of its inputs are low
b.	Only of its inputs is low
c.	All of its inputs are high
d.	Only of its inputs is high
ANSWER:	c
MARK:	1
UNIT:	11
MIX CHOICES	Yes

QN=3	The output of a NOR gate is high if ....
a.	Only of its inputs is low
b.	All of its inputs are low
c.	Only of its inputs is high

d.	All of its inputs are high
ANSWER:	b
MARK:	1
UNIT:	11
MIX CHOICES	Yes

QN=4	Which of the following outputs is 1 when one input is 1 and other input is 0?
a.	OR gate
b.	AND gate
c.	NAND gate
d.	Both OR gate and NAND gate
ANSWER:	d
MARK:	1
UNIT:	11
MIX CHOICES	Yes

QN=5	Which of the following are added to the inputs of the AND gate to convert it to the NOR gate?
a.	XOR
b.	NOT
c.	AND
d.	OR
ANSWER:	b
MARK:	1
UNIT:	11

MIX CHOICES	Yes

QN=1	It's a collection of different instructions that the processor can execute, it also provides instructions to the processor, to tell it what it needs to do.
a.	Operation Code
b.	Instruction Set
c.	Processor Register
d.	None of the others
ANSWER:	b
MARK:	1
UNIT:	12
MIX CHOICES	Yes

QN=2	It's the common form of data which is text or character strings.
a.	Addresses
b.	Numbers
c.	Characters
d.	Conversion
ANSWER:	c
MARK:	1
UNIT:	12
MIX CHOICES	Yes

QN=3	It's most fundamental type of machine instructions, to transfer of data from one

	location to another.
a.	Data transfer
b.	Transfer of control
c.	System control
d.	None of the others
ANSWER:	a
MARK:	1
UNIT:	12
MIX CHOICES	Yes

QN=4	It's the bitwise operation and also includes AND, OR, NOT, XOR, and XNOR gates.
a.	Operands
b.	Arithmetic
c.	Characters
d.	Logical
ANSWER:	d
MARK:	1
UNIT:	12
MIX CHOICES	Yes

QN=5	It's the operation updates the Program Counter (PC) to contain the address of some instruction in memory.
a.	Transfer of Control
b.	I/O
c.	System Control

d.	Skip Instruction
ANSWER:	a
MARK:	1
UNIT:	12
MIX CHOICES	Yes

QN=1	.... address mode is the mode in which the operand is a memory cell has the address located in another memory cell.
a.	Direct
b.	Indirect
c.	Register Indirect
d.	Immediate
ANSWER:	b
MARK:	1
UNIT:	13
MIX CHOICES	Yes

QN=2	.... addressing mode is the mode in which the operand is the content of the register.
a.	Register
b.	Index with Offset
c.	Relative
d.	Indirect
ANSWER:	a
MARK:	1
UNIT:	13

MIX CHOICES	Yes

QN=3	.... address mode is the mode by which you directly specify the value of the operand.
a.	Base-Register
b.	Direct
c.	Immediate
d.	Relative
ANSWER:	c
MARK:	1
UNIT:	13
MIX CHOICES	Yes

QN=4	.... address mode is the most suitable mode to change the normal execution sequence of the instructions.
a.	Immediate
b.	Register
c.	Indirect
d.	Relative
ANSWER:	d
MARK:	1
UNIT:	13
MIX CHOICES	Yes

QN=5	The addressing mode used in PUSH B is ....

a.	Direct
b.	Register
c.	Register Indirect
d.	Index with Offset
ANSWER:	c
MARK:	1
UNIT:	13
MIX CHOICES	Yes

QN=1	.... registers enable the machine or assembly language programmer to minimize main memory references by optimizing use of registers.
a.	General purpose
b.	Control and status
c.	User-visible
d.	None of the others
ANSWER:	c
MARK:	1
UNIT:	14
MIX CHOICES	Yes

QN=2	A processor performs fetching or decoding of different instructions while executing another instruction is called ....
a.	Superscalar
b.	Pipelining
c.	Parallel Computation

d.	None of the others
ANSWER:	b
MARK:	1
UNIT:	14
MIX CHOICES	Yes

QN=3	The time interval when the pipeline, or part of the pipeline, is idle because conditions do not permit continued execution is called ....
a.	Stalls
b.	Bubbles
c.	Stalls or Bubbles
d.	None of the others
ANSWER:	c
MARK:	1
UNIT:	14
MIX CHOICES	Yes

QN=4	For the unsigned integer, 8 bits. Let's say the result when adding: 0100 0111 + 0101 1111.
a.	146
b.	166
c.	176
d.	56
ANSWER:	b
MARK:	1

UNIT:	14
MIX CHOICES	Yes

QN=5	For the signed integer, 8 bits, use the 2's complement method, the representation value of the number -29 is:
a.	1000 0000
b.	1110 0011
c.	1111 0000
d.	1000 1111
ANSWER:	b
MARK:	1
UNIT:	14
MIX CHOICES	Yes

QN=1	Characteristics of RISC organization:
a.	A limited instruction set with a fixed format
b.	A large number of registers or the use of a compiler to optimize register usage
c.	An emphasis on optimizing the instruction pipeline
d.	All of the others
ANSWER:	d
MARK:	1
UNIT:	15
MIX CHOICES	Yes

QN=2	Which of the following architecture was the first to implement pipeline techniques?
a.	RISC
b.	CISC
c.	ISA
d.	ANNA
ANSWER:	a
MARK:	1
UNIT:	15
MIX CHOICES	Yes

QN=3	Which of the following is a way to improve pipeline performance by using a branch no effect until the single instruction that immediately follows the branch is done?
a.	Delayed load
b.	Delayed branch
c.	Unrolling
d.	None of the others
ANSWER:	b
MARK:	1
UNIT:	15
MIX CHOICES	Yes

QN=4	A similar approach to delayed branch, which can be used on the LOAD instructions, is ....
a.	Delayed program
b.	Delayed register

c.	Delayed load
d.	Delayed slot
ANSWER:	c
MARK:	1
UNIT:	15
MIX CHOICES	Yes

QN=5	- Statement I : The major cost in the life cycle of a system is hardware. - Statement II : Almost all RISC instructions use simple register addressing. Which of the above statements are true?
a.	Both the statements are true
b.	Statement I is true
c.	Statement II is true
d.	Both the statements are false
ANSWER:	c
MARK:	1
UNIT:	15
MIX CHOICES	Yes

QN=1	.... is a processor that performs a parallel form called instruction-level parallelism in a single processor.
a.	Scalar
b.	Uniprocessors

c.	Superscalar
d.	None of the others
ANSWER:	c
MARK:	1
UNIT:	16
MIX CHOICES	Yes

QN=2	What are the fundamental limitations to the parallelism that a system must address?
a.	Procedural dependency
b.	Resource conflicts
c.	Anti-dependency
d.	All of the others
ANSWER:	d
MARK:	1
UNIT:	16
MIX CHOICES	Yes

QN=3	Which techniques of the following can be applied in a superscalar processor to enhance performance?
a.	Duplication of resources
b.	Out-of-order issue
c.	Renaming
d.	All of the others
ANSWER:	d
MARK:	1

UNIT:	16
MIX CHOICES	Yes

QN=4	The instruction window (or instruction buffer) is used in:
a.	In-order issue with in-order completion
b.	In-order issue with out-of-order completion
c.	Out-of-order issue with out-of-order completion
d.	None of the others
ANSWER:	c
MARK:	1
UNIT:	16
MIX CHOICES	Yes

QN=5	- Statement I : Register renaming eliminates anti-dependencies and output dependencies. - Statement II : Out-of-order completion requires instruction issue logic is less complicated than In-order completion. Which of the above statements are true?
a.	Both the statements are true
b.	Statement I is true
c.	Statement II is true
d.	Both the statements are false
ANSWER:	b
MARK:	1
UNIT:	16

MIX CHOICES	Yes

QN=1	The type of processing where multiple instructions are sent to more than one processor to execute at the same time is called ....
a.	Word processing
b.	Data processing
c.	Parallel processing
d.	None of the others
ANSWER:	c
MARK:	1
UNIT:	17
MIX CHOICES	Yes

QN=2	Symmetric multiprocessors (SMPs) fall into which category of computer systems?
a.	MIMD
b.	SIMD
c.	SISD
d.	MISD
ANSWER:	a
MARK:	1
UNIT:	17
MIX CHOICES	Yes

QN=3	In an SMP computer, the largest disadvantage of the bus organization is ....

a.	Reliability
b.	Performance
c.	Cache coherence
d.	None of the others
ANSWER:	b
MARK:	1
UNIT:	17
MIX CHOICES	Yes

QN=4	To improve performance and control the power density we can use more of the chip area for ……..
a.	Resistors
b.	Multicore
c.	Silicon
d.	Cache memory
ANSWER:	d
MARK:	1
UNIT:	17
MIX CHOICES	Yes

QN=5	- Statement I: The cache coherence problem is typically addressed in hardware. - Statement II: Snoopy protocols are suitable for a bus-based multiprocessor. Which of the above statements are true?
a.	Both the statements are true
b.	Statement I is true

c.	Statement II is true
d.	Both the statements are false
ANSWER:	a
MARK:	1
UNIT:	17
MIX CHOICES	Yes

QN=1	Which factors of the following led to the development of multicore organizations?
a.	The increase of logic density
b.	The hardware performance
c.	The software challenges
d.	None of the others
ANSWER:	b
MARK:	1
UNIT:	18
MIX CHOICES	Yes

QN=2	Which applications of the following are supported effectively by multicore organizations?
a.	Multi-threaded native applications
b.	Multi-process applications
c.	Multi-instance applications
d.	All of the others
ANSWER:	d
MARK:	1

UNIT:	18
MIX CHOICES	Yes

QN=3	Applications are characterized by having a small number of highly threaded processes called ....
a.	Multithreaded native
b.	Multi-instance
c.	Multiprocess
d.	None of the others
ANSWER:	a
MARK:	1
UNIT:	18
MIX CHOICES	Yes

QN=4	Applications are characterized by the presence of many single-threaded processes called ....
a.	Multi-instance
b.	Multi-process
c.	Multi-threaded native
d.	None of the others
ANSWER:	b
MARK:	1
UNIT:	18
MIX CHOICES	Yes

QN=5	Applications can be run multiple instances of them in parallel called ……..
a.	Multi-threaded native
b.	Multi-process
c.	Multi-instance
d.	None of the others
ANSWER:	c
MARK:	1
UNIT:	18
MIX CHOICES	Yes