



How to design PCB

Pay It Forward

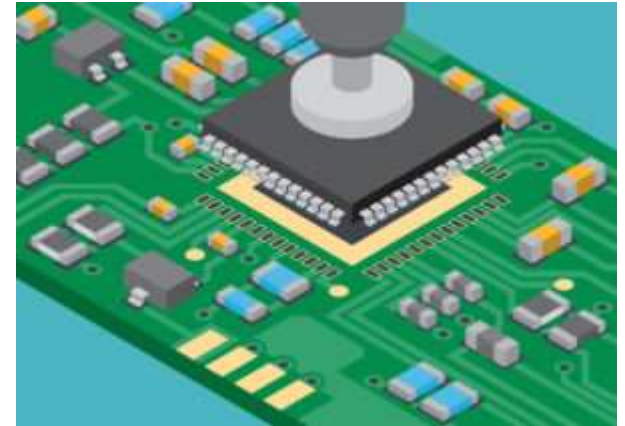
C21

SMD/SMT Component



SMD/SMT Component

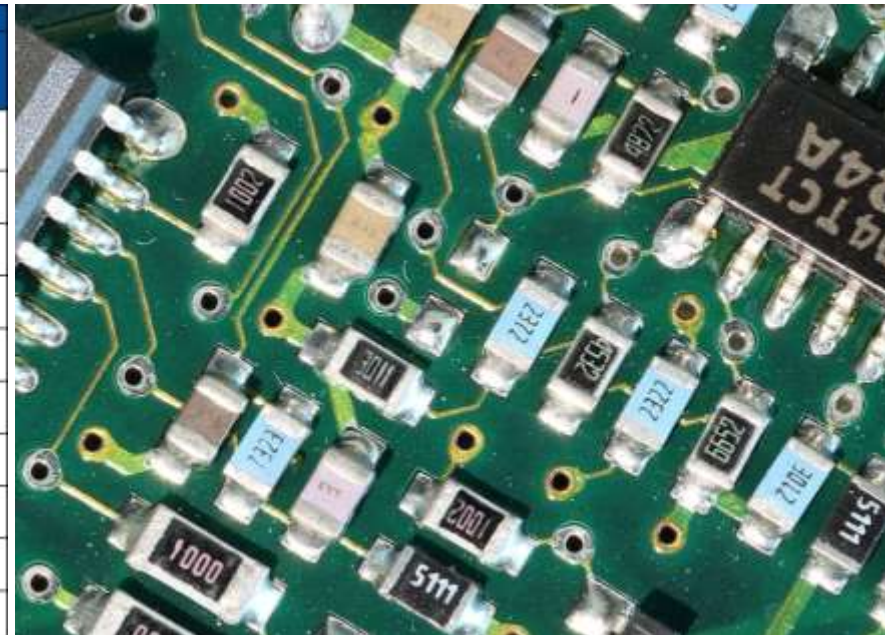
- Surface Mount Devices
- Surface Mount Technology



SMD Resistor

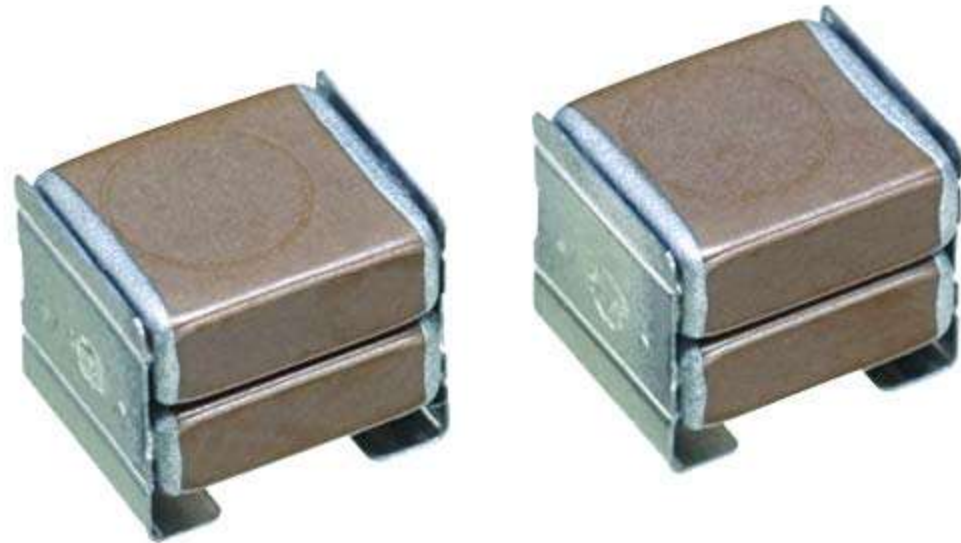
- Giá trị: 0, 10, 330, 4k7, ...
- Kích thước: 0805, 0603, 0402, 0201, ...
- Công suất: 1/20, 1/10, 1/8, ...
- Sai số: 0.25%, 1%, ...

Imperial				Size	Metric			
Resistor Case Code	Approx. Length (in)	Approx. Width (in)	Power (W)		Resistor Case Code	Approx. Length (mm)	Approx. Width (mm)	Power (W)
01005	0.016	0.008	0.031	-	0402	0.4	0.2	0.031
0201	0.02	0.01	1 / 20 (0.05)	-	0603	0.6	0.3	1 / 20 (0.05)
0402	0.04	0.02	1 / 16 (0.062)	-	1005	1.0	0.5	1 / 16 (0.062)
0603	0.06	0.03	1 / 10 (0.10)	-	1608	1.6	0.8	1 / 10 (0.10)
0805	0.08	0.05	1 / 8 (0.125)	-	2012	2.0	1.25	1 / 8 (0.125)
1206	0.125	0.06	1 / 4 (0.25)	-	3216	3.2	1.6	1 / 4 (0.25)
1210	0.125	0.10	1 / 2 (0.5)	-	3225	3.2	2.5	1 / 2 (0.5)
1812	0.18	0.125	3 / 4 (0.75)	-	4532	4.5	3.2	3 / 4 (0.75)
2010	0.20	0.10	3 / 4 (0.75)	-	5025	5.0	2.5	3 / 4 (0.75)
2512	0.25	0.125	1	-	6332	6.3	3.2	1



SMD Capacitor

- Tụ không phân cực



SMD Capacitor

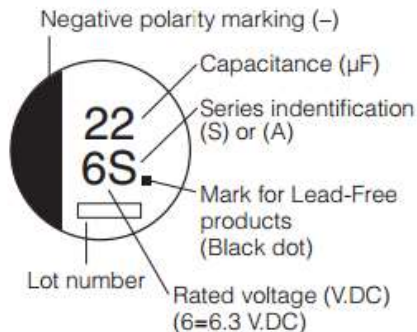
- Tụ hóa

270uF



Marking

Example : 6.3 VDC 22 μ F
Marking color : BLACK



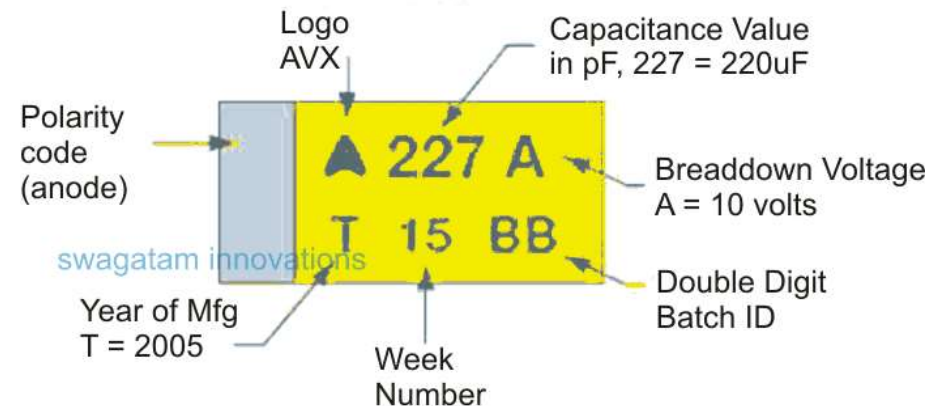
100uF
6V

100uF
16V

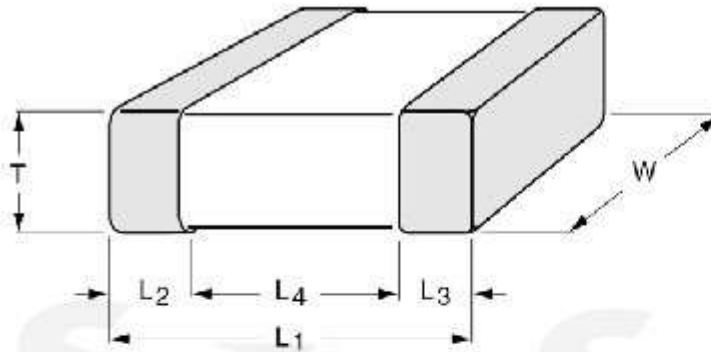


+

SMD Electrolytic Capacitor



SMD Package Ceramic Capacitor



		0201	0402	0603	0805	1206	1210	1812
L_1 [mm]		$0,6 \pm 0,03$	$1,0 \pm 0,05$	$1,6 \pm 0,10$	$2,0 \pm 0,10^1$	$3,2 \pm 0,15^1$	$3,2 \pm 0,20^1$	$4,5 \pm 0,20^1$
					$2,0 \pm 0,20^2$	$3,2 \pm 0,20^2$	$3,2 \pm 0,30^2$	$4,5 \pm 0,40^2$
W [mm]		$0,3 \pm 0,03$	$0,5 \pm 0,05$	$0,8 \pm 0,10$	$1,25 \pm 0,10^1$	$1,6 \pm 0,15^1$	$2,5 \pm 0,20^1$	$3,2 \pm 0,20$
					$1,25 \pm 0,20^2$	$1,6 \pm 0,20^2$	$2,5 \pm 0,30^2$	
T [mm]	min.	$0,3 \pm 0,03$	$0,5 \pm 0,05$	$0,8 \pm 0,15$	$0,6 \pm 0,10$	$0,6 \pm 0,10$	$0,6 \pm 0,10$	$0,6 \pm 0,10$
	max.				$1,25 \pm 0,20$	$1,6 \pm 0,20$	$2,5 \pm 0,20$	$3,2 \pm 0,20$
L_2/L_3 [mm]	min.	0,10	0,20	0,20	0,25	0,25	0,25	0,25
	max.	0,20	0,30	0,60	0,75	0,75	0,75	0,75
L_4 [mm]	min.	0,20	0,40	0,40	0,55	1,40	1,40	2,20

¹ $C < 1 \mu F$ and all NPO

² $C \geq 1 \mu F$

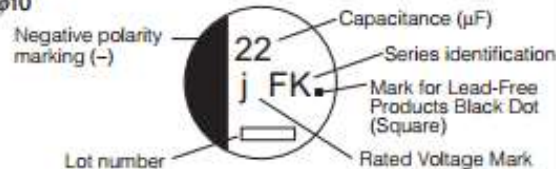
SMD Package Electrolytic Capacitor

■ Marking

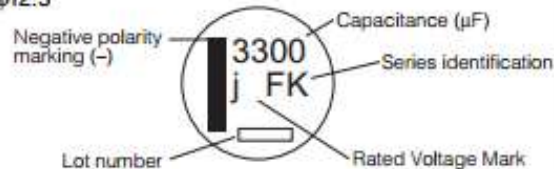
Example: 6.3 V 22 μ F, 6.3 V 3300 μ F

Marking color : BLACK

$\leq \phi 10$



$\geq \phi 12.5$

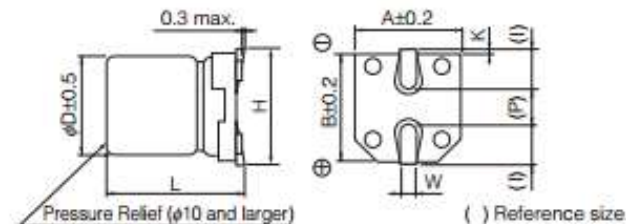


Rated Voltage Mark

j	6.3 V	H	50 V
A	10 V	J	63 V
C	16 V	K	80 V
E	25 V	2A	100 V
V	35 V		

■ Dimensions in mm (not to scale)

(Unit : mm)



Size code	D	L	A, B	H	I	W	P	K
B	4.0	5.8 \pm 0.3	4.3	5.5 max.	1.8	0.65 \pm 0.1	1.0	0.35 $^{+1.5}_{-0.2}$
C	5.0	5.8 \pm 0.3	5.3	6.5 max.	2.2	0.65 \pm 0.1	1.5	0.35 $^{+1.5}_{-0.2}$
D	6.3	5.8 \pm 0.3	6.6	7.8 max.	2.6	0.65 \pm 0.1	1.8	0.35 $^{+1.5}_{-0.2}$
D8	6.3	7.7 \pm 0.3	6.6	7.8 max.	2.6	0.65 \pm 0.1	1.8	0.35 $^{+1.5}_{-0.2}$
E	8.0	6.2 \pm 0.3	8.3	9.5 max.	3.4	0.65 \pm 0.1	2.2	0.35 $^{+1.5}_{-0.2}$
F	8.0	10.2 \pm 0.3	8.3	10.0 max.	3.4	0.90 \pm 0.2	3.1	0.70 \pm 0.2
G	10.0	10.2 \pm 0.3	10.3	12.0 max.	3.5	0.90 \pm 0.2	4.6	0.70 \pm 0.2
H13	12.5	13.5 \pm 0.5	13.5	15.0 max.	4.7	0.90 \pm 0.3	4.4	0.70 \pm 0.3
J16	16.0	16.5 \pm 0.5	17.0	19.0 max.	5.5	1.20 \pm 0.3	6.7	0.70 \pm 0.3
K16	18.0	16.5 \pm 0.5	19.0	21.0 max.	6.7	1.20 \pm 0.3	6.7	0.70 \pm 0.3

SMD Package Tantalum Capacitor

Table 2 – Land Dimensions/Courtyard

KEMET	Metric Size Code	Density Level A: Maximum (Most) Land Protrusion (mm)						Density Level B: Median (Nominal) Land Protrusion (mm)						Density Level C: Minimum (Least) Land Protrusion (mm)					
Case	EIA	W	L	S	V1	V2	W	L	S	V1	V2	W	L	S	V1	V2			
A	3216-18	1.35	2.20	0.62	6.02	2.80	1.23	1.80	0.82	4.92	2.30	1.13	1.42	0.98	4.06	2.04			
B	3528-21	2.35	2.21	0.92	6.32	4.00	2.23	1.80	1.12	5.22	3.50	2.13	1.42	1.28	4.36	3.24			
M	3528-15	2.35	2.20	0.92	6.32	4.00	2.23	1.80	1.12	5.22	3.50	2.13	1.42	1.28	4.36	3.24			
C	6032-25	2.35	2.77	2.37	8.92	4.50	2.23	2.37	2.57	7.82	4.00	2.13	1.99	2.73	6.96	3.74			
U	6032-15	2.35	2.77	2.37	8.92	4.50	2.23	2.37	2.57	7.82	4.00	2.13	1.99	2.73	6.96	3.74			
D	7343-31	2.55	2.77	3.67	10.22	5.60	2.43	2.37	3.87	9.12	5.10	2.33	1.99	4.03	8.26	4.84			
E ¹	7360-38	4.25	2.77	3.67	10.22	7.30	4.13	2.37	3.87	9.12	6.80	4.03	1.99	4.03	8.26	6.54			
T	3528-12	2.35	2.20	0.92	6.32	4.00	2.23	1.80	1.12	5.22	3.50	2.13	1.42	1.28	4.36	3.24			
V	7343-20	2.55	2.77	3.67	10.22	5.60	2.43	2.37	3.87	9.12	5.10	2.33	1.99	4.03	8.26	4.84			
X ²	7343-43	2.55	2.77	3.67	10.22	5.60	2.43	2.37	3.87	9.12	5.10	2.33	1.99	4.03	8.26	4.84			

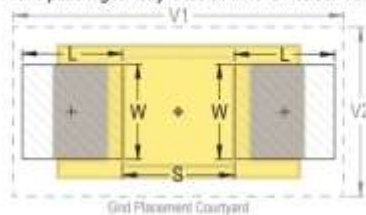
Density Level A: For low-density product applications. Recommended for wave solder applications and provides a wider process window for reflow solder processes.

Density Level B: For products with a moderate level of component density. Provides a robust solder attachment condition for reflow solder processes.

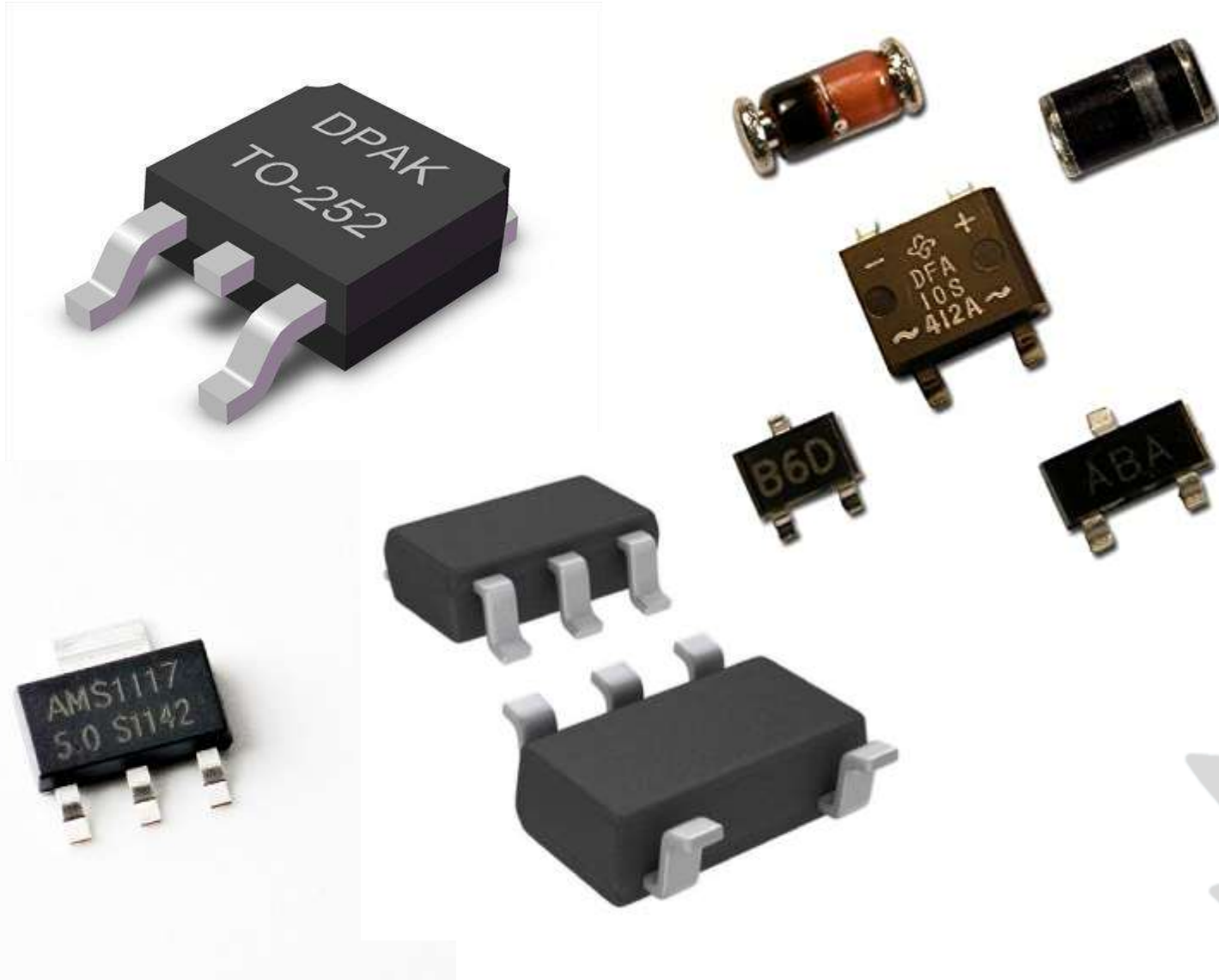
Density Level C: For high component density product applications. Before adapting the minimum land pattern variations the user should perform qualification testing based on the conditions outlined in IPC standard 7351 (IPC-7351).

¹ Height of these chips may create problems in wave soldering.

² Land pattern geometry is too small for silkscreen outline.

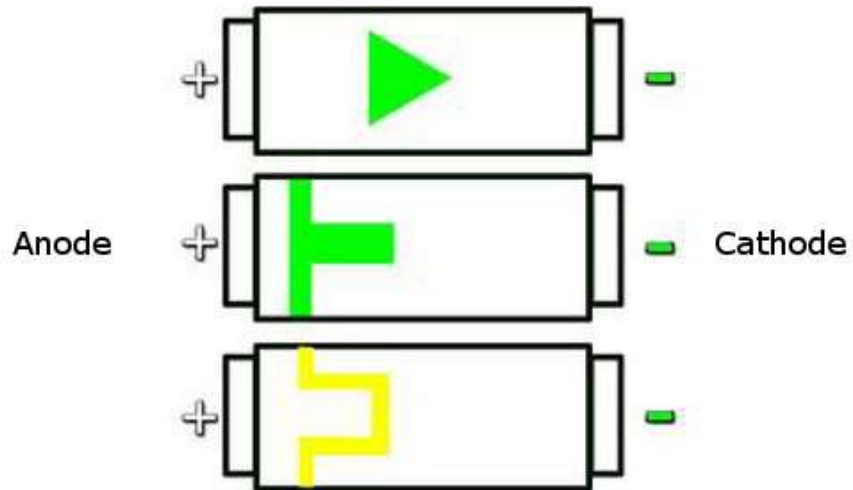


SMD semiconductor



SMD LED

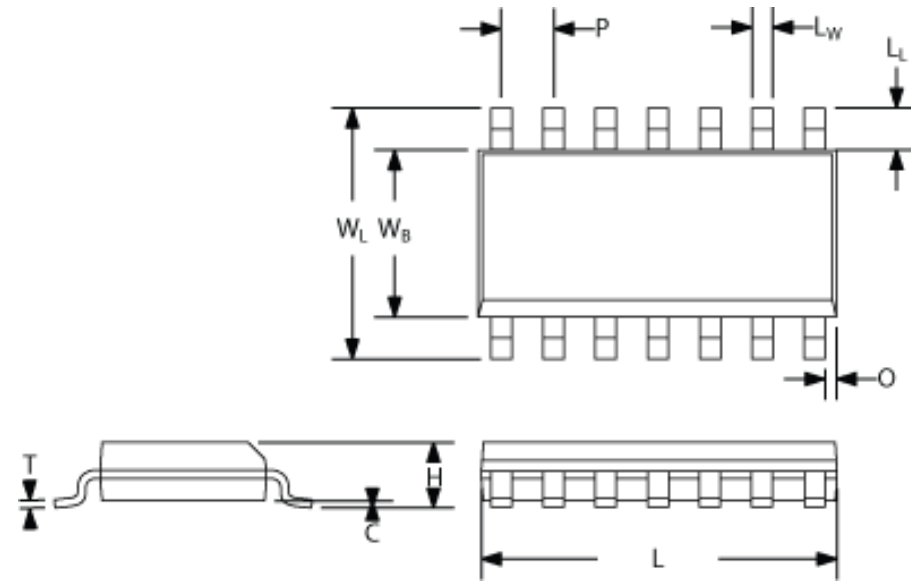
Surface Mount LED Polarity Indictators
Underside of an SMD LED



SMD Inductor



SOIC (Small Outline IC)



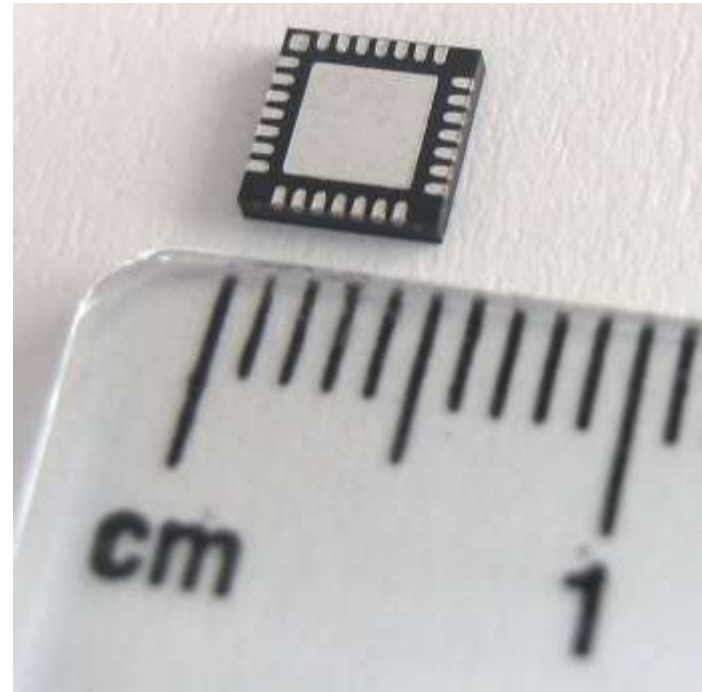
QFP Package

Package
BQFP: bumped quad flat package
BQFPH: bumped quad flat package with heat spreader
CQFP: ceramic quad flat package
EQFP: plastic enhanced quad flat package
FQFP: fine pitch quad flat package
LQFP: low profile quad flat package
MQFP: metric quad flat package
NQFP: near chip-scale quad flat package. ^[3]
SQFP: small quad flat package
TQFP: thin quad flat package
VQFP: very small quad flat package
VTQFP: very thin quad flat package
TDFP: thin dual flat package. ^[4]



QFN Package

Package	
DFN	dual flat no-lead package
DQFN	dual quad flat no-lead package
cDFN	
TDFN	thin dual flat no-lead package
UTDFN	ultra-thin dual flat no-lead package
XDFN	extremely thin dual flat no-lead package
QFN	quad flat no-lead package
QFN-TEP	quad flat no-lead package with top-exposed pad
TQFN	thin quad flat no-lead package
LLP	leadless leadframe package
LPCC	leadless plastic chip carrier
MLF	micro-leadframe
MLPD	micro-leadframe package dual
MLPM	micro-leadframe package micro
MLPQ	micro-leadframe package quad
DRMLF	dual-row micro-leadframe package
VQFN/WQFN	very thin quad flat no-lead
UQFN	ultrathin quad flat no-lead



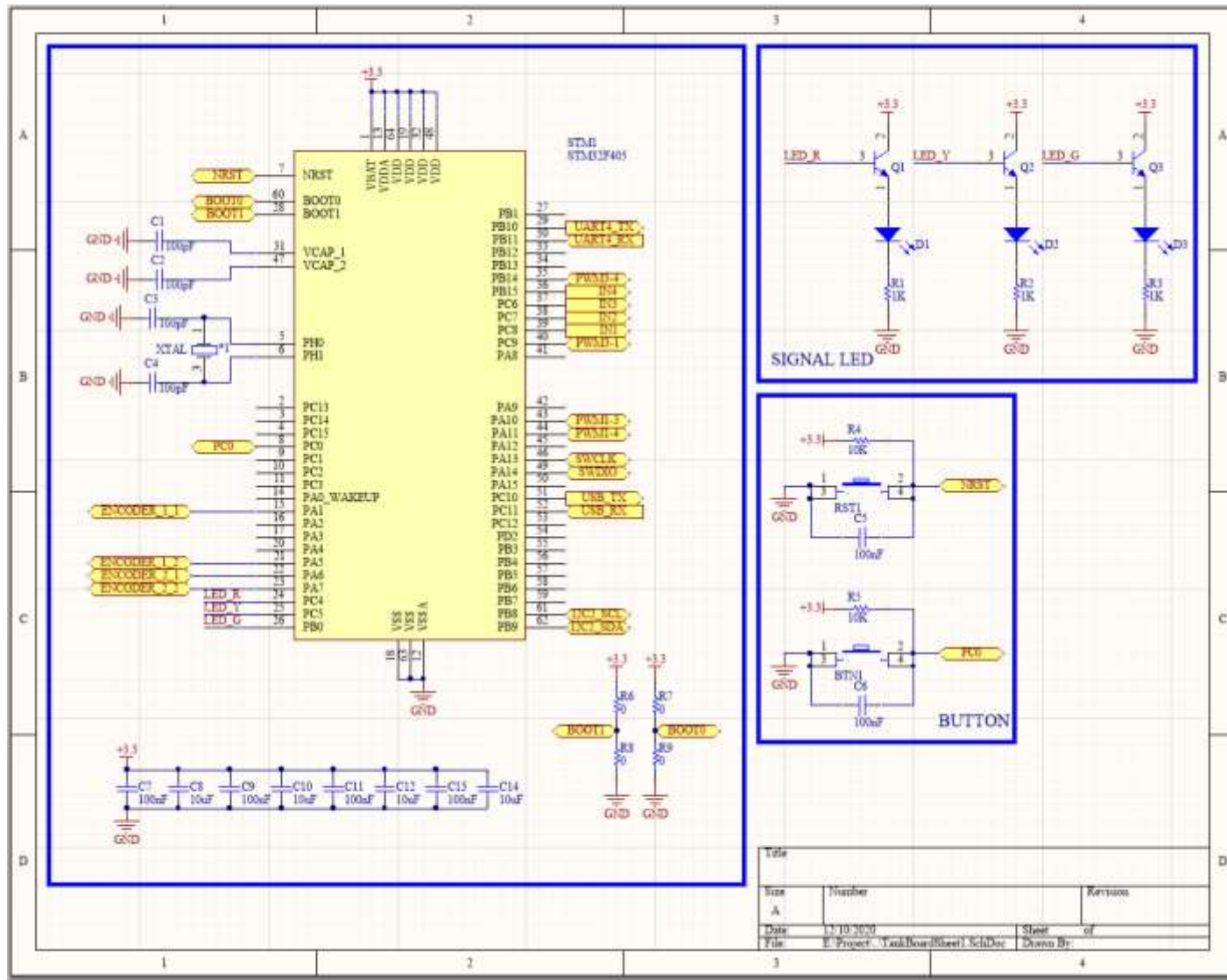
Create Schematic And Design PCB



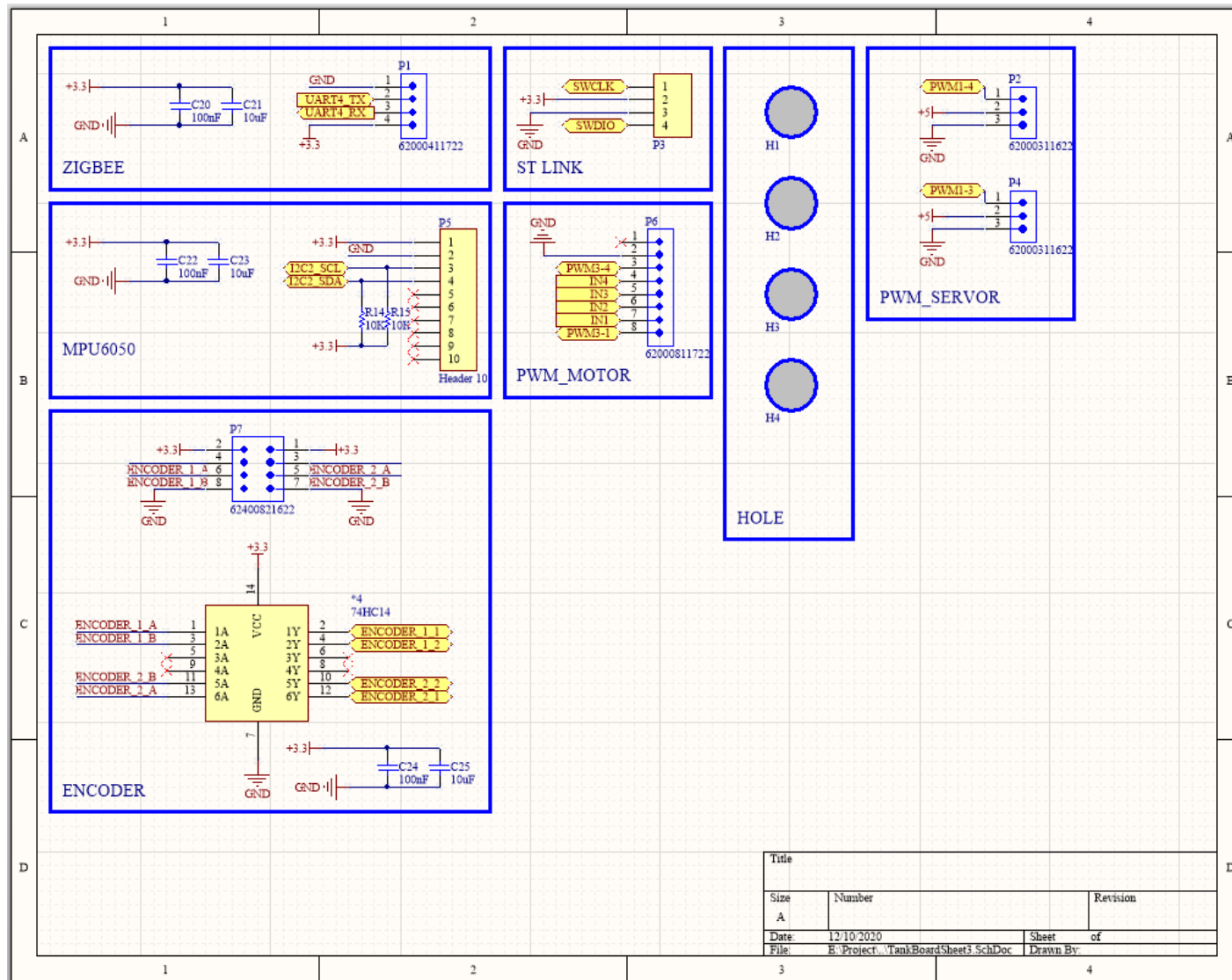
Schematic



Schematic

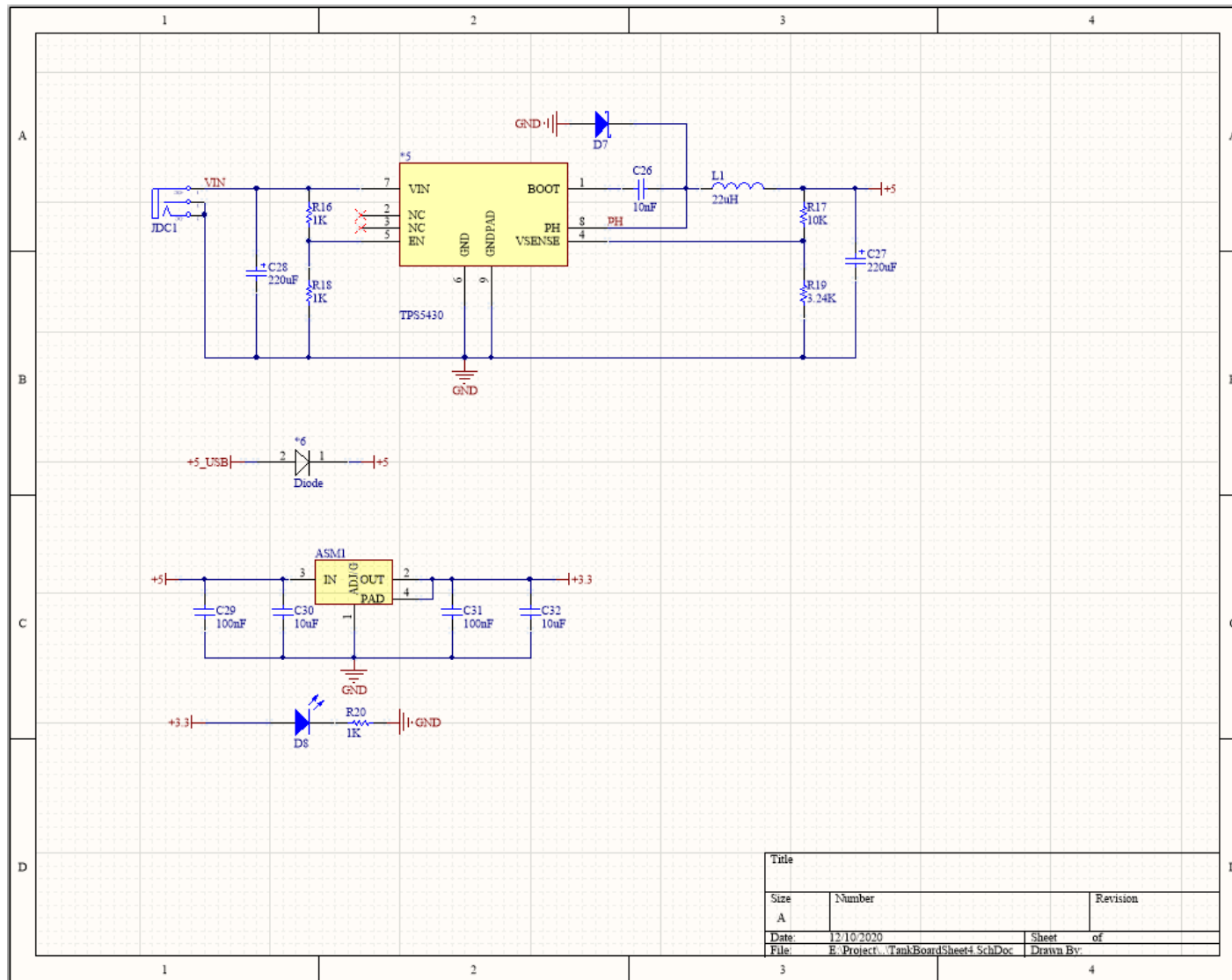


Schematic



Title		
Size	Number	Revision
A		
Date:	12/10/2020	Sheet of
File:	E:\Project\TankBoardSheet3 SchDoc	Drawn By:

Schematic



Title		
Size	Number	Revision
A		
Date:	12/10/2020	Sheet of
File:	E:\Project\TankBoardSheet4 SchDoc	Drawn By:

Basic layout rules



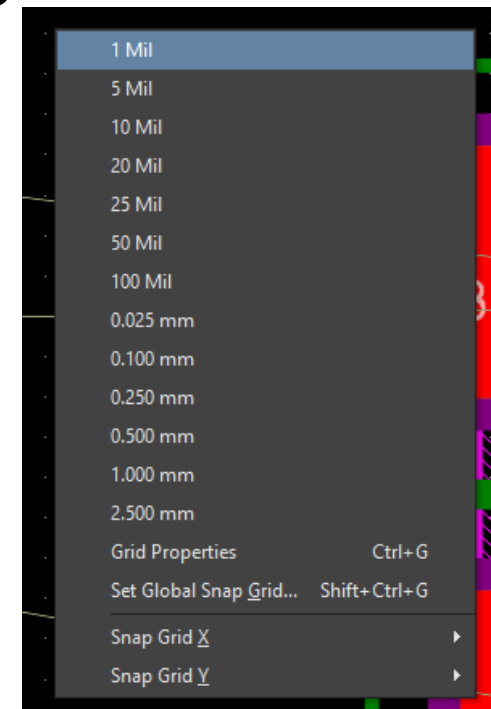
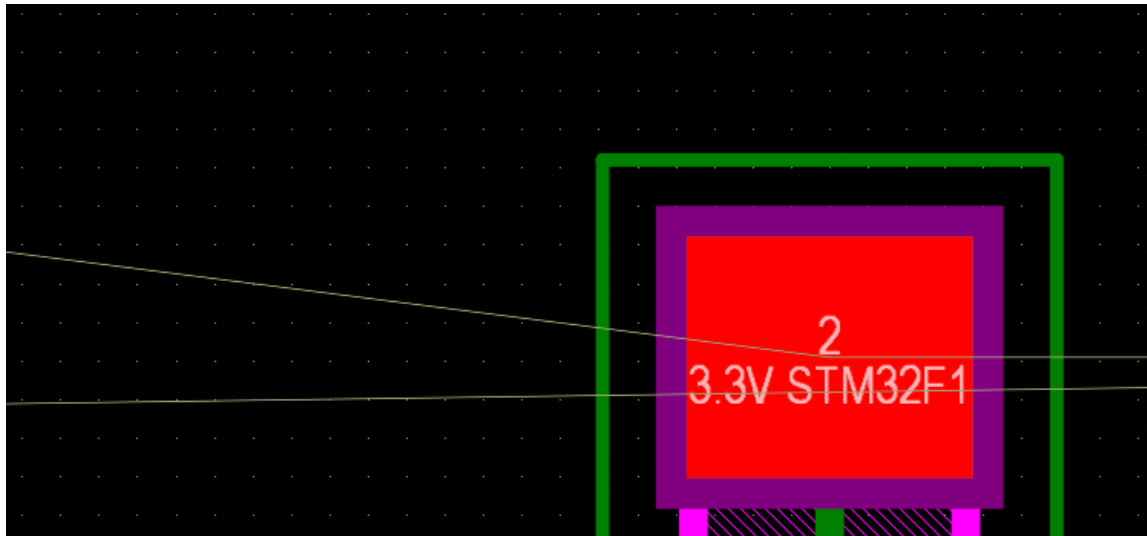
Layout PCB - General

- Luôn luôn imperial units (i.e inches, mil).
- Mil = 1 phần nghìn inch ($1 \text{ mil} = 1/1000''$).
 - 100 mils = 0.1 inch = 2.54 mm
 - 50 mils = 0.05 inch = 1.27 mm
 - 1 “pitch” = 1 inch
- Sử dụng mils cho track, pads, clearance and grids đó là điều cơ bản của “design and layout”.
- Chỉ sử dụng mm cho “mechanical and manufacturing” như lỗ khoan (hole) và kích thước board



Layout PCB – Snap Grid

- Công dụng: để đặt component và track trên fixed grid (lưới cố định).
- Nên để mật độ lưới là 50-25-20-10-5
- Nhớ là đơn vị là mil



Layout PCB - Tracks

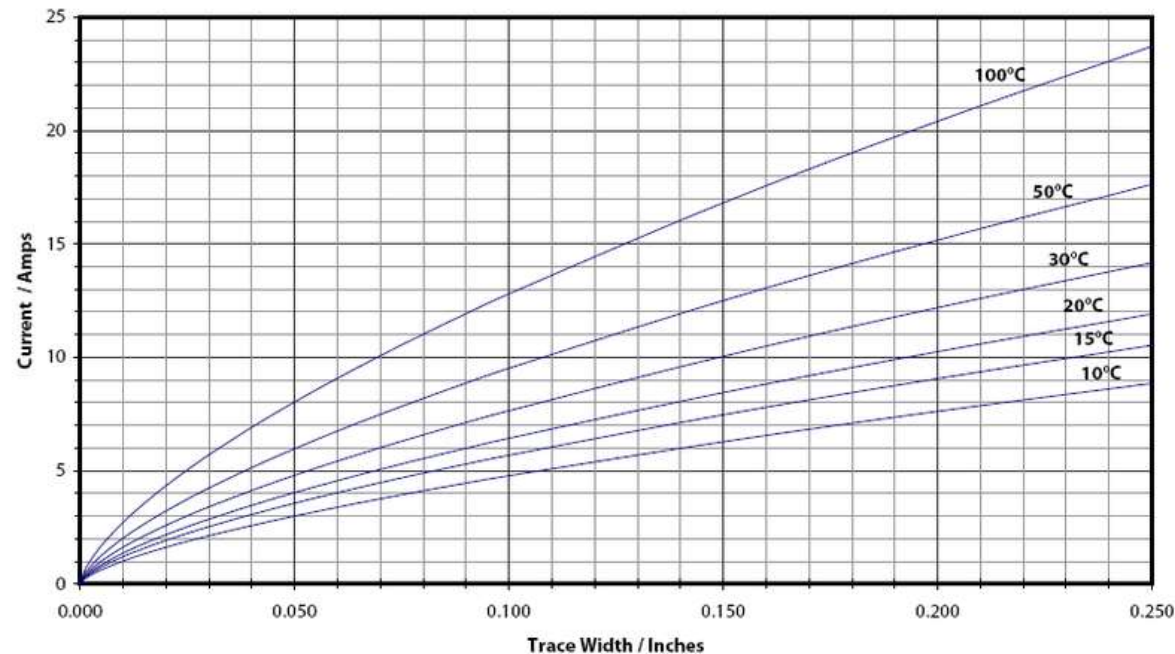
- Kích thước đường dây (tracks) sẽ phụ thuộc vào:
 - Yêu cầu kĩ thuật
 - Đường đi dây
 - Clearance
- Đường dây càng bự càng tốt, nhưng không có nghĩa là tốt nhất.
- Cố gắng giữ đường dây bự hết nhất có thể



Layout PCB – Tracks width

- Tracks width vs current

Trace Current Capacity on 1oz (35um) PCB



IPC Recommended Track Width For 1 oz cooper PCB and 10 °C Temperature Rise

Current/A	Track Width(mil)	Track Width(mm)
1	10	0.25
2	30	0.76
3	50	1.27
4	80	2.03
5	110	2.79
6	150	3.81
7	180	4.57
8	220	5.59
9	260	6.60
10	300	7.62



Layout PCB – Tracks width

- Link: [Printed Circuit Board Trace Width Tool | Advanced Circuits \(4pcb.com\)](http://4pcb.com/Printed-Circuit-Board-Trace-Width-Tool)

Printed Circuit Board Width Tool

This Javascript web calculator calculates the trace width for printed circuit board conductors for a given current using formulas from IPC-2221 (formerly IPC-D-275).

Inputs:

Current	<input type="text" value="2"/>	Amps
Thickness	<input type="text" value="1"/>	oz/ft ² ▼

Optional Inputs:

Temperature Rise	<input type="text" value="10"/>	Deg C ▼
Ambient Temperature	<input type="text" value="25"/>	Deg C ▼
Trace Length	<input type="text" value="1"/>	inch ▼

Results for Internal Layers:

Required Trace Width	<input type="text" value="80.0"/>	mil ▼
Resistance	<input type="text" value="0.00631"/>	Ohms
Voltage Drop	<input type="text" value="0.0126"/>	Volts
Power Loss	<input type="text" value="0.0252"/>	Watts

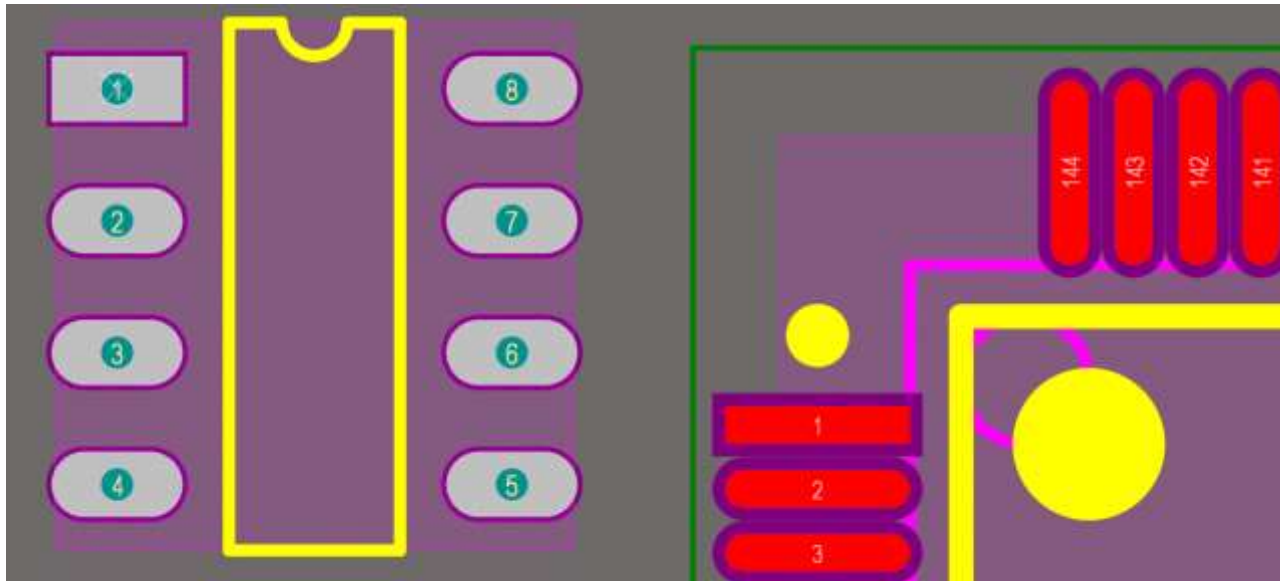
Results for External Layers in Air:

Required Trace Width	<input type="text" value="30.8"/>	mil ▼
Resistance	<input type="text" value="0.0164"/>	Ohms
Voltage Drop	<input type="text" value="0.0328"/>	Volts
Power Loss	<input type="text" value="0.0656"/>	Watts



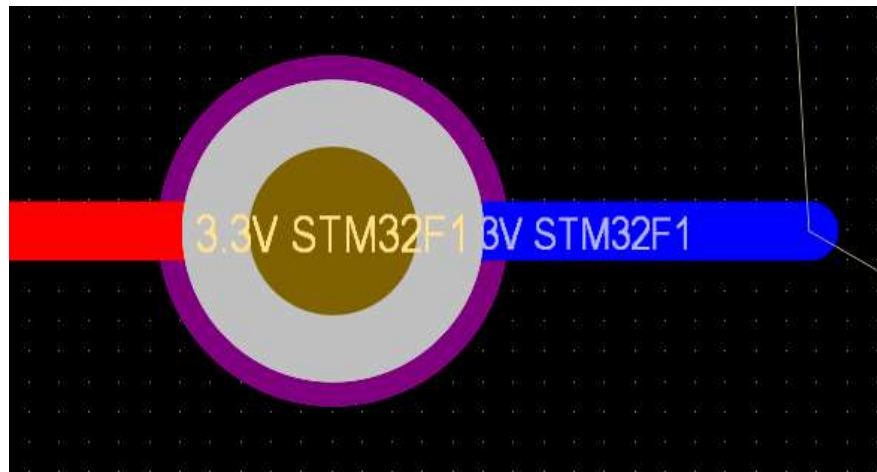
Layout PCB - Pads

- Pad luôn có đường kính lớn hơn đường kính lỗ khoan 1.8 lần hoặc lớn hơn 0.5mm
- Pin 1 luôn có hình dáng khác với các pin còn lại, thường là hình vuông



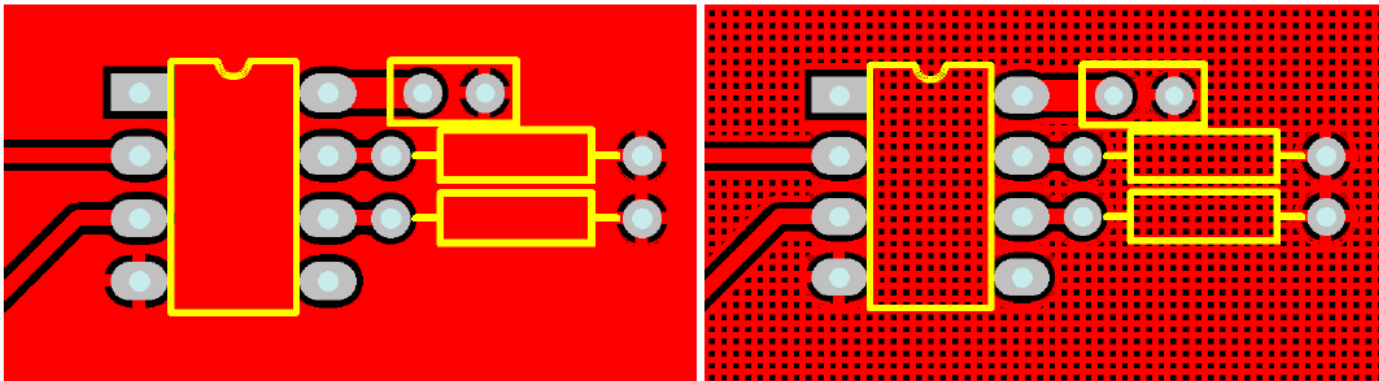
Layout PCB – Vias

- Vias dùng để kết nối dây từ layer này sang layer khác.
- Lỗ vias thường bé hơn pad linh kiện.
- Kích thước via thường ở 0.5-0.7 mm
- Hãy via ít nhất có thể



Layout PCB - Polygon

- Polygon là một lớp phủ đất vào những vị trí chưa có dây đồng.
- Có hai loại polygon là Solid (nguyên khối) và Hatch (lưới)
- Phủ polygon sau khi sắp xếp linh kiện và đi dây.



An example of a “Solid Polygon Fill” (Left), and a “Hatched Polygon Fill” (Right)



Layout PCB - Clearance


- Clearance là khoảng cách giữa các linh kiện, đường dây với nhau.
- Đối với mạch xuyên lỗ thì tối thiểu là 15mils
- Còn đối với SMD thì khoảng 8-10 mil
- Chú ý với những board có điện áp cao



Layout PCB - Clearance

Different Nets Only

Minimum Clearance 6mil



☐ Ignore Pad to Pad clearances within a footprint

☒ Simple ☐ Advanced

	Track	SMD Pad	TH Pad	Via	Copper	Text
Track	6					
SMD Pad	6	6				
TH Pad	6	6	6			
Via	6	6	6	6		
Copper	6	6	6	6	6	
Text	6	6	6	6	6	6
Hole	6	6	6	6	6	6

Required clearances between electrical objects and Board Cutouts / Board Cavities are determined using the largest of Electrical Clearance rule's Region -to- object settings and Board Outline Clearance rule's settings.

Layout PCB - Clearance

Clearances for Electrical Conductors

Voltage (DC or Peak AC)	Internal	External (<3050m)	External (>3050m)
0-15V	0.05mm	0.1mm	0.1mm
16-30V	0.05mm	0.1mm	0.1mm
31-50V	0.1mm	0.6mm	0.6mm
51-100V	0.1mm	0.6mm	1.5mm
101-150V	0.2mm	0.6mm	3.2mm
151-170V	0.2mm	1.25mm	3.2mm
171-250V	0.2mm	1.25mm	6.4mm
251-300V	0.2mm	1.25mm	12.5mm
301-500V	0.25mm	2.5mm	12.5mm

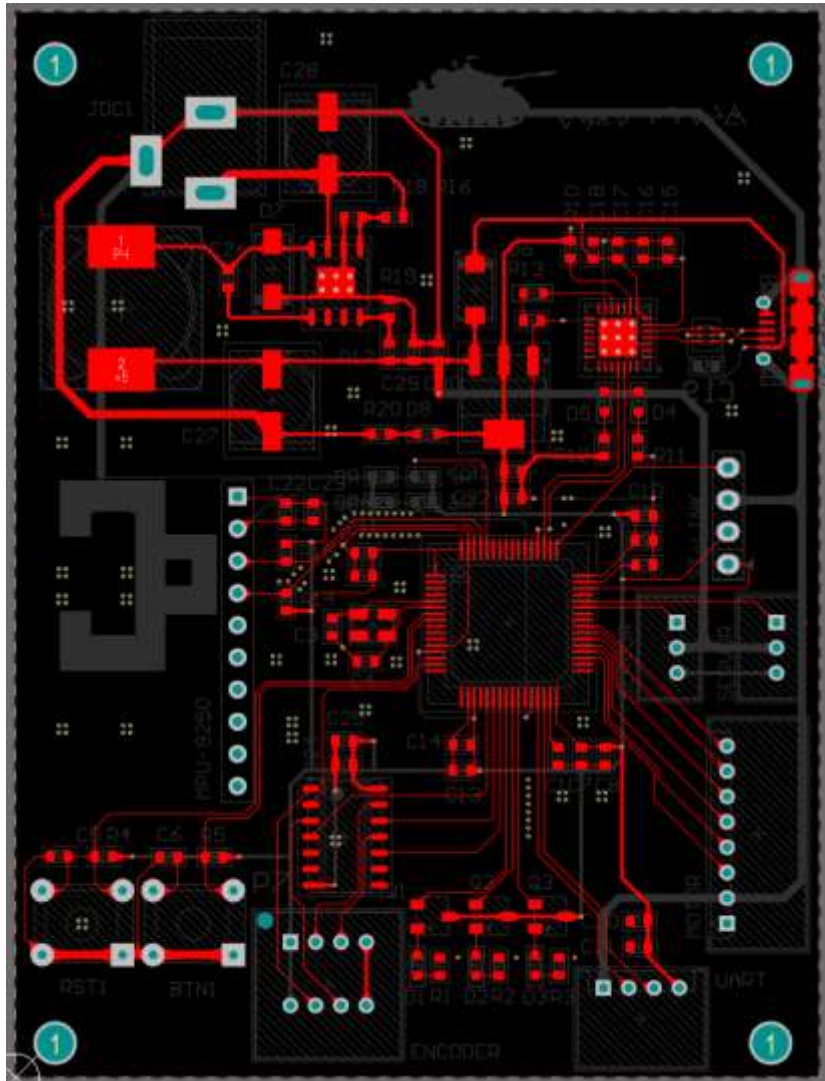


Layout PCB – Component placement

- Nhớ cài đặt grid, track, vias, pad.
- Đặt các linh kiện một cách hợp lí.
- Nên đặt các linh kiện quan trọng trước và đi dây quan trọng trước.
- Sử dụng DRC sau khi vẽ board
- Nhờ ai đó kiểm tra cái board mình vẽ.



Layout PCB – Component placement



- Việc đặt linh kiện hợp lí khiến công việc có hoàn thành gần 90%.

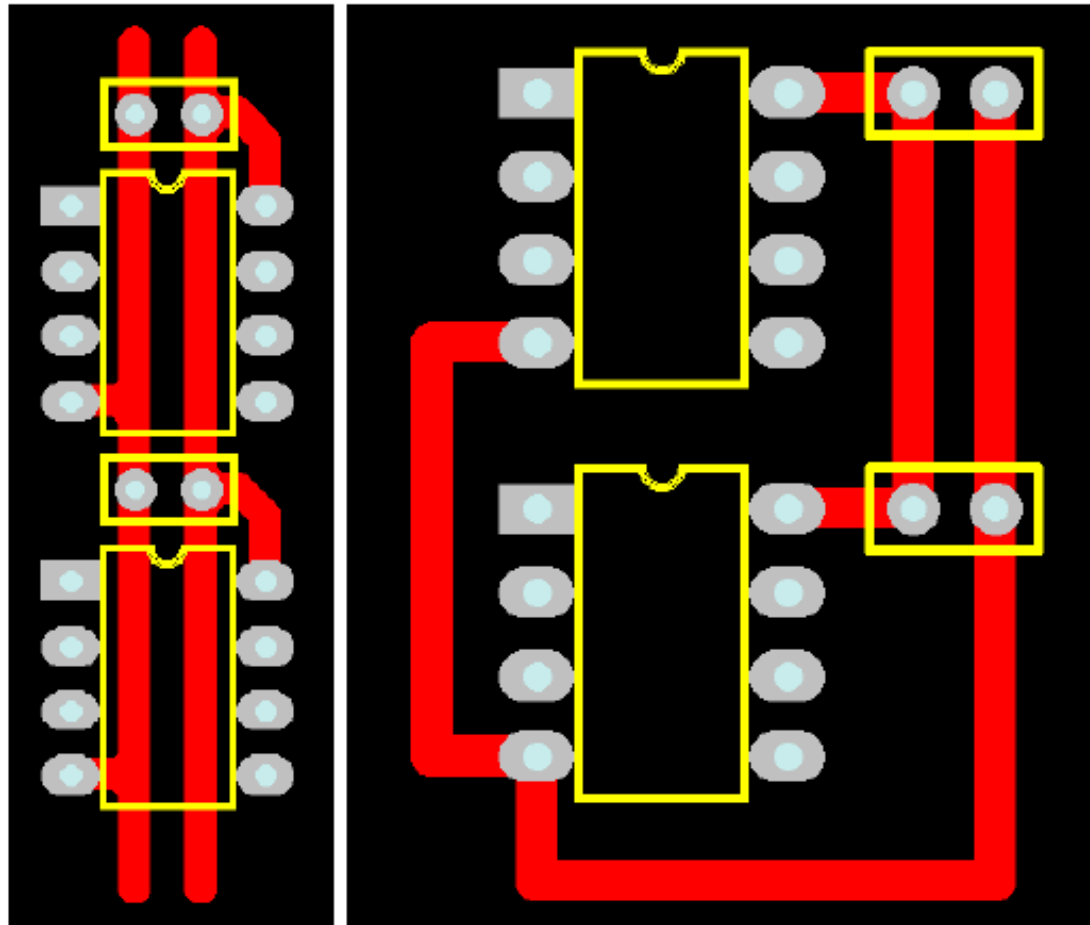


Layout PCB – Basic routing

- Đi track ngắn nhất có thể.
- Nên đi góc 45 độ.
- Luôn đi track tới trung tâm của pad.
- Đối với những dây có cường độ lớn thì nên xài nhiều via khi đổi layer.
- Nên để đường dây nguồn có kích thước lớn nhất có thể.
- Nên để đường dây nguồn và dây đất gần nhau nhất có thể.

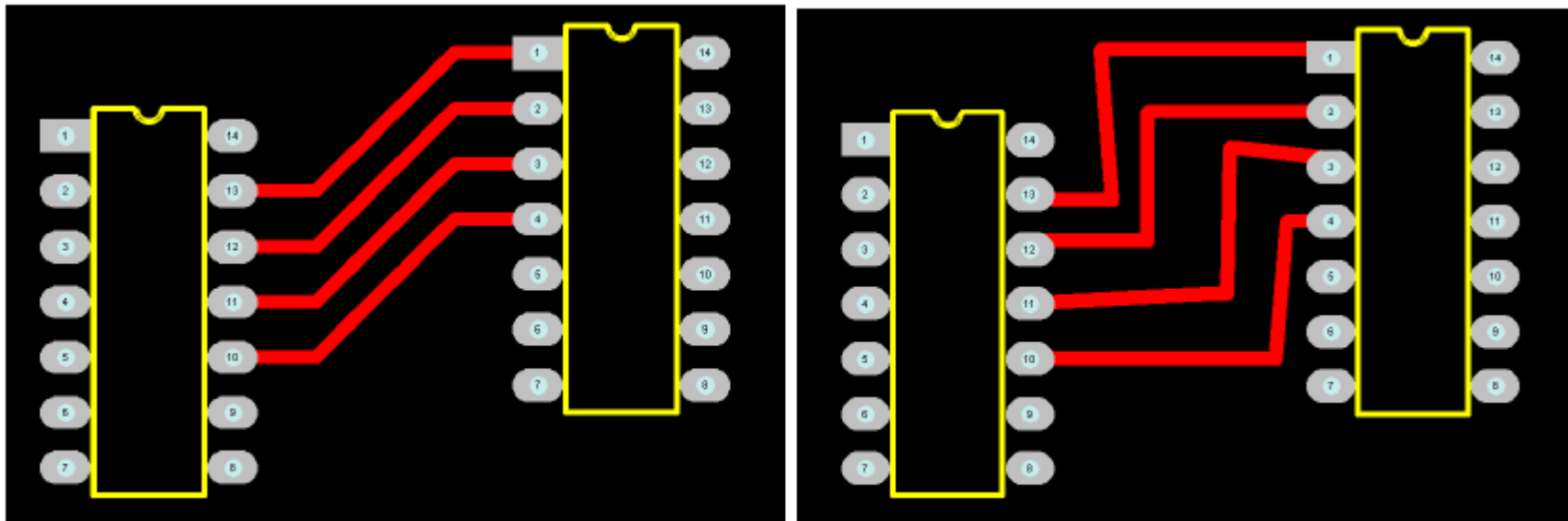


Layout PCB – Basic routing



An example of GOOD power routing (Left) and BAD power routing (Right)

Layout PCB – Basic routing



An example of GOOD routing (Left) and BAD routing (Right)

Lưu ý: không để đường dây / polygon không (dead copper), hãy nối đất hoặc xóa nó ra khỏi layout



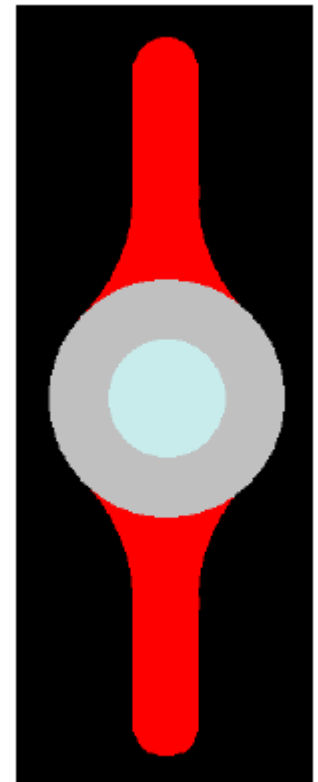
Layout PCB – 2-layer routing

- Không nên đặt via dưới các linh kiện điện tử.
- Hãy via ít nhất có thể.
- Nên xài linh kiện dán (SMD).




Layout PCB – Finishing touches

- Tạo các lỗ khoan để bắt vít trên board khi có nhu cầu gắn board lên.
- Thêm các “teardrops” cho các pad và via



Layout PCB – Auto tools



- Auto route:
 - *“Real PCB designers don’t auto route!”*
- Auto placement:
 - “Professional PCB designers do not use Auto Placement tools. Don’t rely on the Auto Place feature to select the most optimum layout for you. *It will never work!*”



References

- [1] PCB Design Tutorials – David L. Jones



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