NGUYEN THANH TUNG

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OBJECTIVE

Fourth-year Electronics and Telecommunications student with a strong interest in Digital Design. Possesses hands-on experience in digital logic design, FPGA implementation, and system-level verification through academic projects. Seeking an internship opportunity to apply digital design principles and gain practical experience in real-world engineering environments.

EDUCATION

- **Ho Chi Minh City University of Technology (HCMUT), VNU-HCM** *Oct 2022 - present*
  Major: Bachelor of Electronics - Telecommunications Engineering
  - GPA: 3.1/4.0
  - **Project 1:** RISC-V–Based SoC Design with System Bus and Peripherals Integration.
  - **Project 2:** FPGA-Based Multi-Band Audio Equalizer Using Folded FIR Architecture.
  - **Course:** Marvell "IC Design for AI Infrastructure" Training Course.

PROJECTS

- **Project 1: RISC-V–Based SoC Design with System Bus and Peripherals Integration.** *April 2025*
  Tools: Cadence Xcelium/SimVision, Quartus II 13.0 sp1, ModelSim.
  - Designed and implemented a 5-stage pipelined RISC-V (RV32I) processor (IF, ID, EX, MEM, WB) with data forwarding and hazard handling.
  - Implemented branch prediction schemes: static (always-taken/not-taken) and dynamic (2-bit saturating counter, global/local predictors).
  - Integrated TileLink-UL/APB bus with a custom bridge to interface peripherals: SRAM (IS61LV25616), UART, LCD1602, 7-seg LED, watchdog timer.
  - Verified functionality using directed testbenches, synthesized and deployed on Altera DE2-115 FPGA.
- **Project 2: FPGA-Based Multi-Band Audio Equalizer Using Folded FIR Architecture** *November 2025*
  Tools: MATLAB 2025a, Cadence Xcelium/SimVision, Quartus Prime 24.1 and QuestaSim.
  - Designed a multi-band audio equalizer using folded FIR filters, including low-pass, band-pass and high-pass filters.
  - Generated FIR coefficients in MATLAB using the Hamming window method at a 48 kHz sampling rate.
  - Verified filter performance using multi-tone sine inputs and FFT spectrum analysis in MATLAB.
  - Implemented the design on Altera DE10-Standard FPGA and interfaced with WM8731 audio codec (ADC/DAC), validated using an oscilloscope.
- **Other Project:** *2024 - 2025*
  Tools: MATLAB 2025a, Cadence Xcelium/SimVision/Genus/Virtuoso, Quartus Prime 24.1 and QuestaSim.
  - Designed & implemented multi-waveform generator (sine, square, triangle, sawtooth, ECG, noise) on DE10 Standard FPGA; verified via oscilloscope.
  - Designed & implemented a single-precision floating-point adder/subtractor compliant with IEEE 754.
  - Verification of single-precision floating-point 8-Point Radix-2 FFT Core.
  - Designed CMOS logic gates and combinational circuits in FreePDK45, including full adders and decoders, with DRC/LVS-clean layouts.
  - Analyzed 6T SRAM cell and 8×8 SRAM array with decoder and sense amplifier; verified read/write stability and timing through circuit-level simulation.

TECHNICAL SKILLS

- **HDL:** Verilog and SystemVerilog
- **Computer Architecture:** RISC-V, Pipeline, Branch Prediction, Bus Protocols
- **FPGA:** Quartus, ModelSim/QuestaSim, DE2-115, DE10-Standard
- **EDA Tools:** Cadence Xcelium, Virtuoso, Genus, MATLAB, WaveDrom
- **Programming Language:** C, Assembly (AVR, RV32I), Bash, Makefile
- **OS & Documentation:** Experienced with Linux (Ubuntu, CentOS), LaTeX

LANGUAGE

- ENGLISH: TOEIC L/R 620