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Improving Adder Efficiency Through Prefix Parallelism

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ABSTRACT

The adder is one of the most critical components in digital systems, as it is used extensively in arithmetic logic units and data paths. Fast adders are essential for high-performance computing. The Brent-Kung adder is a parallel prefix form adder known for its high-speed and low-complexity design. This paper presents the implementation and performance analysis of a Verilog-based 8-bit Brent-Kung prefix form adder. The adder is coded in Verilog Hardware Description Language and simulated using the Vivado tool. The functionality of the designed adder is verified by exhaustive simulation of various input combinations. Timing analysis is performed by observing the waveforms to calculate the delay. The synthesized netlist is analyzed to estimate area and power utilization. Results show that the Brent-Kung adder provides reduced delay compared to ripple-carry adders, with a modest increase in area and power. The parallel prefix structure and optimized carry generation logic enable fast carry propagation in the Brent-Kung adder. Detailed analysis of the simulation waveforms provides insight into the worst-case delay scenario, which determines the maximum operating frequency. The performance metrics obtained from this study will serve as a benchmark for comparing different adder architectures. The Verilog modeling approach enables the reuse of the design and integration into larger systems. Overall, this paper demonstrates an effective performance analysis methodology for fast adders using Verilog simulation.

Keywords: Adder, Carry-lookahead adder, Brent Kung adder, Verilog VHDL.

I. INTRODUCTION

In the realm of electronics, all information is typically encoded using binary digits or bits. The instructions responsible for manipulating this data are also expressed in the form of bits. To handle these data and instructions effectively within an electronic system, the use of a binary adder is imperative. The critical requirement for such an adder is its ability to operate swiftly. Similar to the base-10 number system, binary addition conventionally involves adding numbers, necessitating the use of a carry bit from the previous position to determine the correct sum bit at the corresponding location.

However, as the size of data and instructions in the current standard continues to grow, the speed of conventional binary addition becomes a significant challenge. This limitation has led to the development and patenting of various adder architectures aimed at overcoming this speed impediment. One notable architecture in this regard is the Brent-Kung adder (BKA).

This paper focuses on the Brent-Kung adder, discussing its significance as an alternative adder architecture. The BKA addresses the speed challenge posed by the expanding size of data and instructions, offering a solution that optimizes the process of binary addition. Through an exploration of its design and functionality, the project aims to shed light on the effectiveness of the Brent-Kung adder in meeting the high-speed requirements of modern electronic systems.

The Brent-Kung adder (BKA) is recognized as a parallel prefix form of the Carry-Lookahead Adder (CLA). Its architectural advantages include minimized wiring congestion and a reduced chip area requirement for implementation. Moreover, the design incorporates abundant branching and depth of logic. The Brent-Kung adder exhibits up to three fan-outs and five depth levels to calculate eight carry outputs. This characteristic results in a comparatively slower operation when compared to the Kogge-Stone Adder (KSA). However, the intentional trade-off is that the BKA is designed to be cost-effective and straightforward to manufacture, necessitating less hardware than the KSA.

II. LITERATURE SURVEY

[1] M. Basir, R. Ismail, S. Naziri, M. Isa, S. Murad, and A. Harun, "Speed and Area Efficient FXP Adders and Multipliers: A Comparative Analysis for LNS System,", Designing an efficient digital signal processing (DSP) architecture is crucial for advanced computations in fields like time-varying signal processing, image processing, and machine vision. Combining Fixed-Point (FXP) for addition and subtraction with Logarithmic Number System (LNS) for multiplication and division significantly improves accuracy and speed, though LNS operations involving non-linear functions may increase computation time. Implementation of a Carry Look-Ahead Adder (CLA) and Parallel Prefix Adders (PPAs) like Brent Kung (BK), Kogge Stone (KS), and Ladner Fisher (LF) enhance both speed and area efficiency. Functional verification, including rigorous testing of each module with comprehensive test benches in synthesizable design tools like Quartus II, ensures reliability. Comparative studies highlight LF adders and modified Baugh Wooley multipliers for their low latency and reduced silicon area, crucial for high-speed data processing and compact microprocessor designs utilizing the proposed LNS approach. [2] K. Rahila and U. S. Kumar, "A comprehensive comparative analysis of parallel prefix adders for ASIC implementation,", This paper presents a comprehensive comparative analysis of different parallel prefix adders like Kogge-Stone, Ladner-Fischer, Brent-Kung, and Sklansky for ASIC implementation. The comparative study analyzes the area, delay, power, and area-delay product metrics for adder widths from 16 to 1024 bits. The results show that the Kogge-Stone adder has the minimum delay but requires a larger area and power. Brent-Kung adder has the lowest area excluding ripple carry adder. For small adder widths, Kogge-

Stone has a minimum area-delay product but for medium to large widths, Brent-Kung has the best area-delay product. Overall, the study provides insights into selecting the optimal adder topology based on design parameters for ASIC implementation.

III.EXISTING METHODOLOGY

Ripple Carry Adder: A popular digital circuit used in computers to add binary integers is the ripple carry adder. Although it is a simple and effective method of adding, it is not without restrictions. One bit at a time additions are made using the ripple carry adder, which transfers any excess bits to the following stage. Because of the carry propagation delay, this method can be slow when adding larger numbers, while being straightforward and easy to use. On the other hand, the ripple carry adder is a dependable and affordable option for smaller calculations.

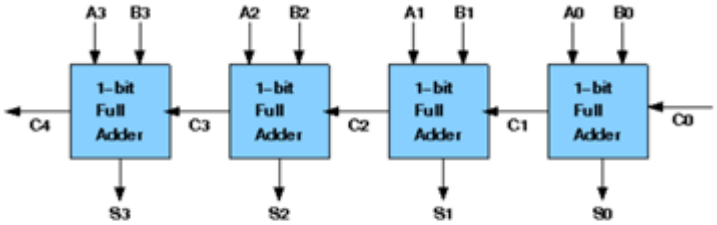

Fig 1: Block diagram of 4-bit Ripple Carry Adder

The 4-bit ripple carry adder is implemented by using four 1-bit full adders connected in series. Each full adder has inputs A, B, and Cin which produce outputs Sum and Cout. The Cout of each adder is connected to the Cin of the next adder to propagate the carry through the chain. The first adder takes A[0] and B[0] as inputs, while the last adder outputs the final Cout. The Sum outputs of each adder produce the 4-bit total sum.

Carry-Look Ahead Adder: carry-look-ahead adder is a type of digital circuit used in computer processors to quickly add together binary numbers. Unlike traditional adders that calculate each bit one at a time, a carry-look-ahead adder can generate the carry signals for multiple bits simultaneously, speeding up the addition process significantly. This is achieved through a clever combination of logic gates that allow for parallel computation of carry bits. By predicting and propagating carry signals ahead of time, the carry-look-ahead adder reduces the overall time needed to perform addition operations, making it a crucial component in modern high-speed computing systems.

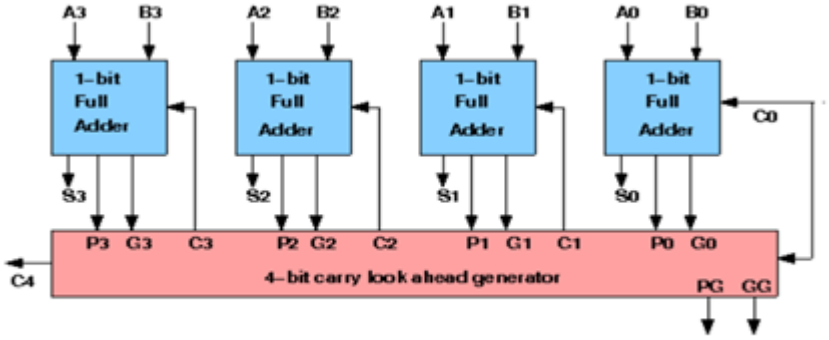

Fig 2: Block Diagram of 4 bit Carry-Look

IV. PROPOSED METHODOLOGY

This paper demonstrates the 8 bit Brent-Kung adder. Brent-Kung adder is famous for its effective performance in terms of speed and area usage. This is because the Brent-Kung adder employs a more intricate structure that minimizes the number of logic levels required to generate the sum and execute signals, enabling faster arithmetic computations. On the other hand, to expedite the addition process, the carry-look-ahead adder depends on producing carry signals beforehand. Despite this, the carry-look-ahead adder is utilized in more general-purpose scenarios because of its simplicity and ease of use, while the Brent-Kung adder is frequently chosen in high-performance applications where speed is critical.

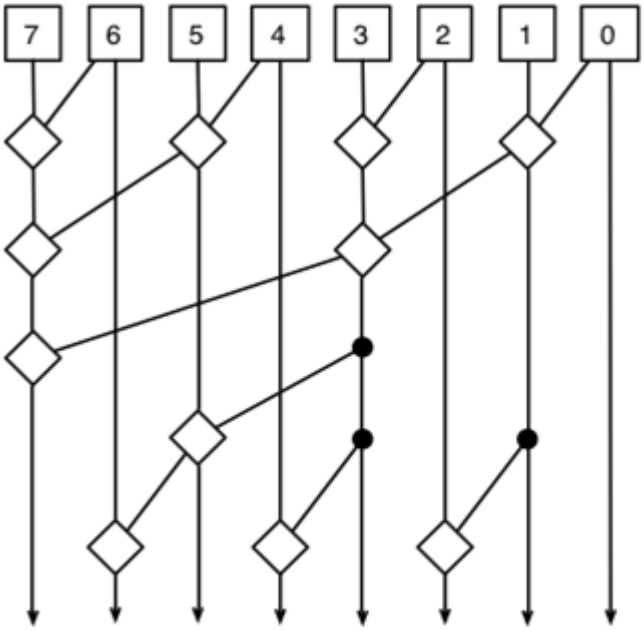

Fig 3: Block diagram of 8 bit Brent-kung adder

V. RESULT AND DISCUSSION

The code is written using Verilog and VHDL at the behavioral level within the Vivado IDE software. The Brent Kung adder, an 8-bit module, functions by adding two 8-bit binary numbers (A and B) as inputs. Initially, A and B are simultaneously added through a carry-save mechanism, producing intermediate results known as sum bits (S) and carry-out bits (C). Following the carry-save addition, a carry-propagate step drives the carry bits forward to derive the final sum. The outputs from the carry-save phase are channeled into a series of adders arranged in a tree structure. This method efficiently carries the carries across multiple levels, reducing the delay significantly compared to ripple carry adders. In the Brent-Kung adder, the carry-propagate phase is executed through a binary tree design with specific connections to minimize the tree's levels, enhancing performance. Concluding the carry-propagate step, the final sum bits (S) signify the outcome of the summation operation.

Fig 4: Output of Brent-kung adder when the A=10101110, B=01101001 and c=0

VI. CONCLUSION

Using Vivado software, we analyzed various designs, revealing significant improvements in speed and resource utilization compared to traditional adder architectures.This demonstrates the effectiveness of employing prefix parallelism methods to improve adder circuit efficiency. By strategically applying prefix parallelism, critical path delays were mitigated, and propagation times within the adder circuitry were minimized, leading to accelerated arithmetic operations. Additionally, optimized resource allocation facilitated more efficient FPGA resource utilization, particularly beneficial for applications requiring rapid arithmetic computations in resource-constrained environments. Furthermore, the project provided valuable insights into design considerations and trade-offs inherent in implementing prefix parallelism techniques, laying a foundation for future research in digital circuit design. In conclusion, the integration of prefix parallelism into adder circuits using Vivado software offers promise for enhancing the performance and efficiency of digital systems, with implications for signal processing, cryptography, and data-intensive computations, fostering transformative developments in these fields.

VII. REFERENCES

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