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VIRTUAL LAB REPORT

COURSE: Linear Integrated Circuits

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Characteristics and Parameters of Op-Amp

Aim: To study and measure the characteristics and parameters of an Op-amp (IC-741):

(a) Input bias current at inverting terminal

(b) Input bias current at non-inverting terminal

(c) Input offset current

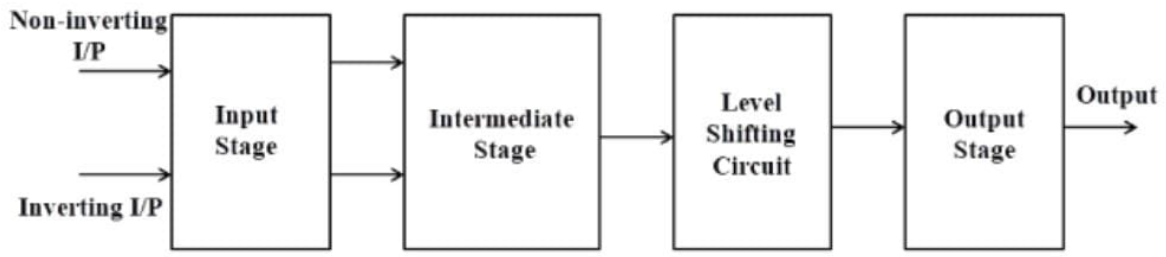
(d) Input offset voltage

(e) Slew rate

Theory: An operational amplifier is a direct coupled high gain amplifier usually consisting of one or more differential amplifiers and followed by a level translator and an output stage. The output stage is generally a push-pull or push-pull complementary-symmetry pair. An operational amplifier is available as a single integrated circuit package.

The operational amplifier is a versatile device that can be used to amplify dc as well as ac input signals and was originally designed for performing mathematical operations such as addition, subtraction, multiplication and integration. Thus, the word operational amplifier stems for its original use for these mathematical operations and is abbreviated to op-amp. With the addition of suitable external feedback components, the modern day op-amp can be used for a variety of applications, such as ac and dc signal amplification, active filters, oscillators, comparators, regulators and others.

Since an op-amp is a multistage amplifier, it can be represented by a block diagram as shown in Fig. 1.



The input stage is the dual input, balanced-output differential amplifier. This stage generally provides most of the voltage gain of an amplifier and also establishes the input resistance of

the op-amp. The intermediate stage is usually another differential amplifier, which is driven by the output of the first stage. In most amplifiers the intermediate stage is the dual input, unbalanced (single-ended) output. Because direct coupling is used, the dc voltage at the output of the intermediate stage is well above ground potential. Therefore, generally, the level translator (shifting) circuit is used after the intermediate stage to shift the dc level at the output of the intermediate stage downward to zero volts with respect to ground. The final stage is usually a push-pull complementary amplifier output stage. The output stage increases the output voltage swing and raises the current supplying capability of the op-amp. A well-designed output stage also provides low output resistance.

Schematic symbol:

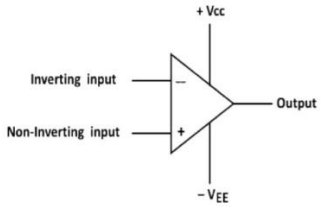


Fig-2: Schematic symbol of op-amp

The input differential amplifier stage of the op-amp is designed to be operated in the differential mode, the differential inputs are designated by the (+) and (-) notations. The (+) input is the non-inverting input. An ac signal (or dc voltage) applied to this input produces an in-phase (or same polarity) signal at the output. On the other hand, the (-) input is the inverting input because an ac signal (or dc voltage) applied to this input produces a 180° out of phase (or opposite polarity) signal at the output.

Characteristics of an ideal op-amp:

An ideal op-amp would exhibit the following electrical characteristics:

• Infinite voltage gain A.

• Infinite input resistance Ri, so that almost any signal source can drive it and there is no loading of the preceding stage.

• Zero output resistance Ro, so that the output can drive an infinite number of other devices.

• Zero output voltage when input voltage is zero.

• Infinite bandwidth, so that any frequency signal from 0 to ∞ Hz can be amplified without attenuation.

• Infinite common-mode rejection ratio (CMRR), so that the output common mode noise voltage is zero.

• Infinite slew rate, so that output voltage changes occur simultaneously with input voltage changes.

Parameters of an op-amp

Input offset voltage

Input offset voltage is the voltage that must be applied between the two input terminals of an op-amp to null the output as shown in Fig.3. In figure Vdc1 and Vdc2 are dc voltages and Rs represents the source resistance. We denote input offset voltage by Vio. This voltage Vio could be positive or negative. For a 741C, the maximum value of Vio is 6mV dc. The smaller the value of Vio, the better the input terminals are matched. For instance, the 741C precision op-amps has maximum Vio= 150μV.

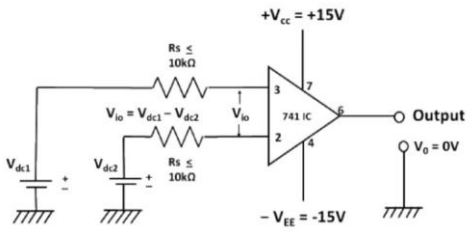


Fig-3: Input offset voltage V_{io}

Input offset current

The algebraic difference between the currents into the inverting and non-inverting terminals is known as input offset current Iio(Fig. 4). In the form of an equation,

Iio = |IB1 - IB2|

where IB1 is the current into the non-inverting input and IB2 is the current into the inverting input. The input offset current for the 741C is maximum 200nA . As the matching between two input terminals is improved, the difference between IB1and IB2 becomes smaller; i.e. the Iio value decreases further. For instance, the precision op-amp 741C has a maximum value of lio equal to 6nA, a dramatic improvement over older technology.

technology.

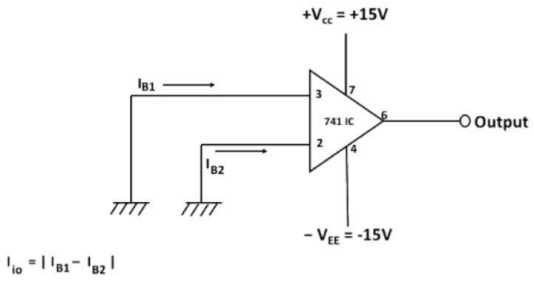


Fig-4: Input offset current I_{io}

Input bias current

Input bias current IB, is the average of the currents that flow into the inverting and non-inverting input terminals of the op-amp. In the form of an equation,

IB = (IB1+ IB2)/2

IB = 500nA (maximum) for 741C, whereas for the precision 741C, it is ±7nA. The two input currents IB1 and IB2 are actually the base currents of the first differential amplifier stage.

Common mode rejection ratio:

The common-mode rejection ratio (CMRR) is defined as the ratio of differential voltage gain Ad to the common mode voltage gain Acm i.e,

CMRR =Ad/ Acm

The differential voltage gain Ad is same as the large-signal voltage gain A, however, the common-mode voltage gain can be determined from the circuit of Fig. 5 as

Acm =Vocm /Vcm

where -

Vocm = output common mode voltage

Vcm = input common mode voltage

Acm = common mode voltage gain

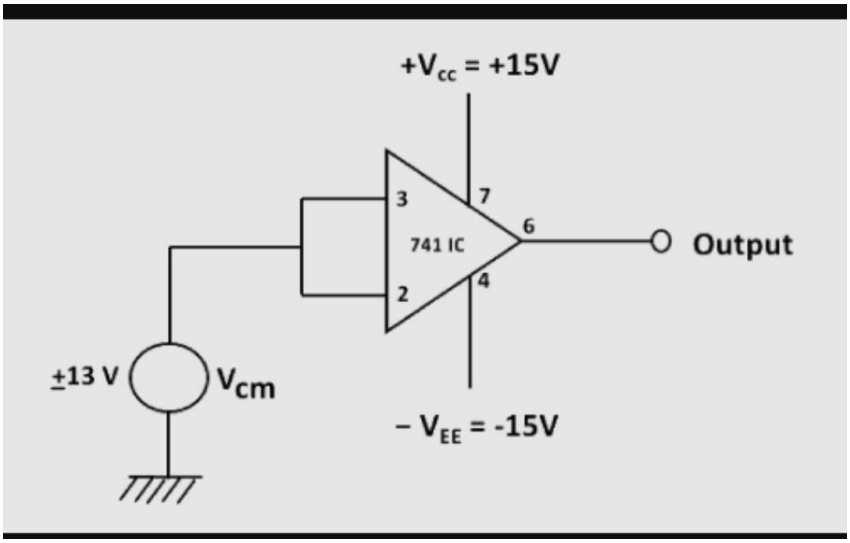


Fig-5: Common mode circuit

Generally, the Acm is very small and Ad = A is very large; therefore, the CMRR is very large. Being a very large value, the CMRR is most often expressed in decibels(dB). For the 741C,CMRR is typically 90dB. This value of CMRR is determined under the test condition that the input source resistance Rs<10KΩ. In Fig.5 Rs is assumed to be zero because most of the practical voltage sources have negligible source resistances.

The higher the value of CMRR, the better is the matching between the two input terminals and the smaller is the output common mode voltage. For the 741C precision op-amp, CMRR =120dB. This means that the precision 741C has a better ability to reject common-mode voltages, such as electrical noise, than the 741C and is preferred in noise environments.

Slew rate

Slew Rate (SR) is defined as the maximum rate of change of output voltage and is expressed in volts per micro-seconds

SR= (dVo /dt)max V/μs,

Slew rate indicates how rapidly the output of an op-amp can change in response to changes in the input frequency. The slew rate changes with change in voltage gain and is normally specified at unity (+1) gain. The slew rate of an op-amp is fixed; therefore, if the slope requirements of the output signal are greater than the slew rate, distortion occurs. The slew rate is one of the important factors in selecting the op-amp for ac applications, particularly at relatively high frequencies.

One of the drawbacks of the 741C is its low slew rate (0.5V/µs), which limits its use in relatively high frequency applications, especially in oscillators, comparators and filters. The newer op-amps: LF351, µAF771 and MC 34001 which are direct replacements for 741, have a slew rate of 13V/µs. In high speed op-amps, especially, the slew rate is significantly improved. For instance, the LM318 has a slew rate of 70V/µs.

Op-amp IC-741 pin configuration

The pin configuration of IC-741 general purpose operational amplifier is shown in Fig. 6. The reference point of the chip is the notch at the top. The pins are numbered in a counter clockwise direction, starting at the notch.

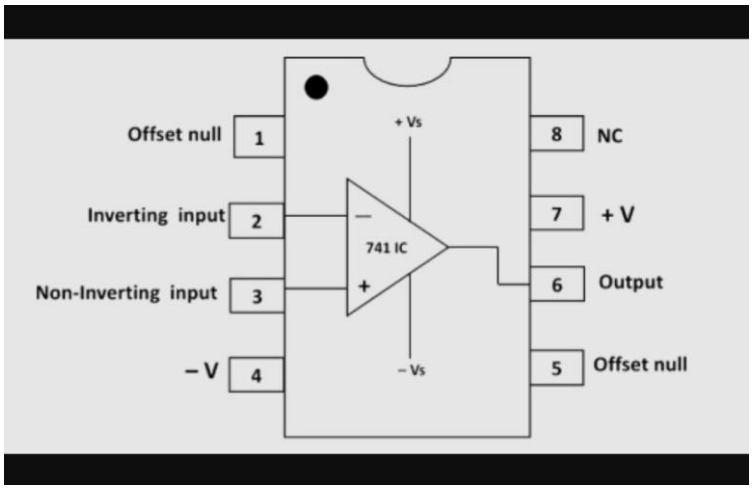


Fig-6: Pin diagram of op-amp IC-741

➢ Pin 1 and Pin 5 are offset null pins. Offset null is a calibration feature of the op-amp. The op-amp is so sensitive to the input voltage that at times, the output will generate a signal even when there is no intentional input. To avoid this condition for certain applications, offset null pins are provided. They are usually connected to a variable resistance such as a potentiometer. The potentiometer can be adjusted to produce a zero-output voltage from Pin 6.

➢ Pin 2 and Pin 3 are two input pins. Both inputs, pin 2 and pin 3, generate an output at Pin 6, but they generate opposite polarities. Pin 2 is the inverting input. Any signal applied to Pin 2 generates a signal of opposite polarity at the output. The non-inverting input, Pin 3, generates an output of the same polarity at Pin 6.

➢ Power to the op-amp is provided through Pin 4 and Pin 7. Pin 4 is either connected to ground or a negative voltage value from 3 to 18 volts. Pin 7 is connected to the positive voltage of the power supply.

➢ The output of the amplifier is at Pin 6.

➢ Pin 8 is not used. 'NC' stands for no connection.

Procedure:

A. Measurement of Input Bias Current IB

(a) Measurement of inverting bias current IB1

1. Click on the components button to place the component on the table.

2. Make connections as per the circuit diagram or connection table.

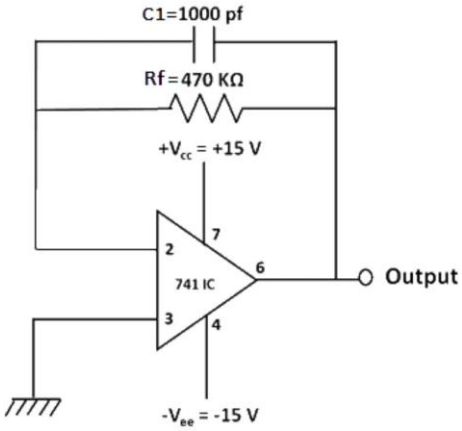


Fig 2: Circuit diagram to measure inverting bias current.

Table 1: Connection table to measure inverting bias current.

S. No.	Source	Target
1	IC741_ pin 07	Supply VCC
2	IC741_ pin 03	Supply GND
3	Multimeter _GND	Supply GND
4	IC741_ pin 04	Supply VEE
5	IC741 _ pin 02	Resistance (R_f) _ terminal C1
6	IC741_ pin 06	Resistance (R_f) _ terminal A1
7	IC741_ pin 02	Capacitance (C_1) _ terminal C1
8	IC741_ pin 06	Capacitance (C_1) _ terminal A1
9	Multimeter_VCC	IC741_ pin 06

3. Click on 'Check Connection' button to check connections. If correct, Click on 'Show output voltage' button to view output on DMM.

4. Calculate the inverting bias current using the formula:

IB1 = Vo/Rf

5. Click on 'Result' button and enter the calculated value.

6. Click on 'Reset' button and proceed in the same way to calculate the input bias current at non-inverting terminal.

b) Measurement of non-inverting bias current IB2

1. Click on the components button to place the component on the table.

2. Make connections as per the circuit diagram or connection table.

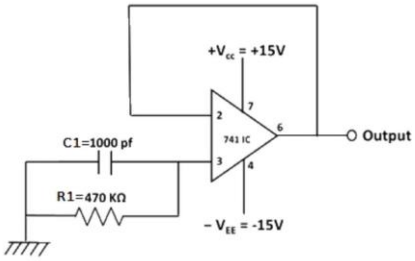


Fig 3: Circuit diagram to measure non-inverting bias current.

Table 2: Connection table to measure non-inverting bias current.

S. No.	Source	Target
1	IC741_ pin 07	Supply VCC
2	Multimeter_GND	Supply GND
3	IC741_ pin 06	IC741_ pin 02
4	IC741_ pin 04	Supply VEE
5	IC741_ pin 03	Resistance (R_1) _terminal C1
6	Supply GND	Resistance (R_1) _terminal A1
7	IC741_ pin 03	Capacitance (C_1) _terminal C1
8	Supply GND	Capacitance (C_1) _terminal A1
9	Multimeter_VCC	IC741_ pin 06

3. Click on 'Check Connection' button to check connections. If correct, Click on 'Show output voltage' button to view output on DMM.

4. Calculate the non-inverting bias current using the formula:

IB2 = Vo/R1

5. Click on 'Result' button and enter the calculated value.

6. The input bias current IB hence, can be calculated using the formula:

IB = (IB1 + IB2)/2

where, IB1 has to be calculated from previous part.

B. Measurement of input offset current Iio

1. Click on the components button to place the component on the table.

2. Make connections as per the circuit diagram or connection table.

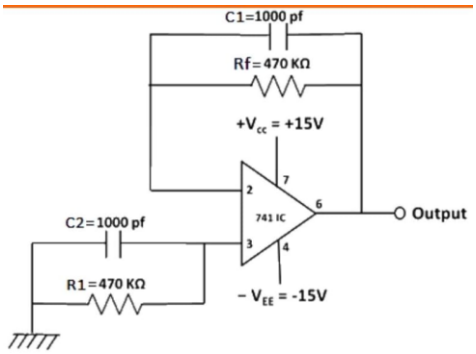


Fig 4: Circuit diagram to measure input offset current.

Table 3: Connection table to measure input offset current.

S. No.	Source	Target
1	IC741_ pin 07	Supply VCC
2	Multimeter_GND	Supply GND
3	IC741_ pin 04	Supply VEE
4	Resistance (R_f)_terminal A1	IC741_ pin 02
5	Resistance (R_f)_terminal C1	IC741_ pin 06
6	Capacitance (C_1) _terminal A1	IC741_ pin 02
7	Capacitance (C_1) _terminal C1	IC741_ pin 06
8	Resistance (R_1) _ terminal A1	IC741_ pin 03
9	Resistance (R_1) _ terminal C1	Supply GND
10	Capacitance (C_2) _terminal A1	IC741_ pin 03
11	Capacitance (C_2) _terminal C1	Supply GND
12	Multimeter_VCC	IC741_ pin 06

3. Click on 'Check Connection' button to check connections. If correct, Click on 'Show output voltage' button to view output on DMM.

4. Calculate the input offset current using the formula:

Iio = Vo/Rf

5. Click on 'Result' button and enter the calculated value.

C. Measurement of input offset voltage Vio

1. Click on the components button to place the component on the table.

2. Make connections as per the circuit diagram or connection table.

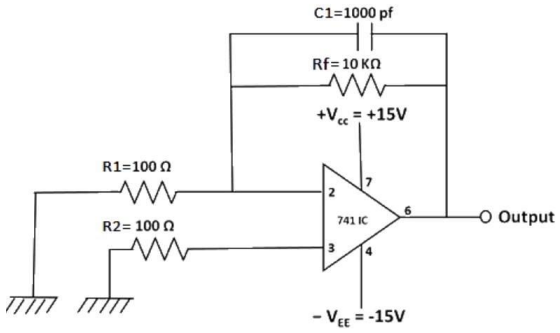


Fig 6: Circuit diagram to measure input offset voltage.

Table 4: Connection table to measure input offset voltage.

S. No.	Source	Target
1	IC741_ pin 07	Supply VCC
2	Multimeter_GND	Supply GND
3	IC741_ pin 04	Supply VEE
4	Resistance (R_f)_terminal A1	IC741_ pin 02
5	Resistance (R_f)_terminal C1	IC741_ pin 06
6	Capacitance (C_1) _terminal A1	IC741_ pin 02
7	Capacitance (C_1) _terminal C1	IC741_ pin 06
8	Resistance (R_2) _terminal A1	IC741_ pin 03
9	Resistance (R_2) _terminal C1	Supply GND
10	Resistance (R_1) _terminal A1	IC741_ pin 02
11	Resistance (R_1) _terminal C1	Supply GND
12	Multimeter_VCC	IC741_ pin 06

3. Click on 'Check Connection' button to check connections. If correct, Click on 'Show output voltage' button to view output (Vo) on DMM.

4. Calculate the input offset voltage, Vio using the formula:

Vio = (Vo - IioRf)/(1+Rf/Ri)

5. Click on 'Result' button and enter the claculated value.

D. Measurement of slew rate S.R.

1. Click on the components button to place the component on the table.

2. Make connections as per the circuit diagram or connection table.

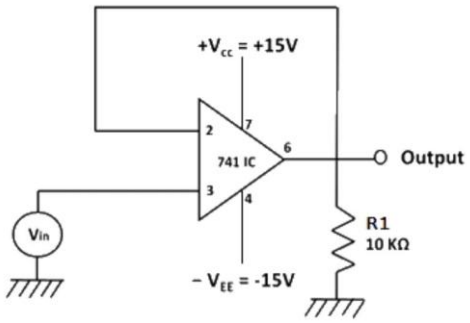


Fig 8: Circuit diagram to measure slew rate.

Table 5: Connection table to measure slew rate.

S. No	Source	Target
1	IC741_ pin 07	Supply VCC
2	IC741_ pin 04	Supply VEE
3	Generator_terminal C	Supply GND
4	Resistance (R_1) _terminal A1	IC741_ pin 06
5	Resistance (R_1) _terminal C1	Supply GND
6	IC741_ pin 06	IC741_ pin 02
7	Generator_ terminal A	IC741_ pin 03
8	CRO_ terminal C	IC741_ pin 06
9	Generator_terminal A	CRO_terminal A

3. The input signal* has to be taken from the red terminal of A.F. Oscillator while the other terminal has to be grounded.

4. Also, feed the input signal to channel CH1 of the C.R.O and the output from Op-Amp IC must be fed to the channel CH2.

5. Click on 'Check Connection' button to check connections. If correct, Click on 'Show output voltage' button to view output.

6. Increase the frequency of input signal using the dial** on A.F. Oscillator until output wave becomes triangular. This is the required frequency fmax in KHz.

7. Calculate the slew rate using the formula:

S.R. = $2\pi f_{max} V_m / 106$ V/μs

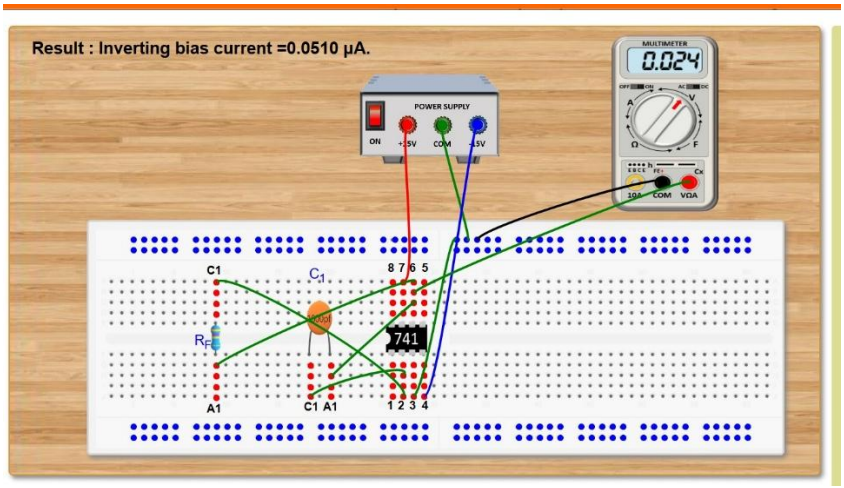
8. Click on 'Result' button and enter the calculated value.

*Amplitude of input signal 'Vm' is 3V.

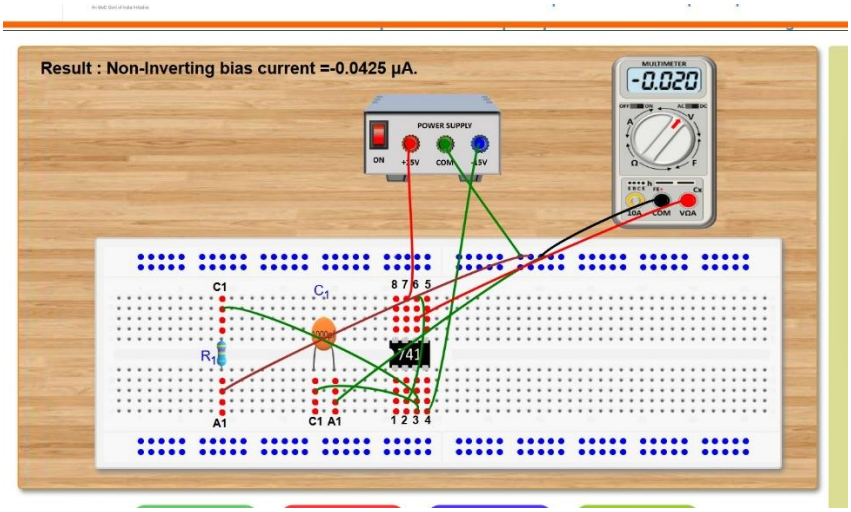
** dial can be controlled through both mouse and keyboard.

Simulation Results:

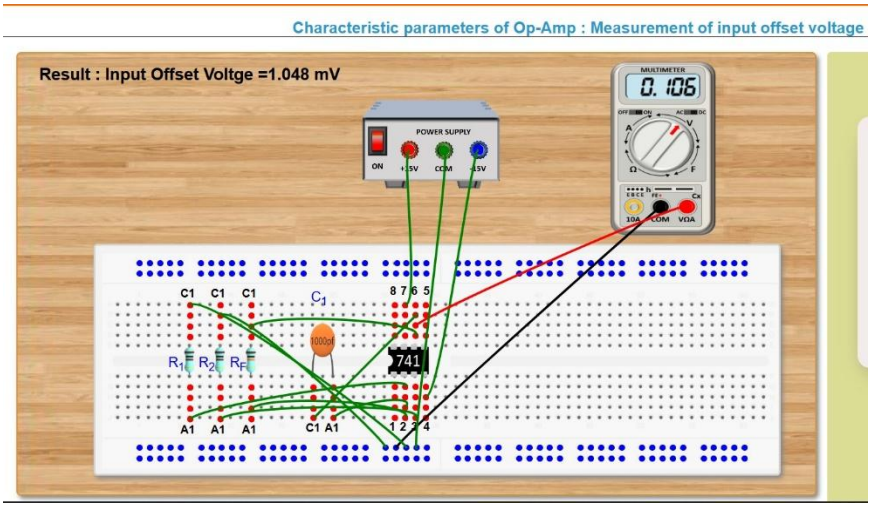
Inverting bias current



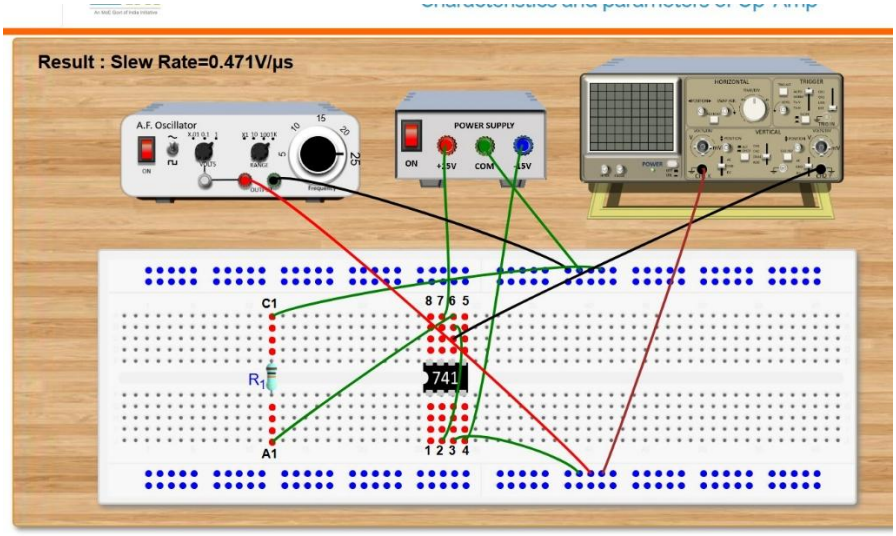
Non-inverting bias current

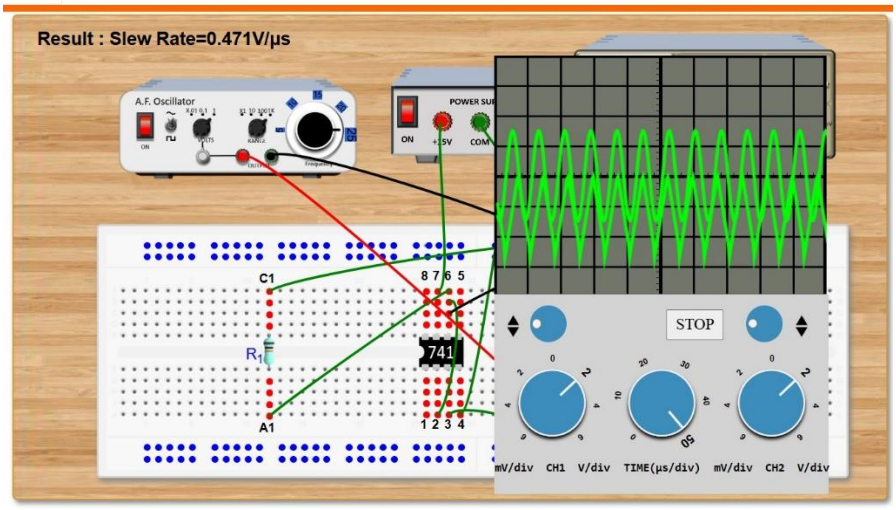


Input Offset current



Slew rate





Result:

The electrical parameters of the IC 741 Operational Amplifier were measured using the virtual simulation. The experimental Slew Rate was found to be 0.471 V/µs, and the Input Offset Voltage was 1.048 mV. These results are consistent with the manufacturer's datasheet specifications.

Inference:

The experiment leads to the following key inferences:

Ideal vs. Practical: Real Op-Amps (like IC 741) deviate from ideal theory. They have finite gain, non-zero offset voltage, and small leakage currents, which must be accounted for in precision circuit design.

Speed Limits: The Slew Rate (0.471 V/μs) limits the Op-Amp's ability to track fast-changing signals, causing distortion (triangular waves) at high frequencies.

Noise Rejection: A high CMRR proves the Op-Amp is highly effective at amplifying the desired signal while rejecting common-mode noise (like 50 Hz power line interference).