ECE 164: Final Project

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The first approach was to calculate the total gain expression of the amplifier by separating the amplifier into the first folded cascode stage and the second CS amplifier stage. The gain expression of the first stage is $A_{folded\ cascode}= -g_{m3}[(g_{m5}r_{o5}r_{o4})||(g_{m6}r_{o6}(r_{o7}||r_{o3}))]$, this was calculated by using the half circuit approach after realizing its symmetry. The gain expression for the CS amplifier stage is $A_{amplifier} = -g_{m9}(r_{o8}||r_{o9})$, this was calculated using a small signal model; thus, the combined gain is $A_{total}= (A_{folded\ cascode})\ (A_{amplifier})$.

The second approach was finding the expressions for the poles, zeros, and phase margin using a simplified reference transconductance circuit. The output impedance from the folded cascode is $R_{out\_cascode}= [(g_{m5}r_{o5}r_{o4})||(g_{m6}r_{o6}(r_{o7}||r_{o3}))]$, the output impedance of the CS stage is $R_{out\_CS}=(r_{o8}||r_{o9})$. Thus, the first pole $w_{pole\_1}=\frac{-1}{(C_c * g_{m9} * R_{out\ cascode} R_{out\ CS})}$, the second pole $w_{pole\_2}=\frac{-g_{m9}}{C_l}$. Next, the unity bandwidth pole is $w_{unity}=(A_{total})(w_{pole\_1})$, and after some cancellation the $w_{unity}= \frac{-g_{m3}}{C_c}$. Finally, we calculated the location of the zero to be at $w_{zero}=\frac{-g_{m9}}{C_c(-g_{m9}R_z-1)}$ and included the zero in to the phase margin expression $PM= 90° - \tan^{-1}(\frac{w_{unity}}{w_{pole2}}) - \tan^{-1}(\frac{w_{unity}}{w_{zeros}})$.

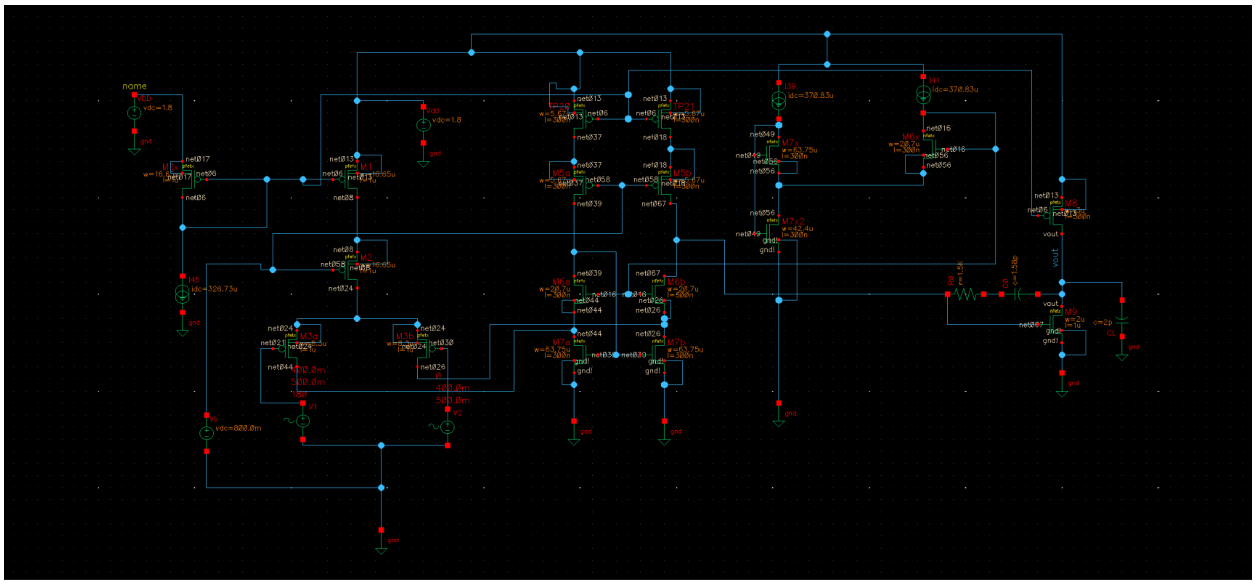
Next, the derived equations were used to find the current ratios of the cascode structure. Setting the unity gain spec to $w_{unity}=\frac{-g_{m3}}{C_c}=\frac{-1}{2\pi}\cdot\frac{2I_3}{v_{ov}}= 130$ MHz. Thus, the resulting $I_3 = 163.36$ uA and since M_3 is a differential pair, $I_1 = 2I_3 = 326.72$ uA. To find the ratio between $I_4 = I_5 = I_6$ and I_3, we set the target gain of the cascode stage to be 50 dB. Putting the g_m's and r_o's in terms of their respective currents and approximating $\lambda = 0.2$ and $V_{ov} = 0.2V$ for both NMOS and PMOS after sweeping v_{ds} and i_{ds} values on Cadence. The resulting ratio is $\frac{I_4}{I_3}= 2.27$, which leads to $I_4 = 2.27I_3 = 370.83$ uA. Notice that M_4 M_5 M_6 have the same current running through and M_7's current is from M_3 and $M_{4,5,6}$, therefore, $I_7 = I_4 + I_3 = 534.19$ uA. To find the last set of currents $I_8 = I_9$, the phase margin equation was set to the desired 65° and $Rz \rightarrow +\infty= \frac{1}{g_{m9}}$ and evaluated. Again substituting the g_m's for their currents, it was found that $\frac{I_9}{I_3}= 2.14$, thus, $I_8=I_9 = 350$ uA. Early in the designing process C_c is set to 2pF, and will later be adjusted to meet the PM and GM specs.

With all the desired currents found, the (W/L)'s of the transistors can be derived by using the saturation current equation. Our results are $(W/L)_1 = (W/L)_2 = 332.72$, $(W/L)_3 = 166.35$, $(W/L)_4 = (W/L)_5 = 377.63$, $(W/L)_6 = 69.39$, and $(W/L)_7 = 99.96$. To start, we standardized and chose a big value for all the transistor L's so that channel length modulation can be neglected. We settled for L = 0.1 um and set the widths based on the ratios above.

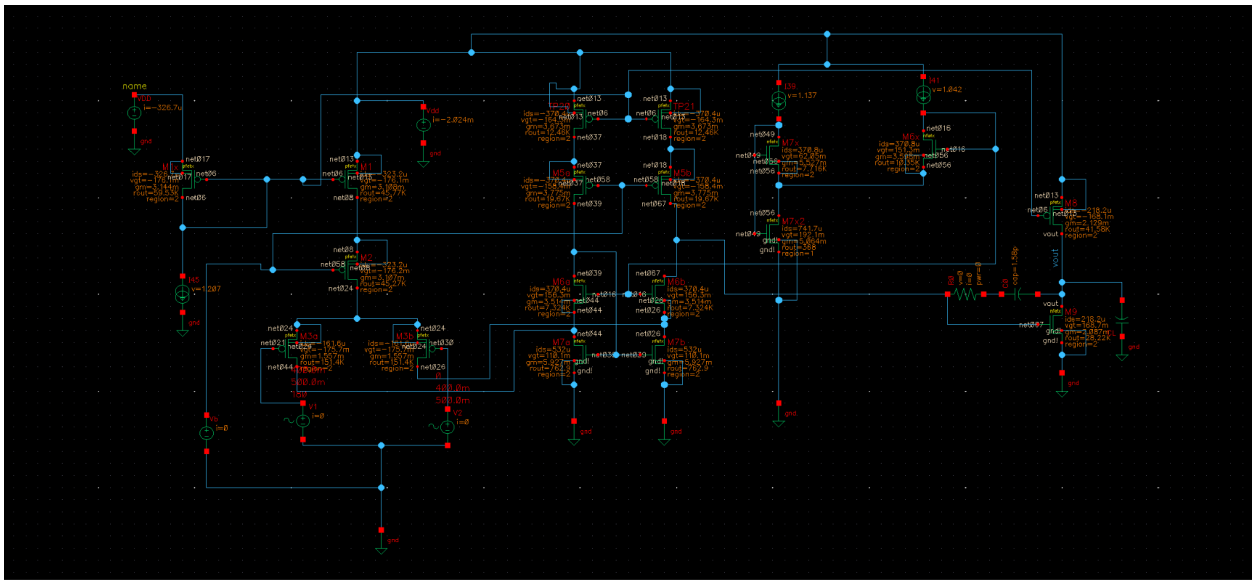
To isolate the amplifier design, some biasing structures were used to fixed idle currents and voltages. The current through M_1 is biased using a PMOS current mirror called M_{1x} with fixed ideal current of 326.72uA, and a fixed voltage source Vb=800mV is set to a voltage that

ensures all transistors are in saturation. M_6 and M_7 are biased using a magic battery to set a fixed current of 370.83uA and a fixed gate voltage for M_6 at about 757mV. Lastly, the common mode input voltage is set to 400mV with opposite phase.

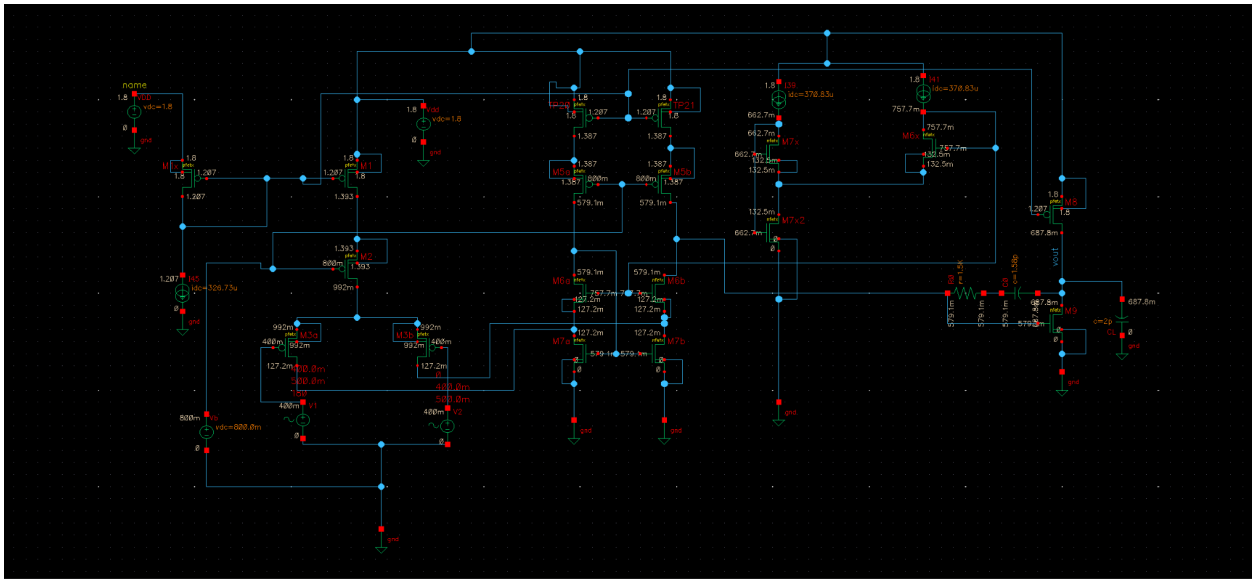
Schematic with just (W/L)



Schematic with Ids, vgt, gm, rout, region



Schematic with just the node voltages



All hand calculations are here

$$\omega_c = -\frac{g_{m3}}{C_c} \Rightarrow \frac{1}{2\pi} \cdot \frac{2I_{D3}}{V_{OV} C_c} = 130\ MHz$$

From the above equation, $I_3 = 163.36$ uA. $I_{1,2} = 2I_3 = 326.72$ uA.

Aiming for 60 dB Gain, so 50 dB for 1st stage, 10 dB for second stage

$$50\ dB\ gain \rightarrow -g_{m3}\left[g_{m5} r_{os} r_{o4} \parallel g_{m6} r_{o6}\left(r_{o7} \parallel r_{o3}\right)\right] = 316.23$$

$$-\frac{2I_{D3}}{V_{OV3}}\left[\frac{2I_{D5}}{V_{OV5}} \cdot \frac{1}{\lambda_5 I_{D5}} \cdot \frac{1}{\lambda_4 I_{D4}} \parallel \frac{2I_{D6}}{V_{OV6}} \cdot \frac{1}{\lambda_6 I_{D6}}\left(\frac{1}{\lambda_7 I_{D7}} \parallel \frac{1}{\lambda_3 I_{D3}}\right)\right]$$

$$= -\frac{2I_{D3}}{V_{OV3}}\left[\frac{2}{V_{OV5}\lambda_5 \lambda_4 I_{D4}} \parallel \frac{2}{\lambda_6 V_{OV6}}\left(\frac{1}{\lambda_7 I_{D7}} \parallel \frac{1}{\lambda_3 I_{D3}}\right)\right]$$

finding ratio between $I_4 = I_5 = I_6$ (cascode) and I_3:

Assume $V_{OV} = 0.2$, $\lambda = 0.2$

$$-\frac{2I_3}{0.2}\left[\frac{2}{0.1^2 \cdot 0.2 \cdot I_4} \parallel \frac{2}{0.1(0.2)}\left(\frac{1}{0.1(I_3+I_4)} \parallel \frac{1}{0.1 I_3}\right)\right] = 316.23$$

$$\frac{I_4}{I_3} \approx 2.27$$

From the above ratio, $I_{4,5,6} = 370.83$ uA. $I_7 = I_4 + I_3 = 534.19$ uA.

Using phase margin spec to find $I_8 = I_9$:

$$PM = 90° - \tan^{-1}\left(\frac{\omega_u}{\omega_{p2}}\right) - \tan^{-1}\left(\frac{\omega_u}{\omega_z}\right) = 65°$$

$$= 90° - \tan^{-1}\left(\frac{-g_{m3}/C_c}{-g_{m9}/C_L}\right) - \tan^{-1}\left(\frac{\frac{-g_{m3}}{C_c}}{\frac{-g_{m9}}{C_c(g_{m9}R_2 - 1)}}\right)$$

$$= 90° - \tan^{-1}\left(\frac{\frac{-2I_3}{C_c V_{ov}}}{\frac{-2I_9}{C_L V_{ov}}}\right) - \tan^{-1}\left(\frac{\frac{-2I_3}{C_c V_{ov}}}{\frac{-2I_9/V_{ov}}{C_c\left(\frac{-2I_9}{V_{ov}}R_2 - 1\right)}}\right)$$

$$= 90° - \tan^{-1}\left(\frac{I_3}{I_9}\right) - \tan^{-1}\left(\frac{I_3}{I_9}\cdot\left(-\frac{2I_9}{V_{ov}}R_2 - 1\right)\right)$$

setting $R_2 = 1/g_{m9}$

$$90° - \tan^{-1}\left(\frac{I_3}{I_9}\right) - \tan^{-1}(0) = 65°$$

$70° =$

$$\tan^{-1}\left(\frac{I_3}{I_9}\right) = 25° \Rightarrow \frac{I_3}{I_9} = 0.466 \Rightarrow \frac{I_9}{I_3} = 2.14$$

From the above ratio, $I_8 = I_9 = 350$ uA.

Using the saturation current equation, the (W/L) ratios and respective W and L values are:

$K_p' = 99.1\ \mu A/V^2$

$K_n' = 267.2\ \mu A/V^2$

using $L = 1\ \mu$

$$I_3 = \frac{1}{2}K_p'\left(\frac{W}{L}\right)_3 V_{ov}^2 \Rightarrow \left(\frac{W}{L}\right)_3 = 166.35$$

$W_3 = 166.35\ \mu m$

$$I_1 = \frac{1}{2}K_p'\left(\frac{W}{L}\right)_1 V_{ov}^2 \Rightarrow \left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = 332.72$$

$W_1 = W_2 = 332.72\ \mu m$

$$I_4 = \frac{1}{2}K_p'\left(\frac{W}{L}\right)_4 V_{ov}^2 \Rightarrow \left(\frac{W}{L}\right)_4 = \left(\frac{W}{L}\right)_5 = 377.63$$

$W_4 = W_5 = 377.63\ \mu m$

$$I_4 = I_6 = \frac{1}{2}K_n'\left(\frac{W}{L}\right)_6 V_{ov}^2 \Rightarrow \left(\frac{W}{L}\right)_6 = 69.39$$

$W_6 = 69.39\ \mu m$

$$\left(\frac{W}{L}\right)_7 = 99.96, \quad W_7 = 99.96\ \mu m$$

g_m calculations (values from hand calculations)

$$g_{m1} = g_{m2} = \frac{2I_{1,2}}{V_{OV}} = \frac{2(326.72\ uA)}{200\ mV} = 3.26\ mS$$

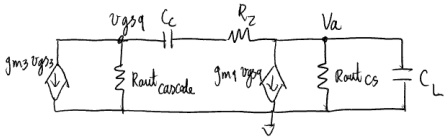
$$g_{m3} = \frac{2I_3}{V_{OV}} = \frac{2(326.72\ uA/2)}{200\ mV} = 1.63\ mS$$

$$g_{m4,5,6} = \frac{2I_4}{V_{OV}} = 3.7\ mS$$

$$g_{m7} = \frac{2I_7}{V_{OV}} = 5.3\ mS$$

$$g_{m8} = g_{m9} = \frac{2I_{8,9}}{V_{OV}} = 3.5\ mS$$

Deriving the equation of the zeros:



$$\Rightarrow \frac{V_a - V_{gs9}}{s\frac{1}{C_L} + R_z} + g_{m9} V_{gs9} + \frac{V_a}{R_{out\,CS}} = 0$$

$$\Rightarrow \frac{-V_{gs9}}{s\frac{1}{C_L} + R_z} + g_{m9} V_{gs9} = 0$$

$$\Rightarrow V_{gs9}\left(g_{m9} - \frac{1}{\frac{1}{sC_L} + R_z}\right) = 0$$

$$w_z = \frac{-g_{m9}}{C_c(g_{m9} R_z - 1)}$$

Early values of C_c and R_z

$$R_z = \frac{C_c + C_L}{C_c(g_{m9})}$$

For $C_c = 2\ pF$ and $C_L = 2\ pF$

$$R_z = \frac{(2\ pF) + (2\ pF)}{(2\ pF)(3.5\ mS)} = 517.4\ \Omega$$

Power dissipation of amplifier P(dc) = Vdd($2I_1 \cdot 2I_4 \cdot 3I_8$) = 5.81 mV

Parameters	Hand Calculations	Cadence Values
I_1,I_2	326.72 uA	323uA
I_3	163.36 uA	161.6uA
I_4, I_5, I_6	370.83 uA	370uA
I_7	534.19 uA	532uA
I_8, I_9	350 uA	218.2uA
g_{m1}, g_{m2}	3.26 mS	3.107mS
g_{m3}	1.63 mS	1.557mS
g_{m4}, g_{m5},g_{m6}	3.7 mS	3.673mS

g_{m7}	5.3 mS	5.927mS
g_{m8}, g_{m9}	3.5 mS	2.129mS, 2.087mS
C_c	2 pF	1.58 pF
R_z	517.4 Ω	1.5 kΩ
Power dissipation (dc) Includes all biasing components.	5.81 mV	4.23mV

Biasing and ratios troubles

In the very early stage of designing, we initially set the lengths of all the transistors to 180n, however, we soon realized that making the length at the minimum will cause channel length effects rendering our hand calculations to look nothing like simulation. Thus, we changed all the lengths into 1um which made most of our hand calculations match up with simulations. Next, we had some problem with biasing the amplifier to meet the desired currents. Transistors M_{7a} and M_{7b} keep going into triode at the slightest change to the lengths of $M_{4,5,6}$ even though the currents, overdrive voltage, and the (W/L) ratios for the entire cascode remain constant. Which is why during simulation, we continuously had to change the (W/L) ratio of M_7 to ensure it stays in saturation. This is why the ratio for M_7 in simulation is at a 212 while the hand calculated ratio is around 100.

AC components problems

Running our first simulation with the initial hand calculated W/L's, currents, and other design parameters, our simulation only met the gain requirement with 70 dB as well as the unity gain bandwidth spec. However, we did not meet the phase margin (we had negative phase) or the gain margin. We ran into the problem of meeting one spec (like phase margin) and being unable to meet the other (like unity gain bandwidth) because the unity gain bandwidth relies on the dominant pole whereas the phase margin relies on the first non dominant pole. Therefore, increasing the UGBW will degrade the PM.

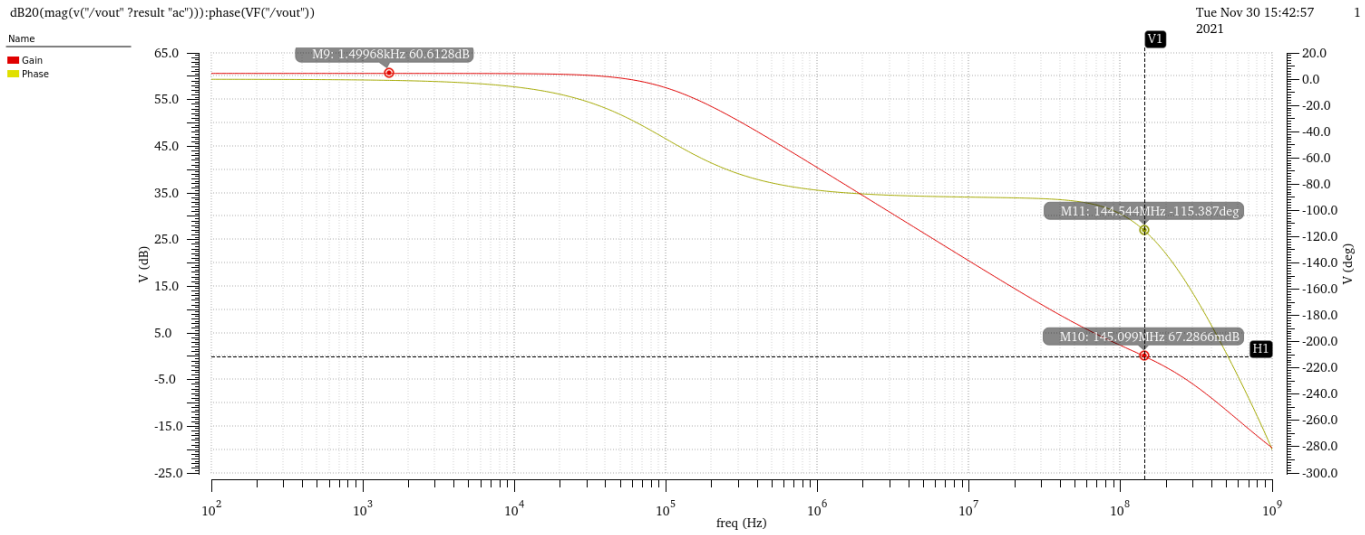
To solve this, we decreased Cc from 2 pF to 1.58 pF to move the poles up to a higher frequency. We aimed to increase Cc such that we hit our UGBW spec with room to spare such that we can tweak our circuit and meet the PM spec. To compensate for the PM after hitting the UGBW, we used pole-zero cancellation to cancel the second pole by setting R_z to $(C_c + C_L)/(C_c g_{m2})$. However, the pole-zero cancellation calculated value of Rz did not give us the desired phase margin, so we increased it a little more to 1.5kΩ, placing the zero after the second pole, until it gave us the correct phase margin. To mitigate the effect of extra non-dominant poles on our gain and phase margins, we lowered the output impedance at target nodes by reducing the length of our devices while keeping their ratio unchanged. This is why L = 0.3 um instead of the

initial L = 1 um in the schematic. Because we decreased L in many of our devices, the gain changed from 70 dB to 60 dB. We iterated through many design choices: different L's to reduce output impedance as well as different combinations of Cc and Rz until we could hit both the UGBW and PM specs.

All the calculated currents and gm's remain very similar to the simulated values, with some minor discrepancies. Error can be attributed to the difference in transistor Vov's. We approximated Vov = 0.2 V for our hand calculations, but it ranged from 0.15-0.22 V. We also neglected channel length modulation in our current calculations, which could also explain the slight deviations. In our simulation, L = 0.3 um, so channel length could be affecting the currents and, therefore, the transconductance. The only dramatically different changes in the table are the values for I_8, I_9 and consequently g_{m8} and g_{m9}. This was because our desired currents and W/L ratios for M_8 and M_9 put those transistors in triode. To place them in saturation, we used the saturation current equation, kept the W/L ratio the same, and solved for the correct currents needed.

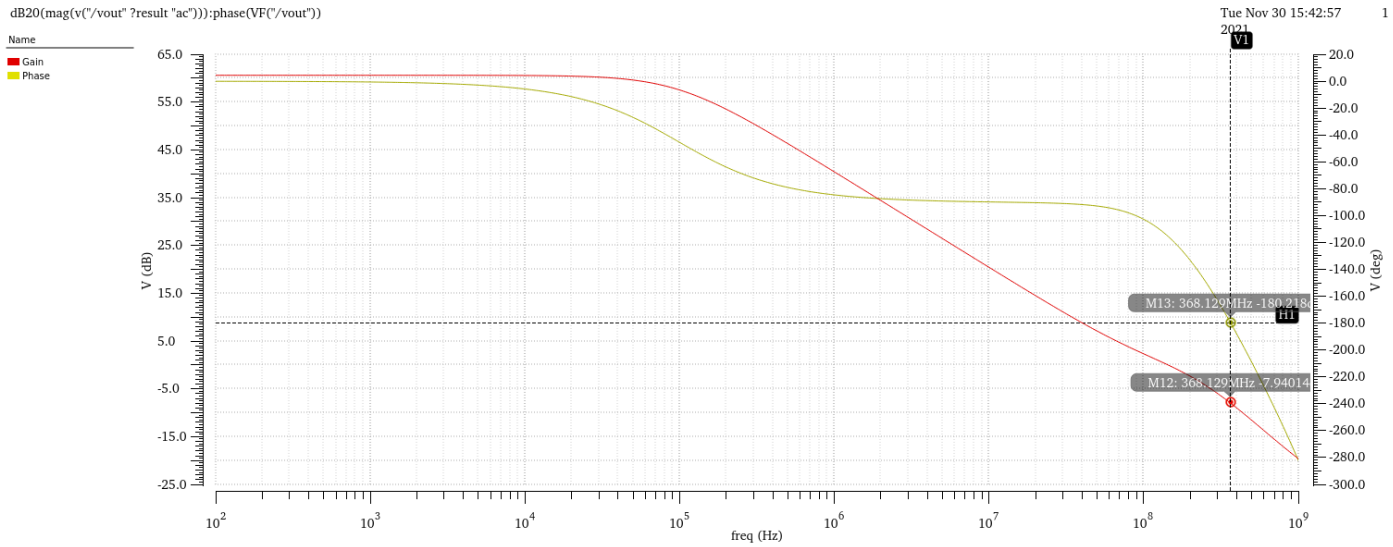
Below is the Bode plot containing the DC gain, Unity Gain bandwidth and Phase Margin

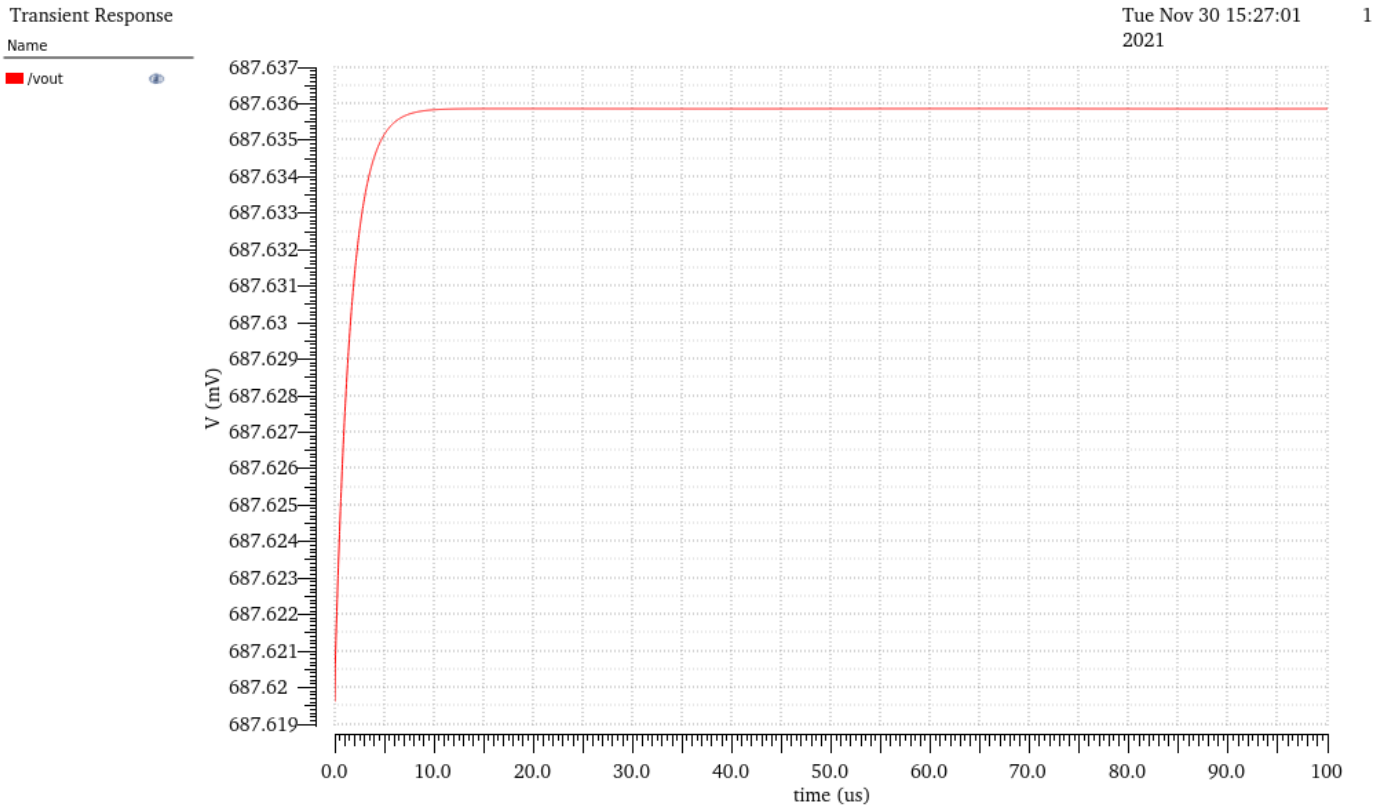
- DC gain is shown by Marker M9: Gain=60dB
- Unity Gain Bandwidth is shown by marker M10: f_{unity_gain}=145MHz
- Phase Margin is shown by markerM10 and M11: -115°-180° = 65°



Below is the bode plot for only the Gain Margin

- Gain Margin is shown by marker M11 and M12: -(-7.904dB)=7.094dB




Transient Response
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time (us)

Regrettably, we were unable to meet the gain margin. We understood our gain equations, where all the AC components such as the poles and zeros derivations came from, and how the biasing circuit is supposed to connect to the amplifier circuits. Everything made sense up to the point of the simulations where a lot of our hand calculations no longer matter due to confusing discrepancies and “invisible” components such as channel length and intrinsic capacitors that messed with our gain and phase margin. We have tried countless iterations with the nulling resistor Rz and Cc to barely meet our phase margin specs and gain spec but they just did not work. We tried to calculate the locations of the poles using the currents and any other values that were available to cancel out poles and to move the zeros, but that didn’t work either. Our gain margin is 7dB off and we are still confused on how to fix this problem.

We learned a lot about the design process and how important it is to analyze a large circuit in smaller parts with derived equations before jumping to any cadence simulation. We also learned that frequency planning is one of the most important considerations and that it should be the foremost step in the design process. In fact, the frequency planning was one of the biggest mistakes we made in our project, and if I had the chance to redo the project again, I would have given it a lot more thought during the initial design process. We approached the project with gain in mind first, and did not really think about the positioning of our poles and zeros until after we simulated the circuit and found that none of the ac requirements were met.