Correspondence

Design and Implementation of High Frequency Ultrasound Pulsed-Wave Doppler Using FPGA

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***Abstract*—The development of a field-programmable gate array (FPGA)-based pulsed-wave Doppler processing approach in pure digital domain is reported in this paper. After the ultrasound signals are digitized, directional Doppler frequency shifts are obtained with a digital-down converter followed by a low-pass filter. A Doppler spectrum is then calculated using the complex fast Fourier transform core inside the FPGA. In this approach, a pulsed-wave Doppler implementation core with reconfigurable and real-time processing capability is achieved.**

I. Introduction

High frequency ultrasound (>20 MHz) probes and B-mode systems with a spatial resolution on the order of a few microns have been widely used [1], [2]. Accompanied with the development of the high frequency B-mode imaging system, the pulsed-wave Doppler (PD) designs have been proposed and implemented [3]–[6]. High frequency ultrasound (>20 MHz) with improved spatial resolution with Doppler capabilities can be used to detect lower velocities and smaller vessels. Pulsed-wave Doppler systems at higher frequencies are generally implemented by either using analog circuitry such as a mixer to implement demodulation and a sample-and-hold (SH) to acquire Doppler shift signals [3]–[5] or, in digital domain, to estimate the velocity directly after the analog-digital converters (ADCs) without using mixers and SHs [6]. Although the work reported in [6] obtained the blood velocity after the echo signals were digitized, it emphasized exclusively the algorithm for blood velocity estimation.

Since the digital beamformers for high frequency ultrasound arrays have been implemented in a field programmable gate array (FPGA) chip [7], [8], it is worthwhile to also implement pulsed-wave Doppler processing functionalities on the same chip to facilitate duplex scanning. Therefore, this study investigates the design and implementation of the pulsed-wave Doppler function using a FPGA. The motivation of this work is to eliminate any need of using analog circuits (mixers and SHs) by processing Doppler spectrum using a single FPGA chip. Using this approach, the Doppler processing becomes programmable and can be easily integrated with the beamforming function in ultrasound imaging. Furthermore, this design shows an alternative way for implementing the ultrasound pulsed-wave Doppler function digitally.

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II. FPGA-Based Pulsed-Wave Doppler Design

The diagram of the proposed pulsed-wave Doppler system is shown in Fig. 1. The single element transducer used in this study is driven by a 10-cycle burst sinusoid signal with a Vpeak-to-peak of 30V. The returned echoes are amplified with a variable gain amplifier (AD8332, Analog Devices Corp., Norwood, MA) and then sampled with an ADC (AD9433, Analog Devices Corp.) at the sampling frequency of 120 MHz. The sampled data are then fed directly to the FPGA (Virtex II Pro, Xilinx, Inc., San Jose, CA). The reason for using the Virtex II Pro is that a beamformer for a high frequency linear array at 30 MHz was designed on this chip [8]. In FPGA, the digitized data are first sent to the digital-down converter (DDC) block where the demodulated samples are obtained. The demodulated in-phase (I) and quadrature (Q) data then go to the range gate block which determines the location where the Doppler frequency shift should be detected. This range gate block can set the window in the axial direction in 1–2048 samples or any location less than 13 mm. Finally, I/Q signals with Doppler directional information are used to generate the Doppler spectrum.

III. Digital-Down Converter

Generally, analog demodulators (mixers) are used to generate the in-phase/quadrature signals. A digital quadrature demodulation method based on direct IF (intermediate frequency) sampling has advantages over conventional analog quadrature demodulation methods in match accuracy between in-phase and quadrature channels. The other advantages of using DDC are digital stability, controllability, and small size. However, the main limitation of DDC is that the digital demodulation effect is mainly determined by the ADC dynamic range when the signal's amplitude varies greatly. In this study, a 12-bit ADC was used with an effective dynamic range of 70 dB. To achieve higher dynamic range, the high speed ADCs with 14 or 16 bits, if available, should be used.

The DDC block has a configurable data path comprising a digital-down synthesizer (DDS), a digital mixer, a filter, and a series cascade of 2 optional polyphase decimators. The DDS generates the digitized sine and cosine signals required to mix with the digitized echo signals

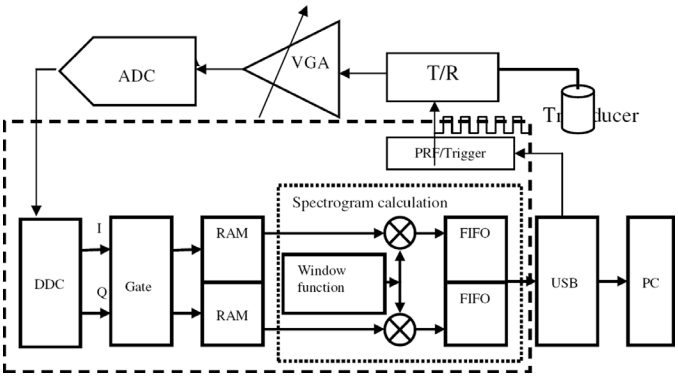

Fig. 1. Diagram of the FPGA-based pulsed-wave Doppler system.

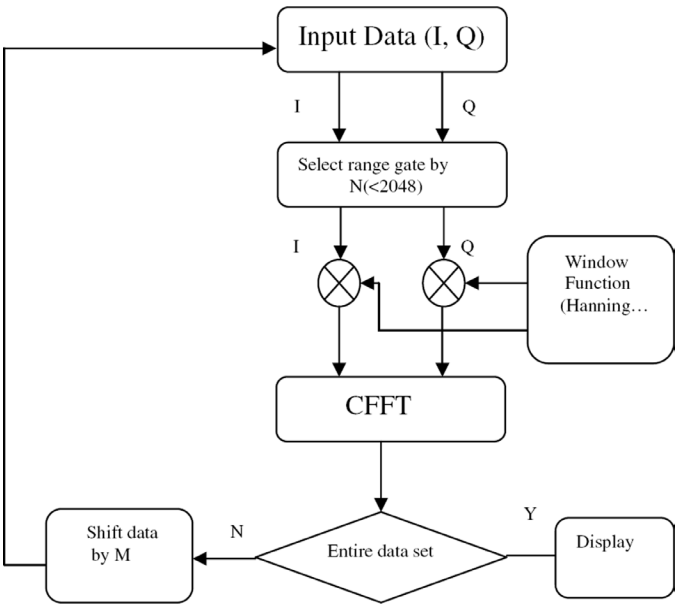

Fig. 2. Block diagram of the spectrogram calculation.

giving both sum and difference frequencies. The filter is a low-pass filter with filter taps and configurable coefficients used to realize the sample rate changes. This quadrature demodulator yields the outputs of I and Q signals, which are used to obtain directional flow infomation.

IV. Spectrum Calculation

The spectrogram block is used to process demodulated data. In this block, the Doppler frequency shift data are selected, weighted, and processed using the complex fast Fourier transform (cFFT) core of the FPGA. The windowed data are also weighted by means of a Hamming function to improve the signal-to-noise ratio (SNR) for the spectrogram display before they are used in the cFFT. In this block, 2 dual-port block random access memories (BRAMs) store the Doppler frequency shifts. A counter is used to generate the reading address for both BRAMs. The windowed I/Q signals are read from memory to be processed using cFFT. The overlap window between 2 consecutive processing is also controlled by another counter. Finally, the Doppler spectrum is obtained after I/Q output from cFFT are squared and summed. The entire spectrogram calculation module is shown in Fig. 2. The implementation results showed that this design uses 29% of total slices, 22% block rams, and 28% multiplexers in the FPGA.

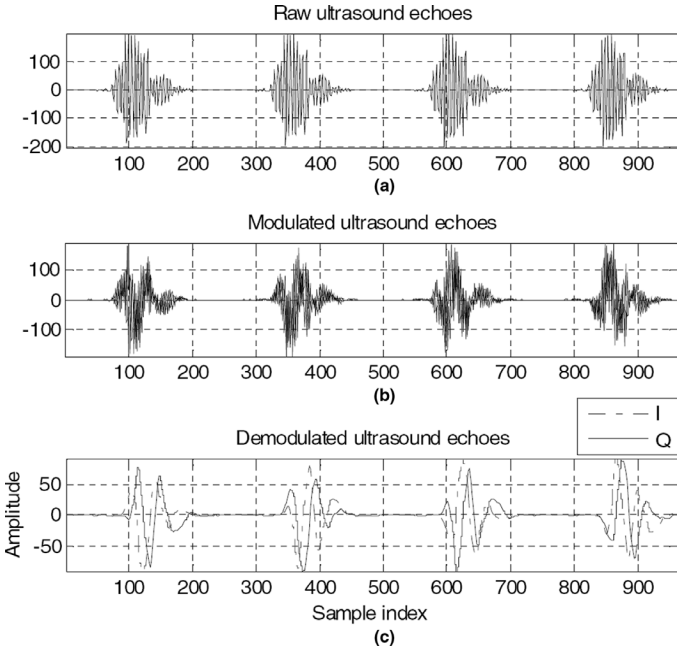

Fig. 3. Results from digital-down conversion block. (a) raw echo train from the Field II simulation; (b) modulated signals with I and Q components from the FPGA; (c) FPGA-demodulated data.

V. Simulation and Experimental Results

The performance of the DDC was tested using the FPGA DSP simulation software (Xilinx, Inc.) and Field II software [9]. The raw ultrasound data were first generated using Field II with a transducer at the frequency of 30 MHz (50% bandwidth). In this simulation, a phantom was used for calculating RF data as measured from the femoral artery in the upper leg. The 250 samples which contain the echoes were selected to form an echo train and were then fed into the DDC module. Fig. 3 presents the results of the digital signal demodulated from the DDC. Fig. 3(a) shows the raw echo train from the Field II simulation, Fig. 3(b) shows the modulated signals with I and Q components from the FPGA. The FPGA-demodulated data are presented in Fig. 3(c). Fig. 4 shows the spectrograms from the numerical simulation and the FPGA data. Fig. 4(a) is the result using Matlab (MathWorks, Inc., Natick, MA), and Fig. 4(b) is the result from the FPGA design. Both spectrograms are displayed at a dynamic range of 40 dB. The mean squared difference between the 2 spectrograms is 0.42.

Measurements of blood velocity from an artery in a human hand were carried out with the implemented high frequency pulsed-wave Doppler function. An angled PMN-PT (HC Materials Corp., Urbana, IL) single crystal needle

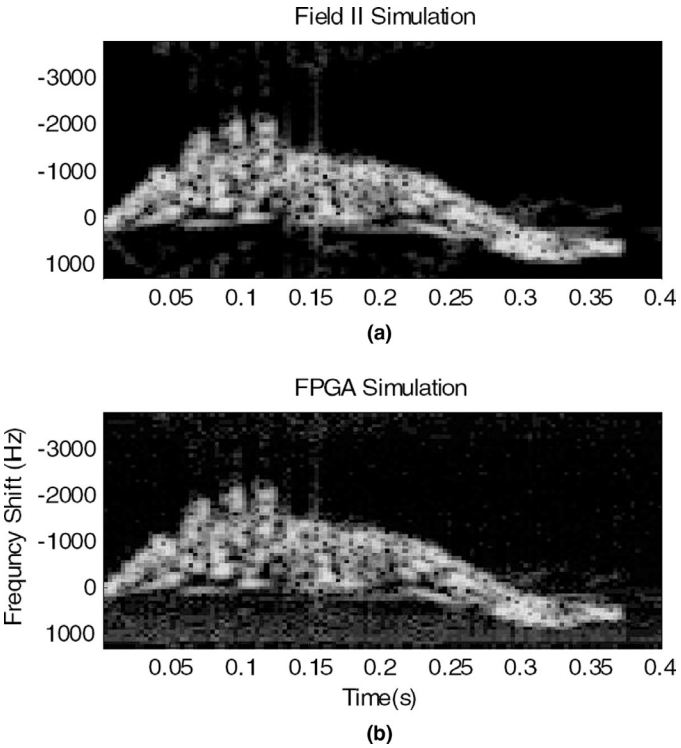

Fig. 4. Spectrograms. Upper: simulation result from Matlab; lower: simulation result from the FPGA.

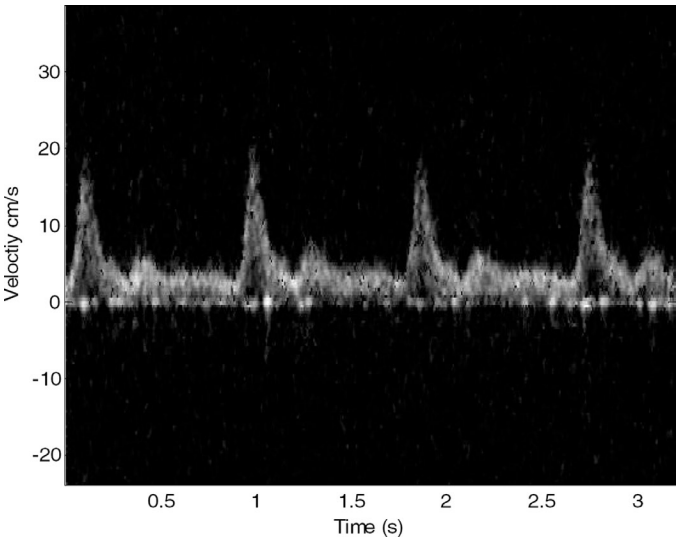

Fig. 5. Spectrogram of an artery in a human hand.

transducer was used. This angled transducer has a center frequency of 30 MHz with a 50% bandwidth. The Doppler angle is 45°. For the measurement, the pulse repetition rate generated from FPGA is 20 kHz. Fig. 5 shows the spectrogram of the Doppler signal from the artery. A maximum axial flow velocity of about 19.5 cm/s is measured.

VI. Conclusions

A pulsed-wave Doppler function for high frequency ultrasound was designed and implemented based on a FPGA chip. Since the FPGA technique has been adopted in medical ultrasound especially for high frequency ultrasound, this design can operate in duplex mode by integrating pulsed-wave function in the same chip with a beamformer in future work.

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