# ANALOG DEVICES

# Evaluation Board for Dual VGA and ADC

# EVAL-AD8332/AD9238

## FEATURES

**Full selection of VGA functions**
**Self-contained high speed differential dual ADC**
**On-board clock source**
**Provisions for external clock**
**Jumper selectable VGA features**
**Standard ADI HSC FIFO board for control**
**Single 5 V supply operation**

## APPLICATIONS

**TGC development in ultrasound systems**
**VGA to ADC interface development**
**Evaluation of TGC filters**
**Evaluation of the AD8332 VGA**
**Evaluation of the AD9238 HS ADC**

## INTRODUCTION

The EVAL-AD8332/AD9238 and ADC evaluation board is a fully integrated dual-channel differential variable gain amplifier (VGA) and analog-to-digital converter (ADC) on a single board. When connected to a multipurpose HSC FIFO board and operated with the accompanying software, ADC Analyzer™, it can convert and display analog waveforms processed by the VGA or perform FFTs and display up to six harmonics. It can be operated with its onboard clock or from an external clock for coherent sampling. Figure 2 is a simplified functional block diagram of the system.

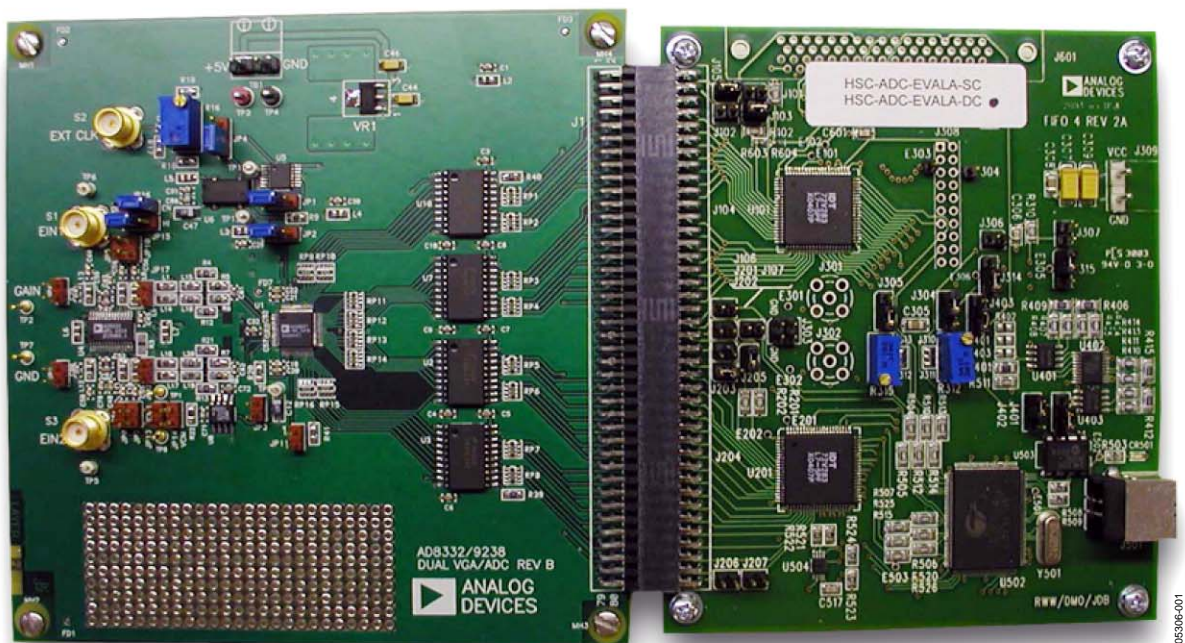Space is provided for a differential filter (with up to four poles) between VGA and ADC.



*Figure 1. AD8332/AD9238 Connected to the FIFO Board*

**Rev. 0**

# TABLE OF CONTENTS

## REVISION HISTORY

**1/05—Revision 0: Initial Version**

# GENERAL DESCRIPTION

Figure 3 is a schematic of the VGA section of the board. There are several user options available for the AD8332. The input impedance is determined by the value of the feedback (RFBn) resistors. Although the default input impedance is 50 Ω, other impedances are obtained replacing the surface mount resistors with the appropriate values (consult the AD8332 data sheet for reference). Removing the feedback resistor results in the open circuit input impedance of 6 kΩ. As a rule of thumb, the value of the resistor is 5.5 × the desired matching impedance.

Figure 4 is the ADC and clock schematic and the power sub-circuit The AD8332 operates from a single 5 V supply, while a 3.3 V LDO (VR1) provides power for the ADC, clock, and digital interface circuitry. Power pins on the devices are decoupled using ferrite beads.

The on-board clock frequency is 20 MHz; thus, the software must be set up with a windowing function to optimize non-coherent sampling. An SMA connector, S2, is provided for an external clock if coherent sampling is desired. The jumper, JP4, must be moved to its upper position. Trimpot R16 can be used to center the clock offset. If R9 and R10 are removed, the two channels of the AD9238 can be operated with independent clocks. Consult the AD9238 data sheet for additional operating details.

Figure 5 is a schematic of the interface circuit. Note that the FIFO evaluation board is available for a parallel port, which uses a standard printer cable, and for a USB. Many new laptop computers have only USB ports, while older laptops have parallel ports but not USB interfaces. Be sure to select the version that will interface with your computer.

For input frequencies from 1 MHz to 5 MHz, the 20 MHz on-board clock provides for adequate sampling despite non-coherency with the input signal, as long as windowing is enabled. (Windowing is an option offered in ADC Analyzer, which ensures that whole integers of the input waveform are sampled.) For the examples shown in this data sheet, the input signal was 1 MHz and the *Hanning* window option was selected. For coherent sampling, synchronized external generators are required for clock and signal inputs. Refer to the FIFO board data sheet for further information.

The signal generator shown in Figure 6 is a general-purpose instrument found on the benches of many labs. Harmonic distortion, although sufficiently low for most applications, can nonetheless be higher than that generated in either the AD8332 or AD9238. To reduce this level at the input, a low pass filter at the frequency of interest may be required.
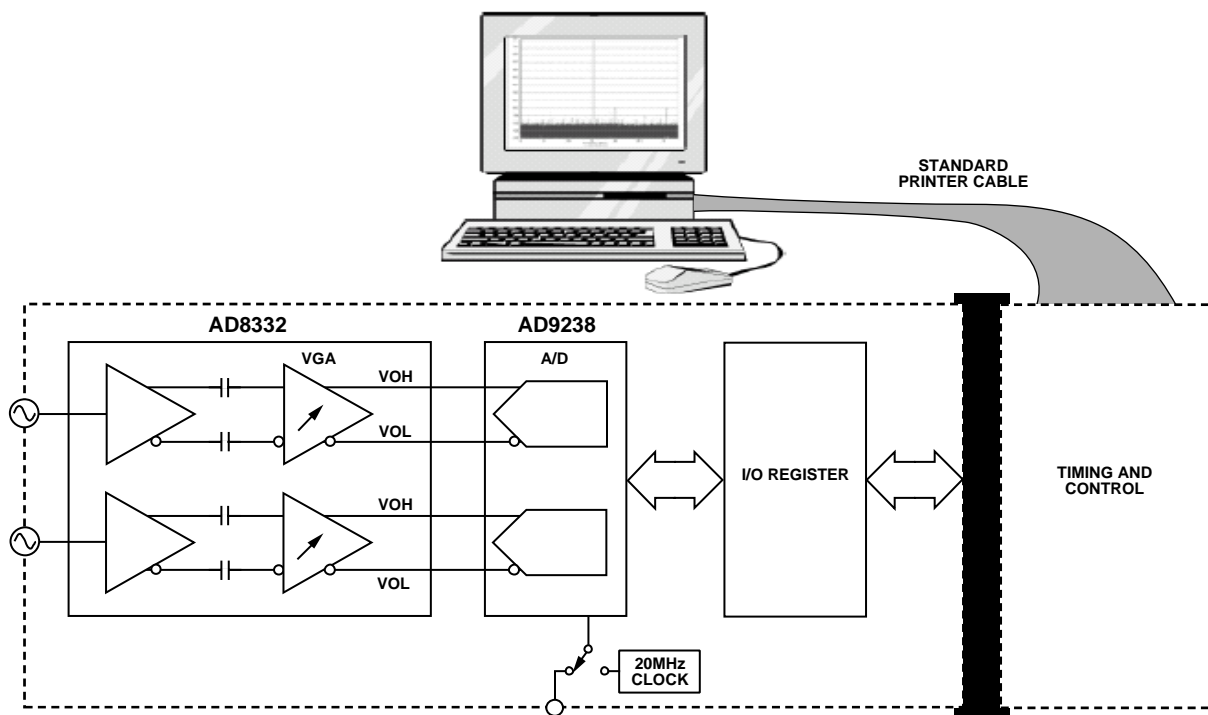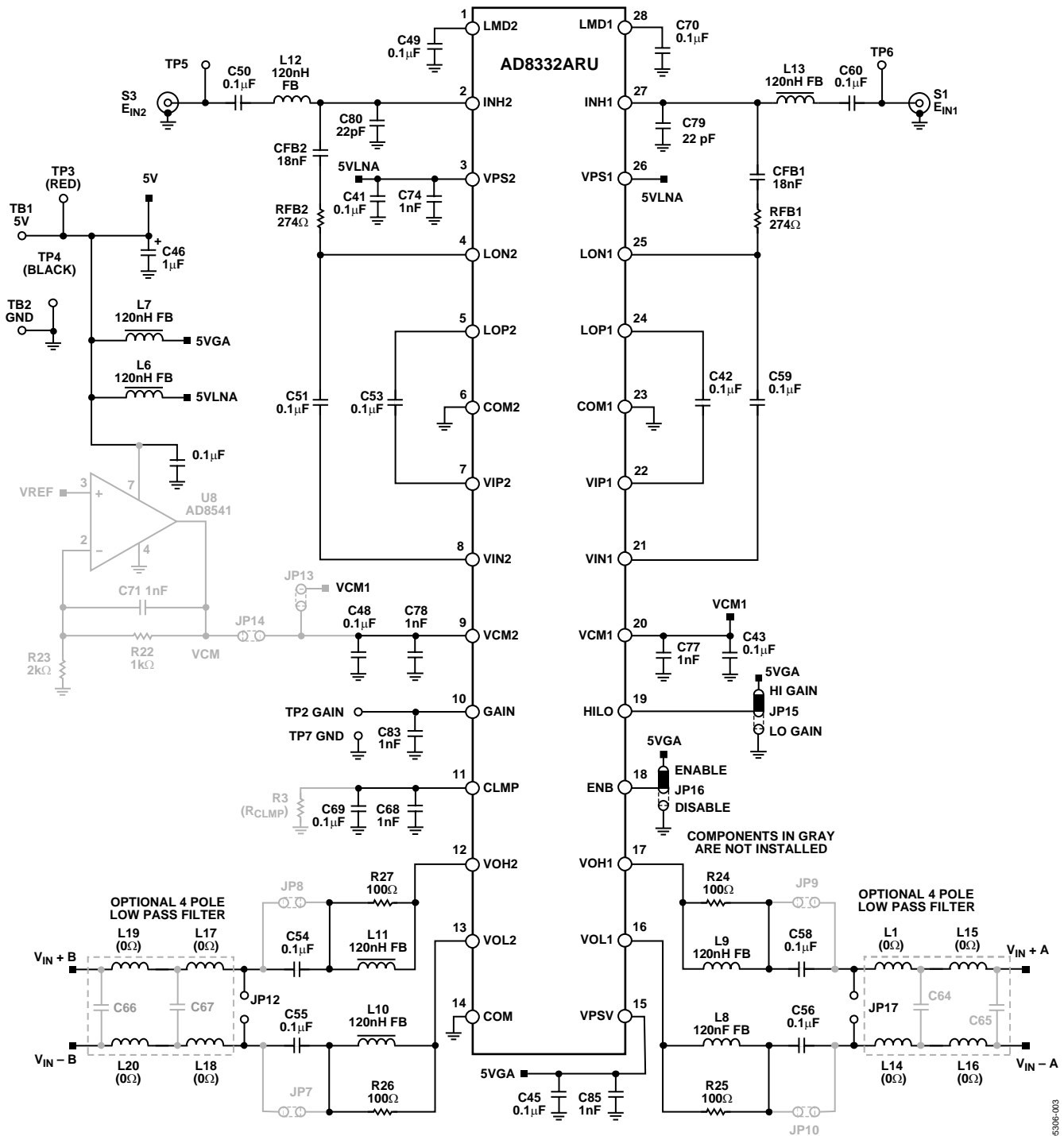


Figure 2. Simplified Block Diagram
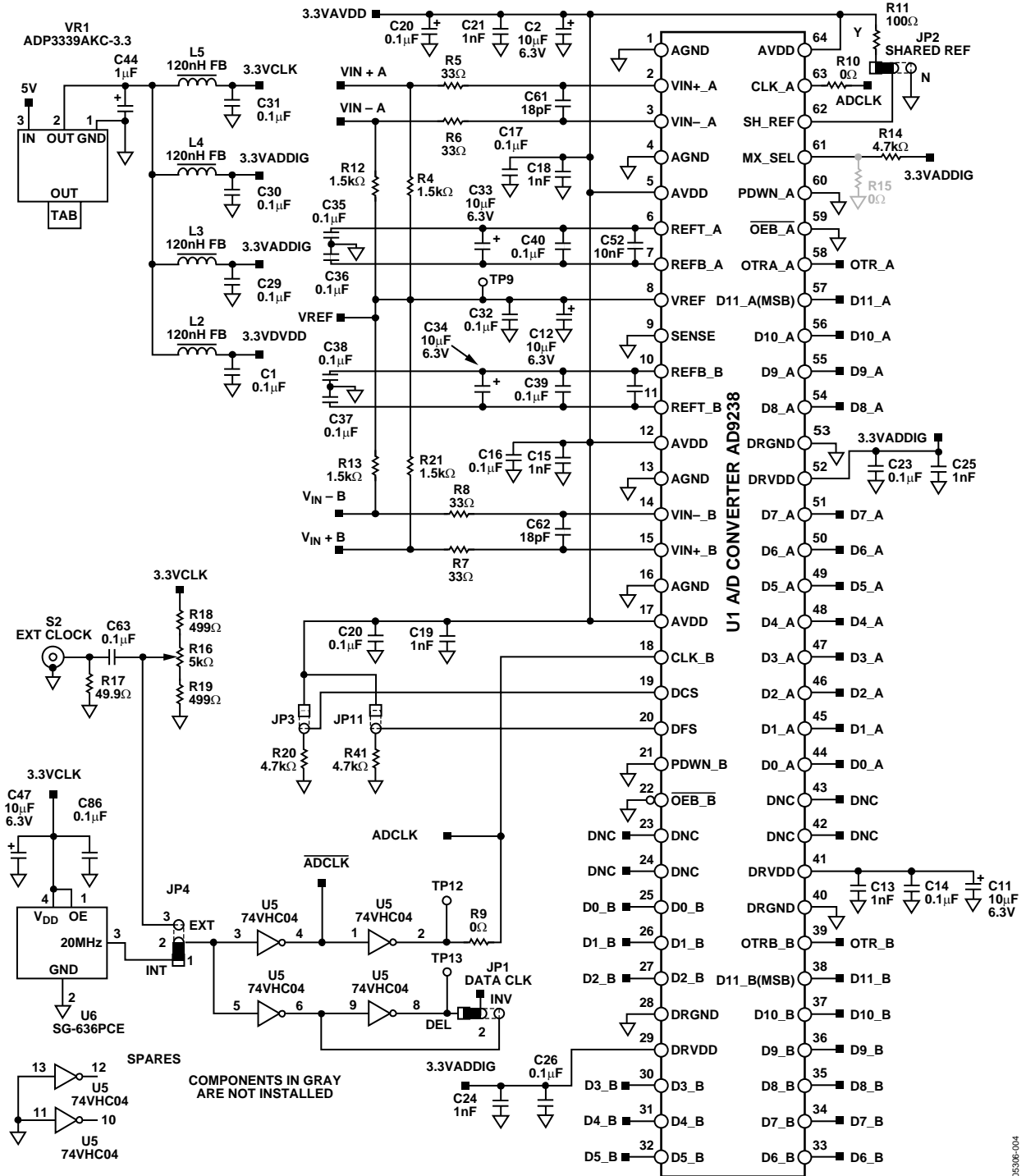
Figure 3. Schematic—VGA
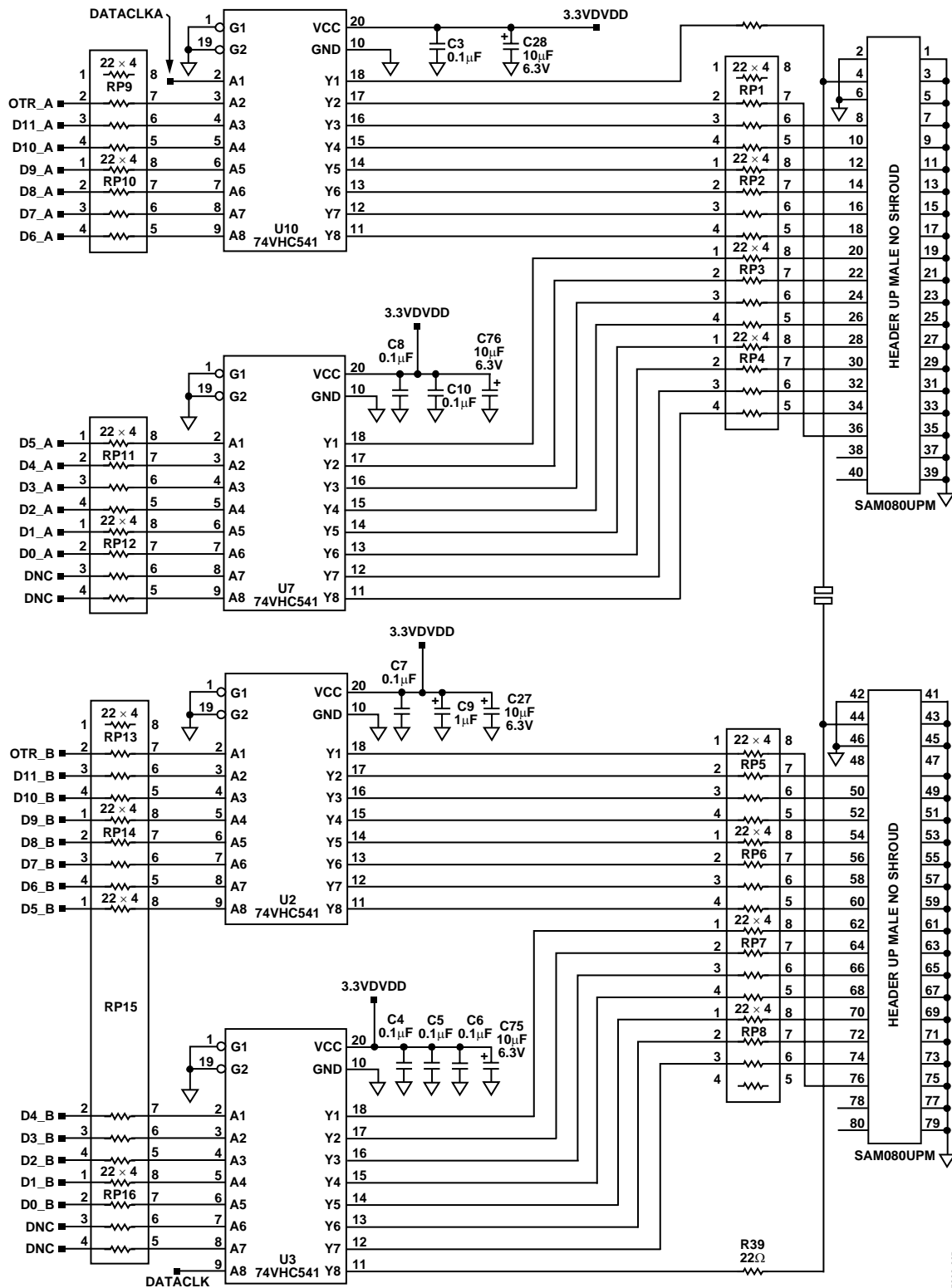
Figure 4. Schematic—ADC

05306-004

Figure 5. Schematic—Interface

# OPERATION

## EQUIPMENT NEEDED

Power supplies—5 V and 3.3 V dc; high speed ADC FIFO evaluation kit; personal computer running Windows 95 or later, analog signal source and low pass filter; and reference supply for Vgain.

## INITIAL SETUP

Table 1 lists the jumper and test-point functions for the VGA and ADC. Because the FIFO board functions as a universal interface for multiple ADC part numbers, it must be configured by jumpers specific for the AD9238. Jumper configurations for printer cable and USB versions are shown separately in Table 2 and Table 3. For a more detailed description of the jumper functions, consult the FIFO data sheet HSC-ADC-EVAL-

SC/HSC-ADC-EVAL-DC (or the EVAL-A version), both of which are found on the Analog Devices website.

Figure 6 illustrates the setup for operation. The EVAL-AD8332/AD9238 is connected to either an HSC-ADC-EVAL-DC or HSC-ADC-EVALA-DC by mating 80 pin headers. The FIFO board connects to a personal computer using a standard parallel port printer cable or USB cable. A mouse is highly recommended if a laptop computer is used. A CD ROM of *ADC Analyzer*, an interactive program that operates the converters and processes the recovered data, is provided with both FIFOs. Refer to the FIFO data sheet for details on loading and operating the software. The system requires +5 V and +3 V 0.5 A supplies.

**Table 1. AD8332/AD9238 Jumpers**

| Jumper | Function | Configuration |
|---|---|---|
| 1 | Data clock—delayed or inverted | Left position (inverted) |
| 2 | Select shared reference (Yes or No) | Left position (Yes) |
| 3 | Duty cycle stabilizer | Not inserted |
| 4 | Select internal or external clock | Internal selected (toward bottom of board) |
| 7 | DC couple low output of Channel 2 | Not inserted |
| 8 | DC couple high output of Channel 2 | Not inserted |
| 9 | DC couple high output of Channel 1 | Not inserted |
| 10 | DC couple low output of Channel 1 | Not inserted |
| 11 | Data format—inserted twos complement; removed offset binary | Not inserted |
| 13 | Connects VCM input of Channel 1 to VCM input of Channel 2 | Not inserted |
| 14 | Connects optional VCM amplifier to VCM inputs | Not inserted |
| 15 | High or low gain select | High gain |
| 16 | Enable or disable the AD8332 | Enable |

**Table 2. FIFO Board Jumper List—Printer Cable (Ref)**

| Jumper | Configuration | Jumper | Configuration | Jumper | Configuration | Jumper | Configuration |
|---|---|---|---|---|---|---|---|
| 1 | Unused | 12 | Installed | 23 | Unused | 33 | Lower position |
| 2 | Unused | 13 | Installed | 24 | Installed | 34 | Installed |
| 3 | Installed | 14 | Installed | 25 | Unused | 35 | Installed |
| 4 | Upper position | 15 | Installed | 26 | Unused | 36 | Installed |
| 5 | Position 3 | 16 | Right position | 27 | Unused | 37 | Installed |
| 6 | Position 3 | 17 | Unused | 28 | Unused | 38 | Installed |
| 7 | Lower position | 18 | Left position | 29 | Unused | 39 | Installed |
| 8 | Installed | 19 | Installed | 30 | Unused | 40 | Installed |
| 9 | Installed | 20 | Installed | 31 | Installed | 41 | Installed |
| 10 | Installed | 21 | Installed | 32 | Left position | 42 | Installed |
| 11 | Installed | 22 | Unused | | | | |

**Table 3. FIFO Jumper List—USB Interface (Ref)**

| Jumper | Configuration | Jumper | Configuration | Jumper | Configuration | Jumper | Configuration |
|---|---|---|---|---|---|---|---|
| 101 | Unused | 202 | Unused | 305 | Position 3 | 313 | Installed |
| 102 | Unused | 203 | Installed | 306 | Unused | 314 | Position 3 |
| 103 | Installed | 205 | Installed | 307 | Unused | 315 | Position 1 |
| 105 | Installed | 206 | Unused | 310 | Installed | 401 | Position 1 |
| 106 | Unused | 207 | Unused | 311 | Installed | 402 | Position 3 |
| 107 | Unused | 303 | Unused | 312 | Installed | 403 | Position 1 |
| 201 | Unused | 304 | Position 3 | | | | |
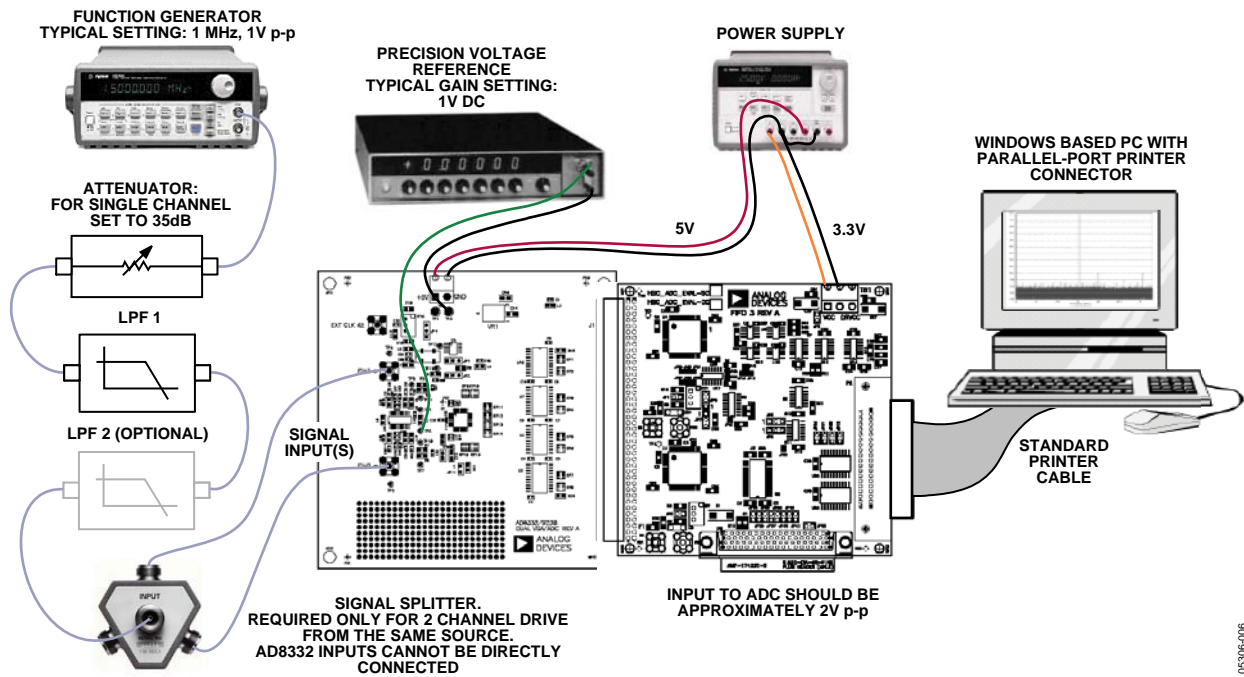


Figure 6. Test Interconnections

## INITIALIZING ANALYZER MENUS

After the power and cabling have been set up, the system is ready for initialization. A 1 MHz sine wave input signal is recommended for this trial run. As a sanity check, observe the waveform prior to digitization by probing JP12 and/or JP17 with a differential probe. Adjust generator and attenuator settings for just under 2 V p-p to the ADC.

Initiate ADC Analyzer on the computer. When prompted for a configuration file, select AD9238. This file will later require modification and will be saved as AD8332 + AD9238.

Before FFT or time domain information can be displayed correctly, you must configure the software for the hardware and the clock frequency in use. In the upper left toolbar, left-click the **Config** button, then FFT (the configuration data applies to both the time domain and FFT displays.) In the **Encode Frequency (MSPS)** box, adjust the MSPS to 20 if the on-board 20 MHz clock is used; otherwise enter the clock frequency of the external clock source being used. In the **Averages** dialog box, type 10. Clear the **Twos Complement** check box. Be sure to enter the same **Encode Frequency (MSPS)** setting to **Channel A** and **Channel B**. See Figure 7 for a display of the FFT configuration setup. Save the revised configuration as a new file—i.e., AD8332 + AD9238.
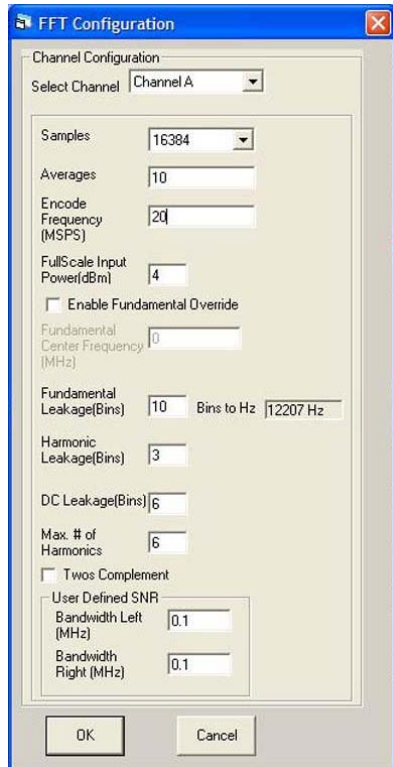


Figure 7. FFT Configuration Menu

Analyzer displays both channels at once. To view a single VGA channel, remove the input signal from the unused input of the AD8332. For a first test, it's a good idea to capture a waveform in time domain. Left-click the **Time Domain** button (Figure 8), and the display appears as in Figure 9.
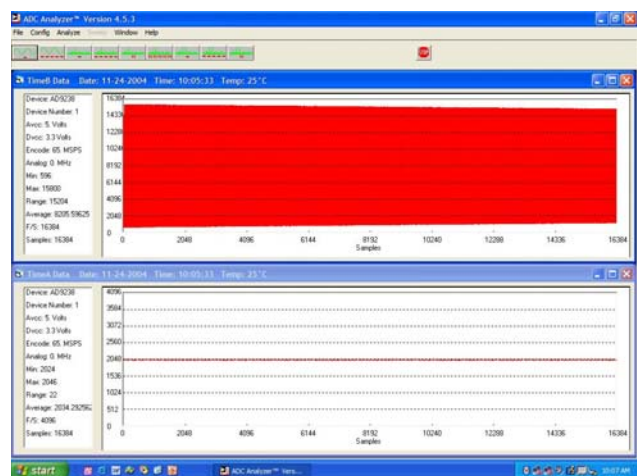


Figure 8. Time Domain Button



Figure 9. Initial Time Domain Display

The plot appears as a solid red rectangle. This is because it is displaying each of the 16 k samples. To crop the display and observe only a few cycles, left-click and drag the cursor horizontally over a small portion of the waveform. Right-click within the dialog box and a menu drops down. Right-click the upper **H-Zoom** option, and the display appears as in Figure 10.
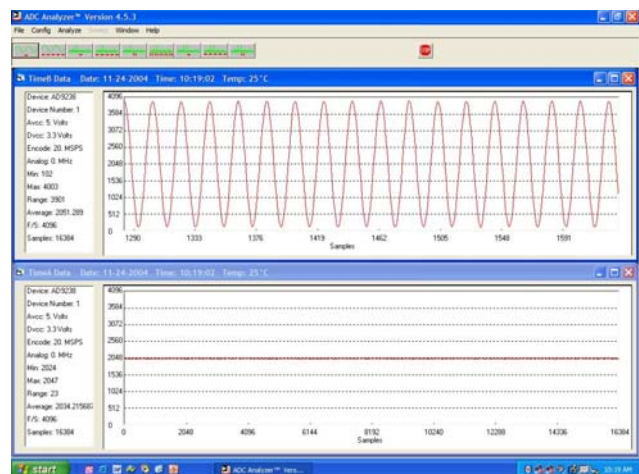


Figure 10. Time Domain Waveform

There are six optional FFT displays: single, sequential-single, average, sequential-average, two-tone and sequential-two-tone. Figure 11 is a display of an FFT performed on both channels of the AD8332 using the same 1 MHz input signal

that is used for the 1 MHz waveforms. A splitter must be used if both LNA channels are driven. Figure 12 and Figure 13 are individual channel FFTs, a useful tool to observe channel isolation.
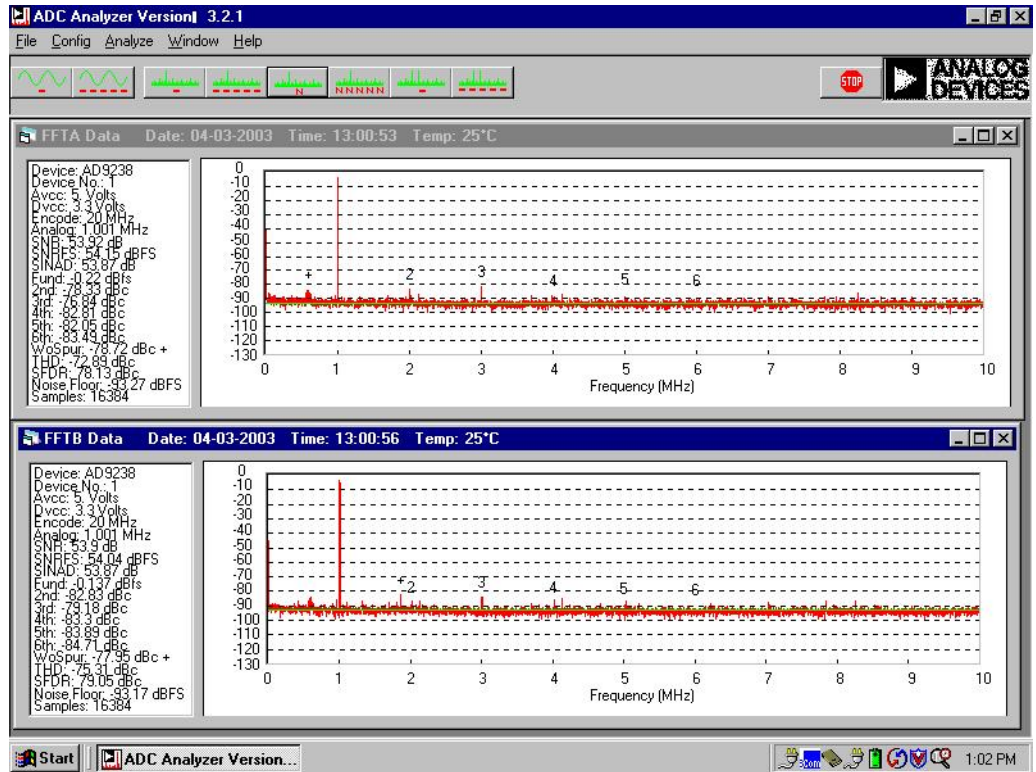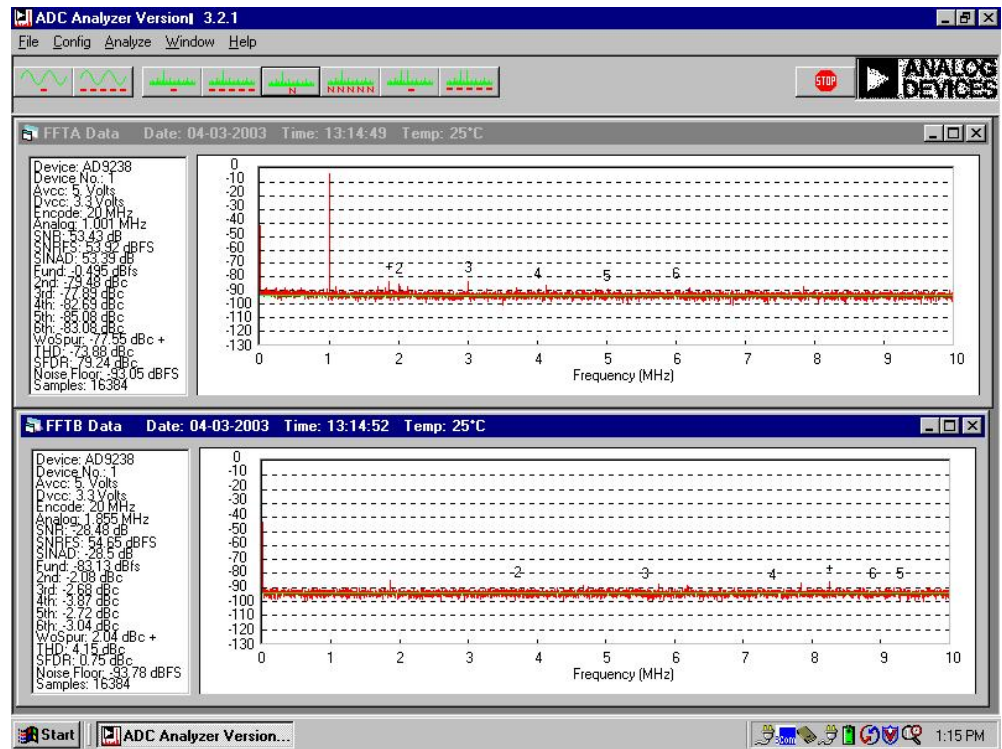


*Figure 11. FFT, Both Channels*
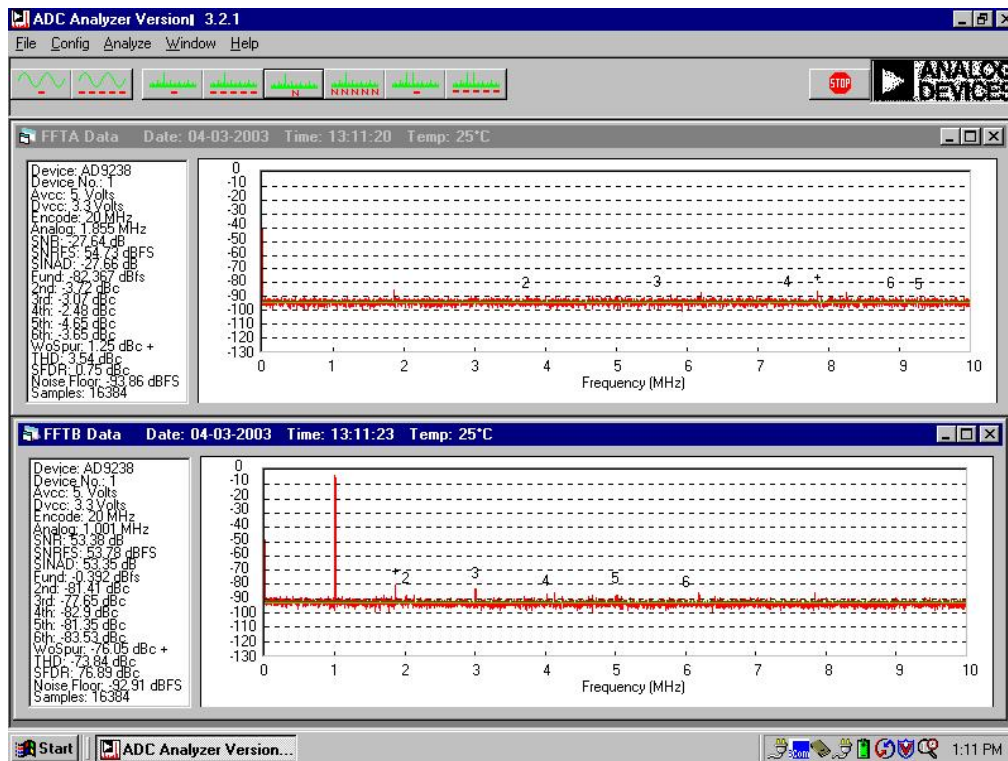
*Figure 12. FFT, Channel 1*



*Figure 13. FFT, Channel 2*

# PRINTED BOARD LAYOUT

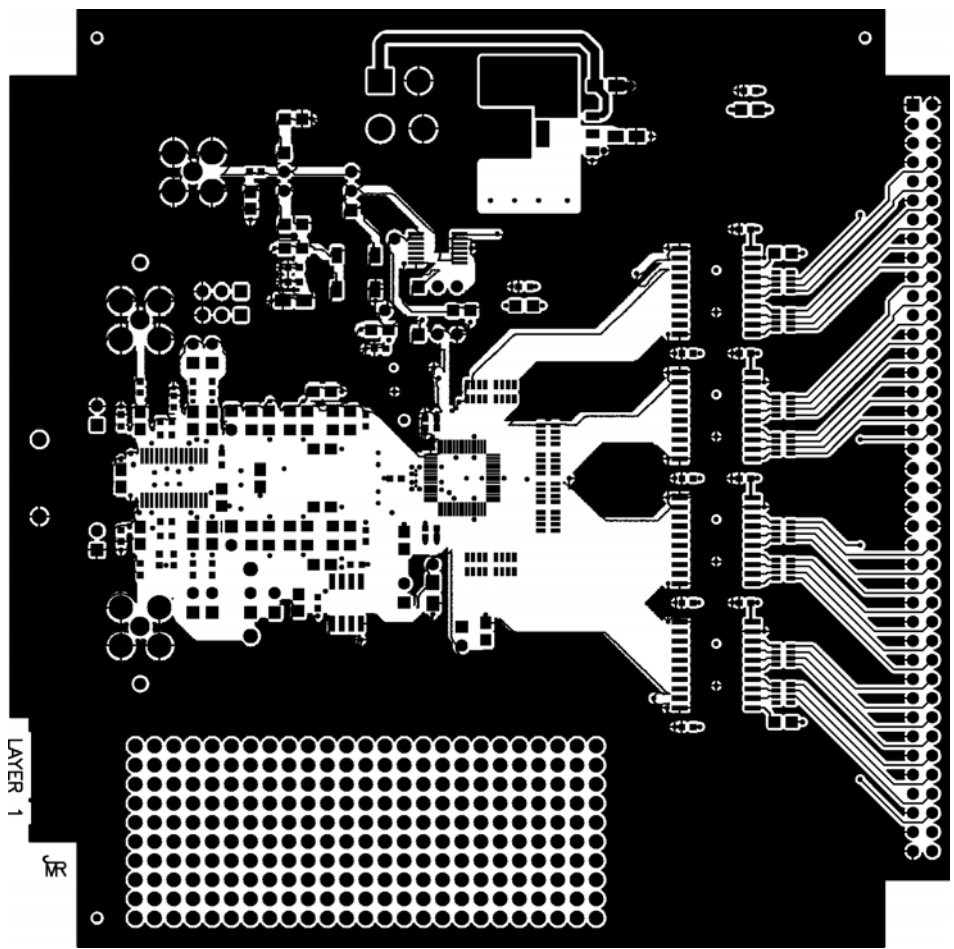Figure 14 through Figure 17 are the copper patterns for the board.
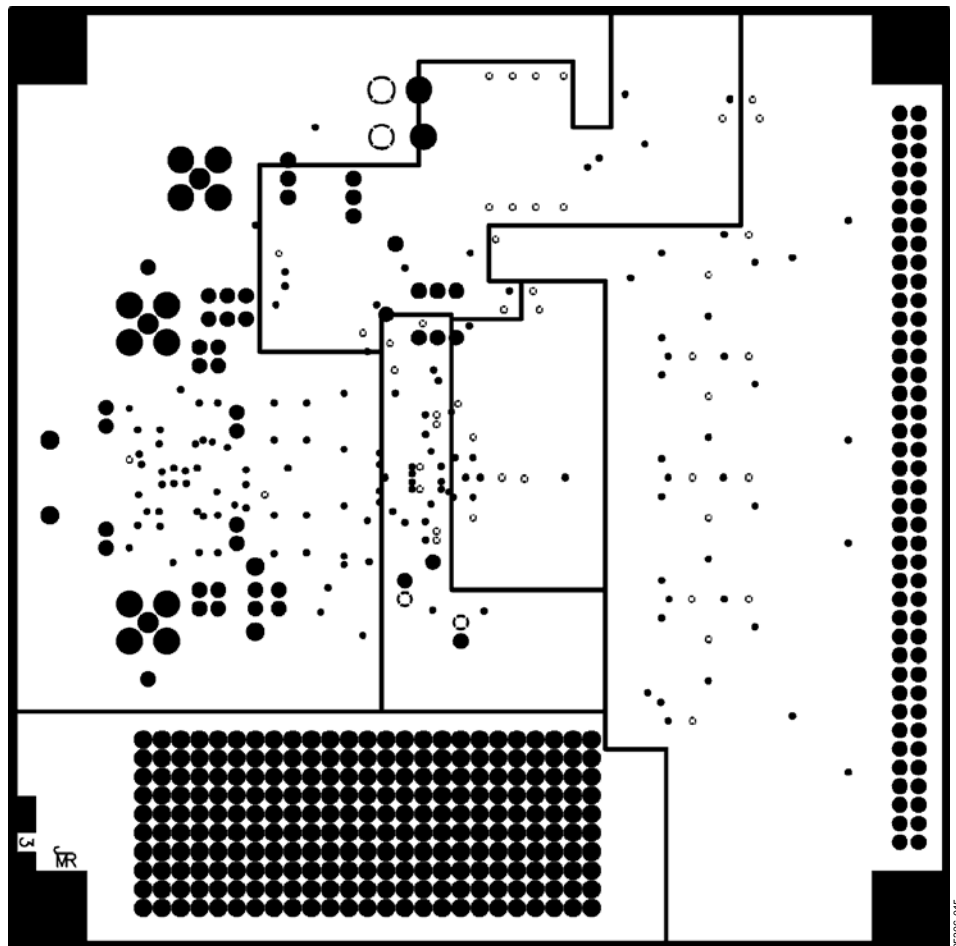


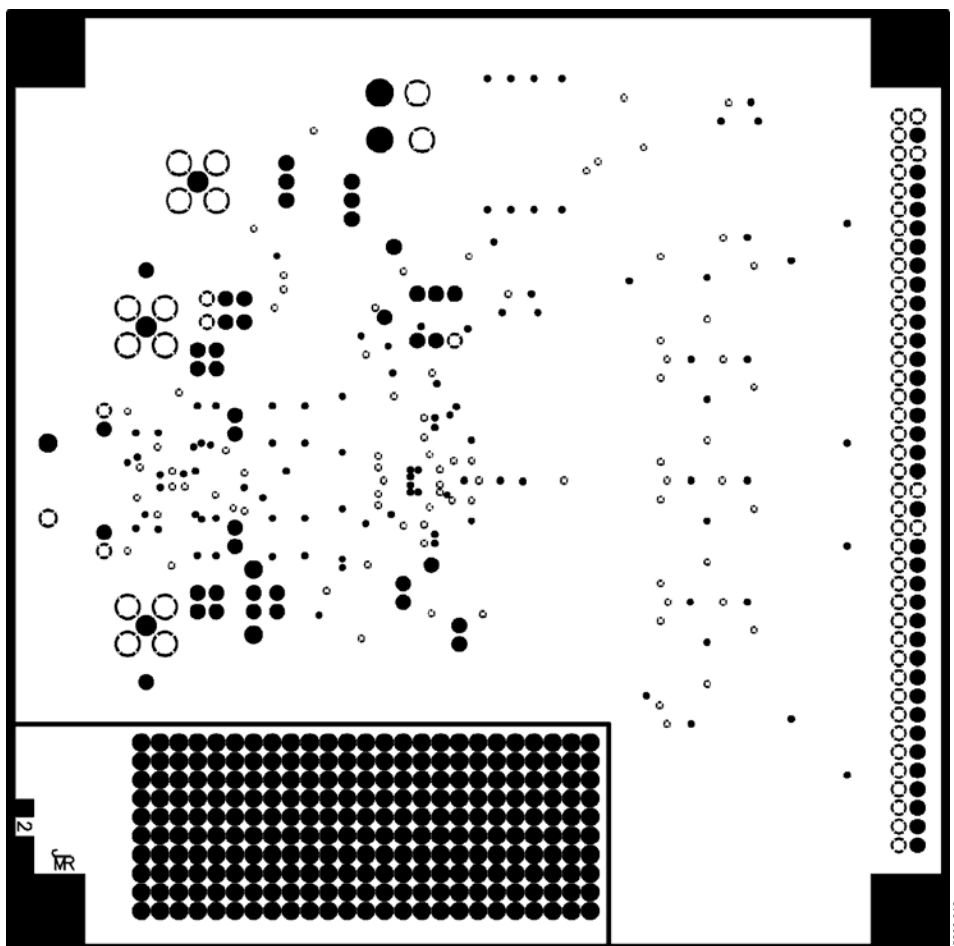Figure 14. Component Side Copper
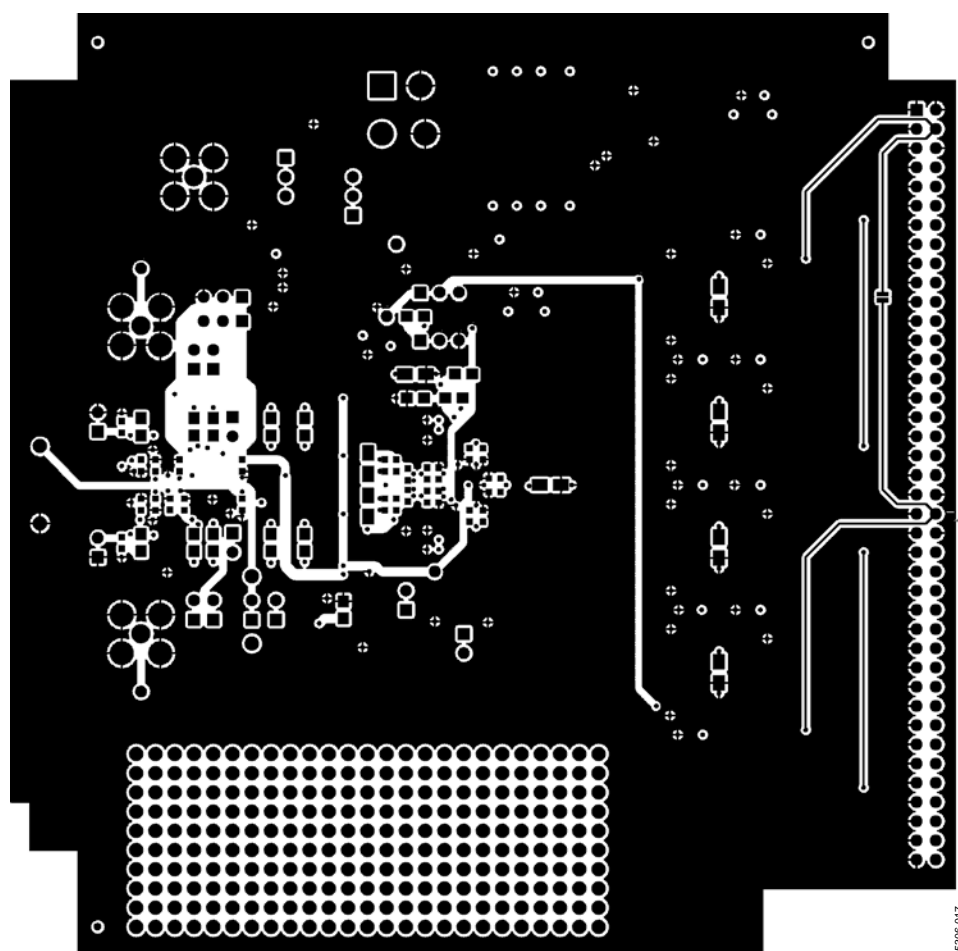
Figure 15. Layer 2 Copper

Figure 16. Layer 3 Copper

Figure 17. Wiring Side Copper

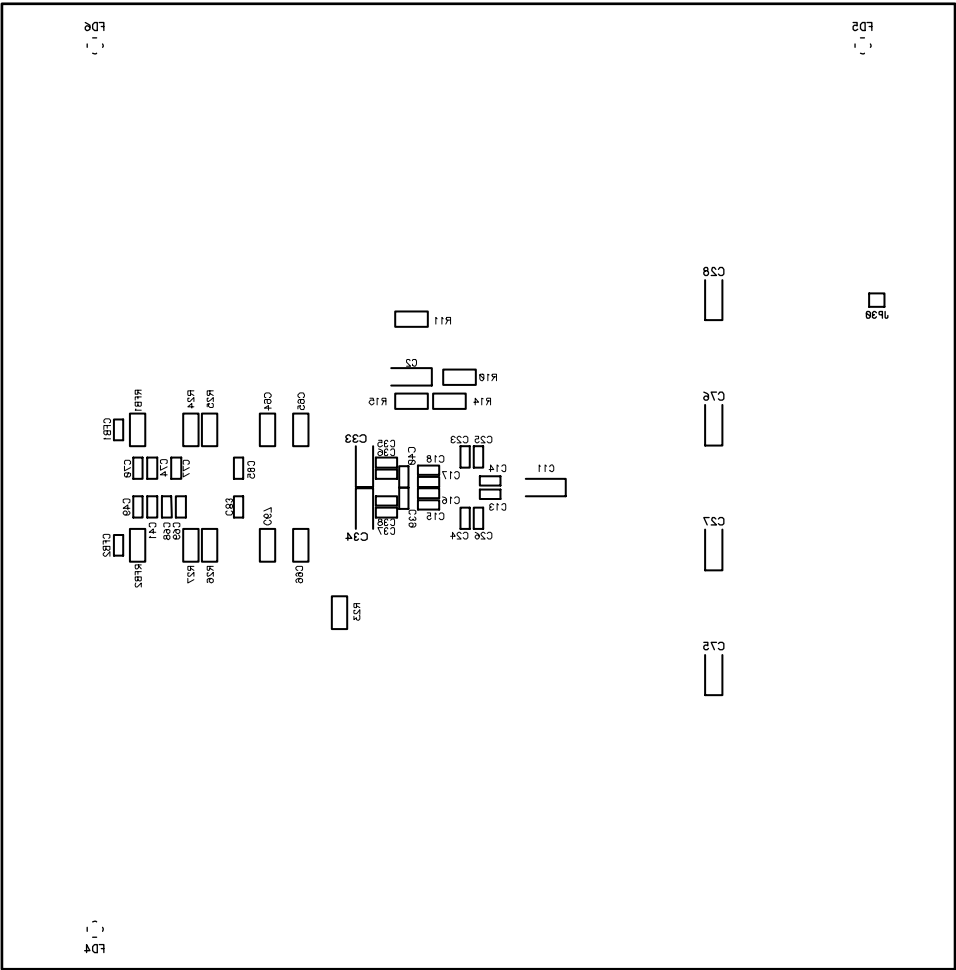*Figure 18. Component Side Silkscreen*

Figure 19. Wiring Side Silkscreen

# ORDERING INFORMATION

**Table 4. Parts List**

| Qty. | Name | Description | Reference Designator | Manufacturer | Manufacturer Part No. |
|---|---|---|---|---|---|
| 46 | Capacitor | 0.1 µF 16 V 0603 Ceramic | C1, 3–10, 14, 16, 17, 20, 22, 24, 26, 29–32, 35–43, 45, 48–51, 53–56, 58–60, 63, 69, 70, 72, 86 | Kemet | C0603C104K4RAC |
| 10 | Capacitor | Tantalum 10 µF 6.3 V A size | C2, 11, 12, 27, 28, 33, 34, 47, 75, 76 | Panasonic | ECS-T0JY106R |
| 12 | Capacitor | 1 nF 50 V 0603 | C13, 15, 18, 19, 21, 23, 25, 68, 74, 77, 78, 83, 85 | Panasonic | ECU-V1H102KBV |
| 2 | Capacitor | Tantalum 1 µF 16 V A size | C44, 46 | Kemet | T491A105K016AS |
| 2 | Capacitor | 10 nF, 6.3 V, 0201 | C52, 57 | Panasonic | ECJ-ZEB0J103K |
| 2 | Capacitor | 18 pF, 5%, NPO, 0603 | C61, 62 | Panasonic | ECJ-1VC1H180J |
| 2 | Capacitor | 22 pF 50 V 5% 0603 | C79, 80 | Panasonic | ECJ-1VC1H220J |
| 2 | Capacitor | 18 nF, 0603 | CFB1, 2 | Panasonic | ECJ-1VB1E183K |
| 1 | Header | 80 Ckt RA Male, 0.1" ctr, 2 row | J1 | Molex | 10-89-1806 |
| 5 | Header | 3 pin, 0.1" ctr | JP1, 2, 4, 15, 16 | Molex | 22-10-2031 |
| 6 | Header | 2 pin, 0.1" ctr | JP3, 5, 6, 11, 12, 17 | Mill Max | 400-10-002-10-001 |
| 8 | Resistor | 5% 1/10 W 0805 0 Ω | Insert in positions L1, 14–20 | Panasonic | ERJ-6ENF0.0 |
| 12 | Ferrite Bead | 120 nH, 0805 | L2–13 | Murata | BLM21BB750SN1 |
| 4 | Resistor | 1% 1/10 W 0805 1.5k Ω | R4, 12, 13, 21 | Panasonic | ERJ-6ENF1501V |
| 4 | Resistor | 5% 1/10 W 0805 33 Ω | R5–8 | Panasonic | ERJ-6GEYJ330V |
| 10 | Resistor | 0 Ω, 5%, 1/10 W, 0805 | R9, 10 (8 @ positions L1, 14–20) | Panasonic | ERJ-6GEY0R00V |
| 5 | Resistor | 100 Ω, 5%, 1/10 W, 0805 | R11, 24–27 | Panasonic | ERJ-6GEYJ101V |
| 3 | Resistor | 5% 1/10 W 0805 4.7 kΩ | R14, 20, 41 | Panasonic | ERJ-6GEYJ472V |
| 1 | Trimmer | 10 kΩ 3/8" SQ | R16 | BOURNS | 3299W-103 |
| 1 | Resistor | 49.9 Ω, 1%, 1/10 W, 0805 | R17 | Panasonic | 6ENF49R9V |
| 2 | Resistor | 499 Ω, 1%, 1/10 W, 0805 | R18, 19 | Panasonic | ERJ-6ENF4990V |
| 4 | Resistor | 1% 1/10 W 0805 1.5 kΩ | R4, 12, 13, 21 | Panasonic | ERJ-6ENF1501V |
| 2 | Resistor | 22 Ω, 5 %, 1/10 W, 0805 | R39, 40 | Panasonic | ERJ-6GEYJ220V |
| 2 | Resistor | 1% 1/10 W 0805 274 Ω | RFB1, RFB2 | Panasonic | ERJ-6ENF2740V |
| 16 | Network | 22 Ω Resistor | RN1–16 | CTS | 742C083220JTR |
| 3 | Connector | SMA Female PC Mount | S1, 2, 3 | Linx | CONREVSMA001 |
| 1 | Terminal | Block Split | TB1 | Wieland | 25.602.2253.0 |
| 4 | Test Pin | Vector | TP1, 2, 7, 8 | Vector | K24A |
| 1 | Test Pin | Loop, 0.093" dia., Red | TP3 | Bisco | TP-104-01-02 |
| 1 | Test Pin | Loop, 0.093" dia., Black | TP4 | Bisco | TP-104-01-00 |
| 5 | Test Pin | Loop, 0.038" dia., White | TP5, 6, 9, 12, 13 | Bisco | TP-105-01-09 |
| 1 | IC | ADC, 12 bit dual, 65 MSPS | U1 | Analog Devices | AD9238BST-65 |
| 4 | IC | Oct. Buffer | U2, 3, 7, 10 | Fairchild | 74VHC541M |
| 1 | IC | Dual VGA | U4 | Analog Devices | AD8332ARU |
| 1 | IC | Hex Inv | U5 | Fairchild | 74VHC04MTCX |
| 1 | Clock | 20 MHZ | U6 | Epson | SG-636PCE 20.0000MC0 |
| 1 | IC, Volt Reg. | 3.3 V Pos. Volt Reg. SOT-223 | VR1 | Analog Devices | ADP3339AKC-3.3 |
| 1 | PC Board | | | | |
| 4 | Hardware | Standoff 4–40 x 1/2" alum. | | | |
| 4 | Hardware | Screw 4–40 x 1/4" SS | | | |
| 5 | Jumper | Mini-jump jumper | Install at JP1, 2, 4, 15, 16 | FCI | 65474-001 |
| 1 | | Socket conn. strip | Part of TB1 | Wieland | Z5.530.0225.0 |

## ORDERING GUIDE

| Model | Description |
|---|---|
| EVAL-AD8332/AD9238 | Evaluation Board |

## ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

NOTES

ANALOG
DEVICES

www.analog.com

# Mouser Electronics

Authorized Distributor


Click to View Pricing, Inventory, Delivery & Lifecycle Information:


[Analog Devices Inc.](): 
  [AD9238BCP-65EBZ]()