Novel Architecture for Wireless Transducer Based Ultrasound Imaging System

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***Abstract*—In medical ultrasound scanning, coaxial cables connects the transducer elements to the computing platforms. During scanning, these probes are hanging from sonographer hand and slides on the patient body providing discomfort for both patient and sonographer. To address this issue, we discussed the feasibility of realizing wireless ultrasound transducer and as a proof of concept we built the prototype of wireless ultrasound transducer based scanning system. The proposed system has two parts: wireless transducer with embedded pre-processing unit, and back-end module for image reconstruction and display purpose. The embedded pre-processing unit consist of analog and digital integrated circuits, transmit beamforming, low noise amplification, time gain compensation and receive beam forming. The output of wireless transducer is scanline data, which is transmitted to back-end module via wireless communication transceiver. The complete back-end module is implemented on a Zedboard platform which comes with FPGA and ARM processor. The signal processing algorithms, which include envelope detection, log compression, scan conversion, interpolation and decimation algorithms are implemented on FPGA, while ARM processor is used to control and coordinate between signal processing modules. The Wi-Fi 802.11n standard is used as a wireless communication transceiver between wireless transducer and back-end module. The wireless transducer prototype is designed for 64 element, 8 channel linear transducer. The proposed prototype of wireless transducer based scanning system is successfully tested by scanning a phantom.**

I. Introduction

Ultrasound scanning, a non-invasive imaging technology works on the principle of transmitting ultrasound waves into the body and reconstructing the images of an organ based on the strength of received echo. The role of transducers in scanning involves, transmitting the ultrasound waves into the body and to sense the echoes coming from the tissues. The raw data acquired from transducers will undergo a series of signal processing algorithms to form the final image. The computing platforms like Field Programmable Gate Arrays (FPGAs), Digital Signal Processors (DSPs), System on Chip (SOCs) etc., [1]–[3] are used for implementing signal processing algorithms. To excite the transducer elements, and to traverse the sensed echo data from transducer elements to the computing platforms, coaxial cables (also called as probes) are used. The probe used in conventional ultrasound scanners is shown in Fig. 1. These probes are generally 1.5-2 m long. While scanning, these probes are hanging from sonographer hand, and sometimes sliding on the patients body, which is annoying for both patient and sonographer. The hanging ultrasound probes are extremely annoying in scenarios like real-time monitoring of complex brain surgeries, Anesthesiology, interventional procedures etc. ultrasound scanning in brain surgeries involves real-time detection of tumor traces present in brain that have to be removed, to guide interventional procedures for biopsies, in Anesthesiology, it is used to guide injecting needles in placing anesthesia near nerves.

Knowing the potentiality of addressing the problem, few patents conceptualizing the wireless ultrasound transducer are filed [4]–[6]. The ultrasound transducers will generate large volumes of data, which depends on parameters like sampling rate, ADC resolution, number of scan lines, number of channels and data acquisition time (depends on depth of scan). The medical ultrasound transducers operate in the frequency range 2 to 20 MHZ, and is typically sampled at 40 MHz frequency. Suppose if we are using 8 channel transducer, then the data generated from transducer will be:

$$\begin{aligned} Data\ generated &= N * F_s * R * D * S * F \\ &= 8 * 40 \times 10^6 * 14 * 65 \times 10^{-6} * 50 * 24 \\ &= 349.44 Mbps \end{aligned} \tag{1}$$

where N: number of channels (8), F_s: sampling frequency

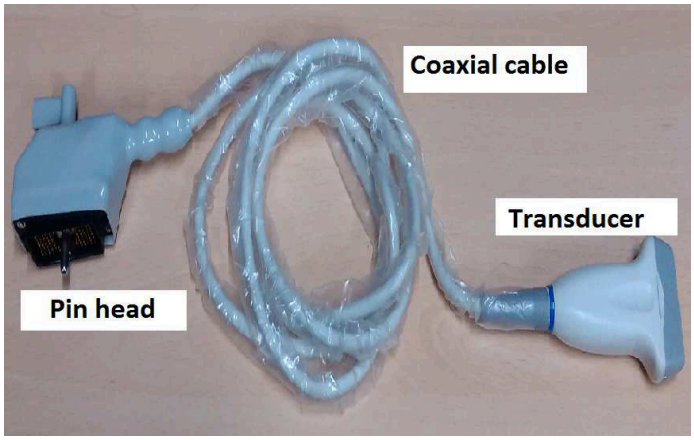

Fig. 1: Conventional ultrasound transducer probe

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(40 MHz), R: Analog to Digital Converter (ADC) resolution (14 bit), D: round trip time took by ultrasound wave to reach scanning depth (for 5 cm depth, D = 2*distance/velocity of sound), S: number of scan lines captured to form an image (50) and F: Frame rate (24). Here, data rate is generated by considering 8 channels and 5 cm depth. The data generated will further increase with increase in depth of scanning and number of channels. Present wireless communication technologies are not capable of supporting these high data rates. The wireless transducer is realizable only if we can reduce the volume of data generated from the transducer. This is achieved by implementing additional signal processing algorithms in the transducer itself before transmitting to the display device. The hardware architecture for wireless transducer is presented in [7], here FPGA embedded with transducer is used for performing entire ultrasound signal processing required for image reconstruction and final image is transferred to the monitor through wireless link for displaying the image. [8] proposed a framework for capturing the RF data from the transducer, beamform it and transmit to the server through Wi-Fi local area network for further processing. To reduce the data rate, compressed sensing based Xampling framework have been proposed in [9], [10]. Here, the RF data is sampled less than Nyquist rate which in turn reduces the number of samples required for image reconstruction, which can be transmitted to the server for image reconstruction.

In this work, we have proposed a novel standalone wireless ultrasound transducer architecture, which can generate and transmit the ultrasound wave into the body, capture the echo signal coming from the tissue, pre-process and transmit the data wirelessly to the computing platforms for image reconstruction. To reduce the data generation from the transducer, pre-ultrasound signal processing algorithms like noise filtering, Time Gain Compensation (TGC), beamforming are performed in the wireless transducer. The beamformed scan line data is transmitted to the Zedboard (Xilinx Inc., San Jose, CA) [11] through Wi-Fi 802.11n tranceiver. Envelope detection, log compression and scan conversion algorithms are implemented on the Zedboard for displaying the image on the monitor.

The rest of the paper is organized in the following way: in Section II, we discuss about the architecture of conventional ultrasound scanner and modifications made in the conventional architecture for realizing the wireless transducer. In Section III, we discuss experimental setup and hardware resource utilization of the algorithm. Section IV concludes the paper.

II. Wireless Ultrasound Imaging System

The block diagram representation of conventional ultrasound scanner is shown in Fig. 2. The transducer elements are interfaced to the High voltage (HV) pulser via co-axial cable. The end-terminal of the co-axial cable is terminated with pin-head, which act as an interface for connecting the computing platform. Based on the functionality, the B-mode ultrasound signal processing algorithms are categorized into front-end and back-end processing algorithms. Front-end processing algorithms include Transmit (Tx) and Receive (Rx) beamforming, low noise amplification, frequency filtering and TGC algorithms. In back-end processing, envelope detection, log compression, scan conversion, interpolation and decimation algorithms are performed. Generally, an ARM with any one of the co-processor like FPGAs, DSPs, SOCs, GPUs etc., are used as computing platforms for implementing entire ultrasound signal processing. Application specific integrated circuits are used for high voltage (HV) pulser, Tx beamformer and analog front end (AFE) for performing specific tasks in the imaging system. AFE includes low noise amplifier (LNA), voltage controlled amplifier (VCA) and programmable gain amplifier (PGA) operations.

The architecture of conventional ultrasound scanning system is modified to realize wireless ultrasound scanning system. The architecture of proposed wireless ultrasound transducer based imaging system is shown in Fig. 3 and Fig. 4 respectively. Fig. 3 represents front-end module with ultrasound transducer and preprocessing unit. The back-end module used for image reconstruction and for display purpose is shown in Fig. 4. Since ultrasound sensors generate huge amount of data, present wireless communication modules are not capable of supporting it [12]. To reduce the data rates, the entire front-end processing is performed within the transducer. Beamforming algorithm is the key component in front-end module that reduces the data rate significantly. Before beamforming, the data generated from the transducer for one scan line is of order $N \times S_a$, where $S_a = F_s \times D$ is the samples acquired by each element in the transducer. In beamforming, the data from all the channels are summed forming a scan line of dimension S_a. After beamforming, the dimension of data is reduced by a factor of number of channels (N:1). The data generated from transducer after beamforming will now be at 43.68 Mbps. This data can be transferred wirelessly to other computing platform through Wi-Fi 802.11n communication module. DSPs, FPGAs, GPUs, Media Processors etc., can be used as a computing platform for performing back-end processing. Here we have used FPGA along with ARM processor due to its high computational and programming capability.

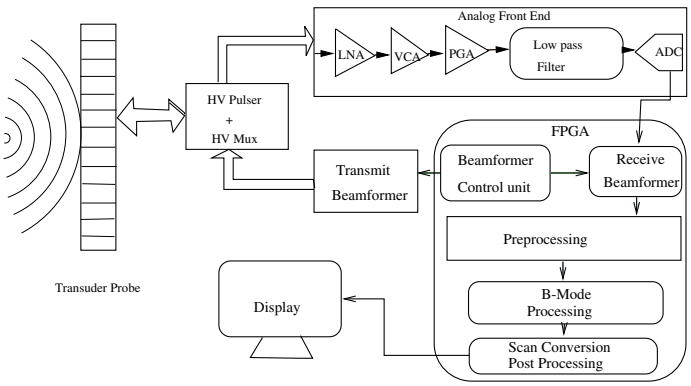

Fig. 2: Conventional ultrasound scanner

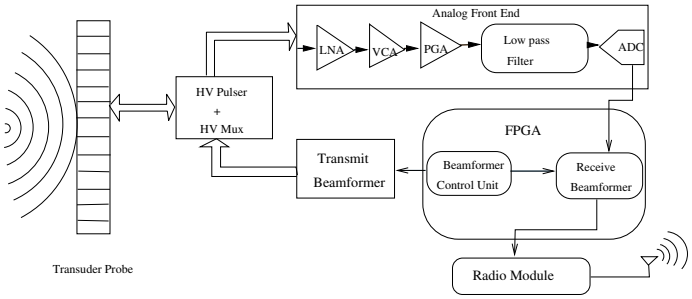

Fig. 3: Proposed Wireless Ultrasound Transducer Architecture.

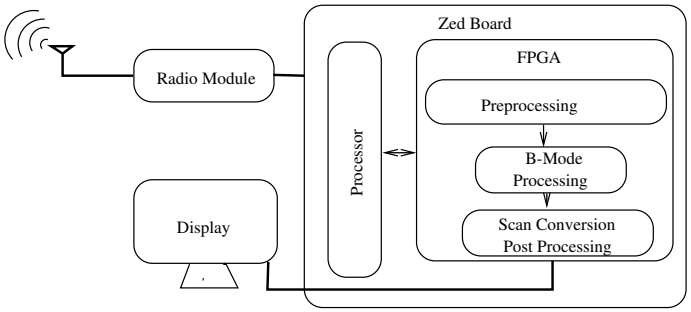

Fig. 4: Ultrasound Scanner Back-end Module

The functionality and implementation of proposed ultrasound imaging system are discussed below:

A. Implementation of Front-end module:

The ultrasound imaging system is designed for 8 channel linear transducer operating with center frequency 5 MHz. The ultrasound transducer elements need a voltage of $\pm 50V$ for excitation. The required voltage is supplied through HV pulser (Max 14808, Maxim Integrated, San Jose, CA) [13]. Tx and Rx beamforming algorithms in ultrasound is employed to get better signal to noise ratio of an echo signal, Tx beamforming includes the excitation of the transducer elements with a specific delay pattern such that the ultrasound waves will converge at a particular point known as focal point. In Rx beamforming, the echoes received from the elements are summed up accordingly depending on distance from the transducer element to the tissue of interest. In our previous work [14], we developed an ASIC for Tx and Rx beamforming algorithm for realizing the portable ultrasound scanner. The same ASIC is used here for implementing the beamforming algorithm. The beamformer IC generates the delay patterns for Tx beamforming, which is used for exciting the transducer elements via HV pulser. An integrated board with HV pulser, beamformer and AFE is shown in Fig. 5. The analog data from the transducer is sampled at 40 MHz using ADCs, low noise amplified and time gain compensated using analog AFE (AFE5808, Texas Instruments, Dallas, Texas) [15]. The data from AFE is given as input for beamforming IC to perform Rx beamforming. Beamformer IC is dynamically programmed through FPGA, After Rx beamforming, the scan line data is

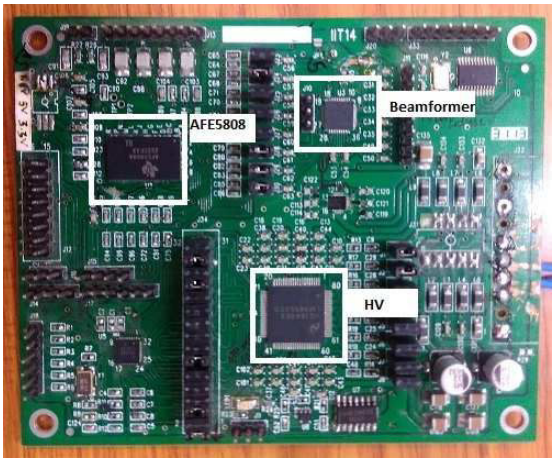

Fig. 5: Integrated board with Beamformer, AFE and HV pulser

transferred via Wi-Fi module, which is interfaced with ARM Cortex A9 processor. The ARM processor will control and coordinate between different processing modules present in wireless transducer. The FPGA and ARM processor present in Zedboard is used for this purpose.

B. Back-end processing module:

Zedboard is used as a terminal device for capturing the beamformed data from wireless transducer, process and display it on the monitor. Back-end algorithms are implemented on the FPGA platform. ARM processor is used to display the processed echo data as an image on the monitor. The Zedboard is interfaced with Wi-Fi communication module to capture the scan line data from the front-end module.

The back-end processing algorithms are performed on the FPGA. In scan line data, only the peaks of RF data conveys the properties of tissue, to detect the peaks, envelope detection is employed. For computing the envelope detection, Hilbert transform based approach is used. The complete FPGA implementation of envelope detection can be found from our previous work [16]. The envelope detected data has high dynamic range, if we map RF data in gray scale range 0 to 255, most of the values will fall in the range 0 to 9 and we can not infer diagnostic information from the image. Non-linear compression techniques like log function is used to reduce the dynamic range of RF data. To reduce the computation burden, Look Up Table (LUT) based approach is used for log compression. In linear excitation, the RF data is localized in rectangular coordinate system, and in beam steering, the RF data is localized in polar coordinate system. If the RF data is in polar coordinate system, then it has to be converted into rectangular coordinate system for displaying it on the monitor. LUT based approach is used for coordinate transformation. The scan line data is inadequate to display on the monitor, to overcome this, bilinear interpolation is employed to increase the number of scan lines. After interpolation, the decimation operation is performed on individual scan line to fit to the resolution of a monitor. To display RF data as an image on

the monitor, a buffer matrix is created in SDRAM of ARM processor. A GUI application is developed using GTK+2.0 libraries [17]. The GTK toolkit allows the stored buffer to be displayed as gray scale image on the monitor. If new frame arrives it overwrites the existing frame in SDRAM of the ARM processor.

III. Results

The prototype of proposed wireless transducer is shown in Fig. 6. The setup is scanned using a non-homogeneous gelatin phantom immersed in water. The phantom is of circular dimension with 8 cm depth, 6 cm diameter. The phantom is scanned for a depth of 5 cm $\times$ 5 cm. The specifications of transducer used for scanning the phantom is shown in Table. I. The hardware setup used for image reconstruction and display is shown in Fig. 7, here Zedboard is interfaced with Wi-Fi and monitor. The Zedboards in both front-end and back-end module are running with Xillinux operating system with 667 MHz clock frequency, 512 RAM.

TABLE I: Parameters used for scanning the gelatin phantom

Specifications	Value
Transmit frequency	5 MHz
Number of channels	8
Kerf of transducer	0.035mm
Element width	0.185mm
Depth of scan	50mm
Focus Depth	30mm
Elevation aperture	4.5mm
Number of scan lines	50

The transducer is linearly excited for acquiring the image of a phantom. The reconstructed ultrasound image of a phantom is shown in Fig. 8. The resources utilized in FPGA for implementing the back-end processing algorithms including envelope detection, log compression, scan conversion, interpolation and decimation operations are analyzed using the Xilinx ISE 14.4 synthesis tool, and this is summarized in Table. II. For implementing backend algorithms 2946 slice registers, 2352 slice LUTs flops, 30 block RAM (BRAM) are utilized in FPGA.

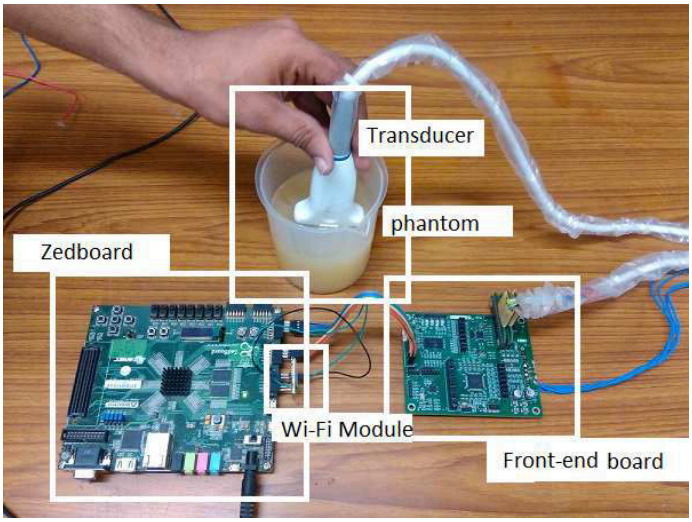

Fig. 6: Wireless ultrasound transducer setup

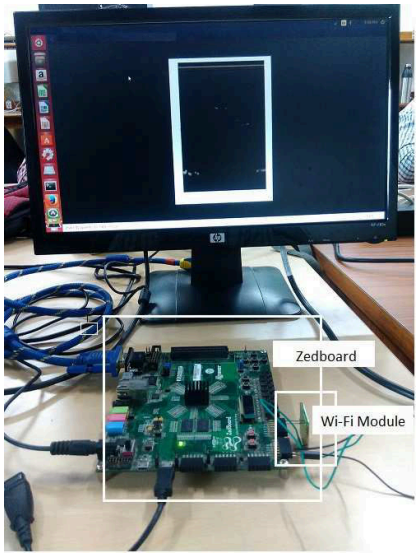

Fig. 7: Proposed back-end module

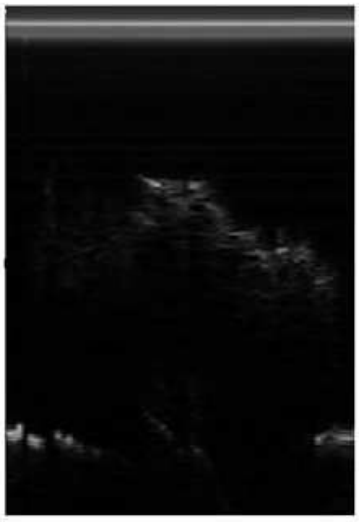

Fig. 8: Reconstructed ultrasound phantom image

IV. Discussion and Conclusion

In this work, we proposed a novel wireless transducer architecture for ultrasound imaging. The proposed architecture is designed for B-mode imaging, since it is widely used imaging mode. The wireless transducer prototype is realized using wired ultrasound transducer and shown that we can achieve wireless transducer for ultrasound scanning system. The proposed architecture is developed for scanning a maximum depth of 6 cm. This is very much sufficient for scanning superficial structures like carotid artery, thyroid, knee etc,. For higher scanning depths, the data generated from the transducer

TABLE II: Resource utilized by FPGA present in Zedboard for implementing back-end processing algorithms.

Resources Available	Resource Used	Percentage
Slice Logic Utilization		
Number of Slice Registers (106400)	2946	2 %
Number of Slice LUTs (53200)	3359	6%
Number used as Logic(53200)	2938	5%
Slice Logic Distribution		
Number of LUT Flip Flop pairs used	3780	
Number with an unused Flip Flop (3780)	1007	27%
Number with an unused LUT (3780)	421	12%
Number of fully used LUT-FF pairs (3780)	2352	62%
Number of unique control sets	61	
IO Utilization		
Number of IOs (200)	34	17 %
Number of Block RAM/FIFO (140)	30	21 %
Number of BUFG /BUFGCTRLs (32)	8	25 %

will be high and the employed transceiver is not capable of transmitting these data, in these scenarios a buffer can be employed at the transmitter side to store the data and transmit to the other end for backend processing. Buffering and transmitting the data adds delay in displaying the images on the monitor. Recent trends in compressive sensing is also useful in reducing the data acquisition rates but comes with additional computations at receiver side, which can be afforded with present computational technologies. In this paper, we powered the transducer with regulated power supply, while in wireless transducer, the powering issues can be addressed with voltage boosters along with batteries. Here we have shown how wireless transducer for ultrasound imaging can be achieved with modification in hardware architecture. Since, we focused on developing the system as a proof of concept, we have used two Zedboards in front-end and back-end models, which is expensive and can also be realizable with other computational platforms.

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