Department of Electronic and Telecommunication Engineering

University of Moratuwa

EN3030 - Circuits and Systems Design

Instruction Set Architecture (ISA)

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A custom CPU is to be designed for a matrix multiplication. The following specifications of the CPU have been given to you.

- CPU process 16-bit Data.
- The CPU can access 64k words of memory, each word being 16-bits wide.
- The CPU does this by outputting a 16- bit address on its output pins A[15…] and reading in the 16-bit value from memory on its inputs D[15…]
- The CPU contains an 16-bit address register(AR), an 16-bit accumulator(AC), 5-bit instruction register, 16-bit data register(DR),16-bit general purpose registers (RA,RB,RC,R1,R2,R3) and an 1-bit zero flag (Z)
- Note that T is a 16-bit value stored in the location immediately following that instruction.

Instruction	**Instruction Code**	**Operation**
NOP	00000XXXXXXXXXX	No operation
LDAC	00001XXXXXXXXXX T	AC ← M[T]
LDACRA	00010XXXXXXXXXX	AC ← M[RA]
LDACRB	00011XXXXXXXXXX	AC ← M[RB]
LDACRC	00100XXXXXXXXXX	AC ← M[RC]
LDRA	00101XXXXXXXXXX T	RA ← M[T]
LDRB	00110XXXXXXXXXX T	RB ← M[T]
LDRC	00111XXXXXXXXXX T	RC ← M[T]
STAC	01000XXXXXXXXXX	M[T] ← AC
STACRA	01001XXXXXXXXXX	M[RA] ← AC
STACRB	01010XXXXXXXXXX	M[RB] ← AC
STACRC	01011XXXXXXXXXX	M[RC] ← AC
MVACR1	01100XXXXXXXXXX	R1 ← AC
MVACR2	01101XXXXXXXXXX	R2 ← AC
MVACR3	01110XXXXXXXXXX	R3 ← AC
JPNZ	01111XXXXXXXXXX	IF Z=0, then go to T
ADDR3	10000XXXXXXXXXX	AC ← AC+R3, IF (AC+R3=0) THEN Z ← 1 ELSE Z ←0
SUB1	10001XXXXXXXXXX	AC ← R1-AC, IF (R1-AC=0) THEN Z ← 1 ELSE Z ←0
SUB2	10010XXXXXXXXXX	AC ← R2-AC, IF (R2-AC=0) THEN Z ← 1 ELSE Z ←0
INAC	10011XXXXXXXXXX	AC ← AC+1
INCRA	10100XXXXXXXXXX	RA ← RA+1
INCRB	10101XXXXXXXXXX	RB ← RB+1
INCRC	10110XXXXXXXXXX	RC ← RC+1
CLAC	10111XXXXXXXXXX	AC ← 0
MULT3	11000XXXXXXXXXX	AC ← AC*R3