ME 420 – MECANICAL ENGINEERING RESEARCH PROJECT

Registration number: E/17/286

Project Title: Configurable neuromorphic processor architecture for spiking neural networks

Project Objectives:

1. To design and implement a configurable neuromorphic processor architecture for spiking neural networks.
2. To implement a RV32IM pipelined CPU in Verilog as a starting point for the design.
3. To complete the current RISC-v NoC (Network on Chip) FPGA implementation for SNNs and integrate it into the processor architecture.
4. To create a test SNN application to verify the functionality and performance of the processor architecture.
5. To evaluate the power consumption and speed of the configurable neuromorphic processor architecture and compare it with existing solutions in the literature.

Learning Objectives:

1. To gain a deep understanding of the principles and concepts of spiking neural networks and neuromorphic computing.
2. To become familiar with the RISC-V instruction set architecture and its implementation in hardware.
3. To gain experience in developing and testing SNN applications.
4. To understand the trade-offs between power consumption, performance, and area in processor architecture design.

Date: 05.05.2023 Signature of a student……

Name of the supervisor: Dr Isuru Nawinne

Signature……..

Name of the supervisor: Dr Mahanama Wickremasinghe

Signature……..

Name of the supervisor: Prof Roshan Ragel

Signature……