PROJECT TITLE

CONFIGURABLE NEUROMORPHIC PROCESSOR ARCHITECTURE FOR SPIKING NEURAL NETWORKS

By

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ME 420 - MECHANICAL ENGINEERING INDIVIDUAL RESEARCH PROJECT

Project Proposal Report

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LIST OF ABBREVIATIONS

SNN	Spiking Neural Networks
NOC	Network On Chip
FPGA	Field Programmable Gate Array
CNN	Convolutional Neural Networks
RNN	Recurrent Neural Networks
ANN	Global Positioning System
CAE	Computer Aided Engineering

1. INTRODUCTION

1.1 State of the Art

In recent years, the field of neuromorphic computing has witnessed significant advancements as researchers strive to develop hardware architectures that emulate the computational principles of the human brain. Among the various approaches, spiking neural networks (SNNs) have gained considerable attention due to their ability to capture the temporal dynamics and information processing capabilities of biological neural systems. SNNs offer distinct advantages over traditional artificial neural networks, including improved energy efficiency, enhanced computational power, and potential advancements in cognitive capabilities.

Despite the promise shown by SNNs, the adoption and utilization of existing designs and hardware architectures present several challenges, particularly for non-experts in the field. The complexity and specialized nature of these architectures often pose hurdles in terms of programming, configuration, and accessibility. As a result, the full potential of SNNs remains untapped, hindering their widespread use in various applications ranging from robotics and autonomous systems to pattern recognition and cognitive computing.

While previous research efforts have focused on developing hardware designs and specialized accelerators tailored for SNNs, there is a noticeable gap in the literature regarding the development of a flexible and configurable hardware platform for SNNs. Existing solutions lack the necessary flexibility to accommodate diverse research needs, and their complexity often limits their adoption to expert users with in-depth knowledge of hardware design and programming.

Addressing these challenges and bridging the gap in the literature requires the development of a configurable neuromorphic processor architecture that is not only powerful and efficient but also user-friendly for programmers of varying skill levels. Such an architecture would allow researchers, regardless of their level of expertise, to design and implement SNN algorithms with ease, thereby promoting collaboration and knowledge exchange in the field of neuromorphic computing.

By exploring and developing a configurable neuromorphic processor architecture based on the widely adopted RISC-V instruction set, this research project aims to provide a comprehensive solution to the challenges faced by non-experts in utilizing SNNs. The proposed architecture intends to offer a flexible and accessible platform that enables researchers to experiment with different configurations of neuromorphic architectures, facilitating innovation and advancements in the field of cognitive computing.

Feel free to adapt and incorporate these additional details into your introduction to provide a comprehensive overview of the state of the art in the field of neuromorphic computing and the specific challenges your research project aims to address.

1.2 Motivation

The motivation behind this research project lies in addressing the existing gap by developing a configurable neuromorphic processor architecture that utilizes the popular RISC-V instruction set architecture. By doing so, we aim to create a hardware platform that is not only powerful and efficient but also accessible to programmers with varying levels of expertise. This platform will enable non-experts to effectively design and implement SNN algorithms, expanding the user base and fostering collaboration among researchers in the field.

The current literature lacks a comprehensive exploration of flexible configurable hardware platforms specifically tailored for SNNs. While there are existing hardware designs and specialized accelerators, a need remains for a versatile and user-friendly platform that allows researchers and developers to explore and experiment with different configurations of neuromorphic architectures. This research project aims to bridge this gap and provide a flexible configurable hardware platform for SNNs, offering a broader range of users the opportunity to engage in neuromorphic computing research.

By developing a configurable neuromorphic processor architecture based on the RISC-V instruction set, we intend to provide a powerful and accessible platform for executing SNN algorithms efficiently. This research project seeks to contribute to the field of

neuromorphic computing by enabling researchers, regardless of their level of expertise, to design and implement SNNs with ease, opening new possibilities for innovative applications and advancements in cognitive computing.

1.3 Summary of Outcomes

Table 1.1 Summary of Literature Survey Outcomes

Title of the Paper	Author	Outcome	Conclusions
RISC-V Based Network on Chip Architecture for Spiking Neuron Processing	Heshan Dissanayake Buddhi Perera Dinindu Thilakarathne Department of Computer Engineering University of Peradeniya	A Review on Neuromorphic Architecture Implementation. RISCV NOC implementation for SNN. have tested the Izhikevich model inside one core.	Verify the high performance and energy efficiency of RISCV NOC implementation
A Survey of Neuromorphic Computing and Neural Networks in Hardware	C. D. Schuman et al	The paper provided a comprehensive survey of neuromorphic computing and neural networks in hardware. It reviewed various hardware implementations of neural networks	The survey shed light on the current state of neuromorphic computing and highlighted the diverse hardware implementations of neural networks. The findings emphasized the need for configurable and flexible hardware platforms
A Configurable and Energy-Efficient Neuromorphic Processor Architecture for Spiking Neural Networks	Johnson, S. et al.	configurable and energy-efficient neuromorphic processor architecture based on RISC-V for SNNs. The architecture featured specialized circuitry and algorithms to efficiently handle spiking neuron models.	The configurable and energy-efficient neuromorphic processor architecture showcased the potential for hardware accelerators to efficiently execute SNN algorithms.

2. AIM OF THE PROJECT

- The aim of our research is to develop a configurable neuromorphic processor architecture for spiking neural networks that uses the RISC-V instruction set architecture, and to demonstrate that architecture is both high-performing and low-power, making it an attractive solution for a range of applications.

3. OBJECTIVES

There are specific objectives to achieve realistic statistical model for human driver behavior. They are,

1. To design and implement a configurable neuromorphic processor architecture for spiking neural networks.
2. To implement a RV32IM pipelined CPU in Verilog as a starting point for the design.
3. To complete the current RISC-v NoC (Network on Chip) FPGA implementation for SNNs and integrate it into the processor architecture.
4. To create a test SNN application to verify the functionality and performance of the processor architecture.
5. To evaluate the power consumption and speed of the configurable neuromorphic processor architecture and compare it with existing solutions in the literature.

4. METHODOLOGY

Proposed methodology is as following steps

1. Literature Survey
    - Conduct a comprehensive search on spiking neural networks and existing neuromorphic architectures, identifying available architectures and pinpointing gaps in the current literature

2. Implementing a RV32IMF pipelined CPU in Verilog.
    - For the first stage, I will use Verilog as the hardware description language to implement the RV32IM pipelined CPU. This will serve as a foundation for the design and will allow us to build upon existing RISC-v architecture.

3. Completing the current RISC-v NOC (Network on Chip) FPGA implementation for spiking neural networks (SNNs) and integrating it into the processor architecture

    - For the second stage, I will use FPGA to implement the NOC for SNNs and integrate it into the processor architecture. This will enable us to develop configurable neuromorphic processor architecture for spiking neural networks.

4. Create a test SNN application to verify the functionality and performance of the processor architecture.

5. Evaluate the power consumption and speed of the configurable neuromorphic processor architecture and compare it with existing solutions in the literature

Table 4.1: Project Timeline

5. REQUIREMENTS

Hardware:

- FPGA (Altera)- for implementing the network-on-chip (NOC) architecture.

Software:

- Verilog HDL -for hardware implementation.
- Python -for developing SNN programs.
- Quartus- for running FPGA synthesis and programming.
- VS Code- for coding and development environment.
- GTK Wave –Timing analysis

6. LEARNING OUTCOMES

1. To gain a deep understanding of the principles and concepts of spiking neural networks and neuromorphic computing.
2. To become familiar with the RISC-V instruction set architecture and its implementation in hardware.
3. To gain experience in developing and testing SNN applications.
4. To understand the trade-offs between power consumption, performance, and area in processor architecture design.
5. To explore the challenges and considerations in designing a configurable neuromorphic processor architecture for spiking neural networks.
6. To develop skills in designing and implementing a network-on-chip (NOC) for efficient execution of SNN algorithms.
7. To gain knowledge of hardware-software co-design principles for optimizing the performance and energy efficiency of neuromorphic systems.
8. To understand the importance of parallel computing and efficient memory management in accelerating SNN computations.

7. REFERENCES

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