# ME 420 – MECANICAL ENGINEERING RESEARCH PROJECT

Registration number: E/17/286

Project Title: Configurable neuromorphic processor architecture for spiking neural networks

Outcomes of the Project:

1. Design and implement a configurable neuromorphic processor architecture for spiking neural networks.
2. Create a test SNN application to verify the functionality and performance of the processor architecture.
3. Evaluate the power consumption and speed of the configurable neuromorphic processor architecture and compare it with existing solutions in the literature.

Milestones of the project (For Semester 8):

1. Enhance the RV32IMF Pipelined CPU to include support for the Network-on-Chip (NOC) and interrupts.
2. Implement a Network on Chip Architecture (NoC)with RV32IMF pipelined CPU
3. Create a test SNN application to verify the functionality and performance and power consumption of the processor architecture.

Project timeline tagged with the milestones:

| No | Task | Week | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 23-Aug | | | 23-Sep | | | | 23-Oct | | | | 23-Nov | | | | 23-Dec | |
| | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 |
| 1 | Enhance the RV32IMF Pipelined CPU for NOC | | | | | | | | Mid Demostration | | | | | | | | | Final Presentation and Demostration | |
| 2 | Implement a Network on Chip Architecture (NoC)with RV32IMF pipelined CPU | | | | | | | | | | | | | | | | | | |
| 3 | Create a test SNN application to verify the functionality and performance and power | | | | | | | | | | | | | | | | | | |
| 4 | Final Report | | | | | | | | | | | | | | | | | | |
| 5 | Final Presentation | | | | | | | | | | | | | | | | | | |

Date: 10.08.2023 Signature of a student.....

Name of the supervisor: Dr Isuru Nawinne

Signature.....

Name of the supervisor: Prof Roshan Ragel

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