



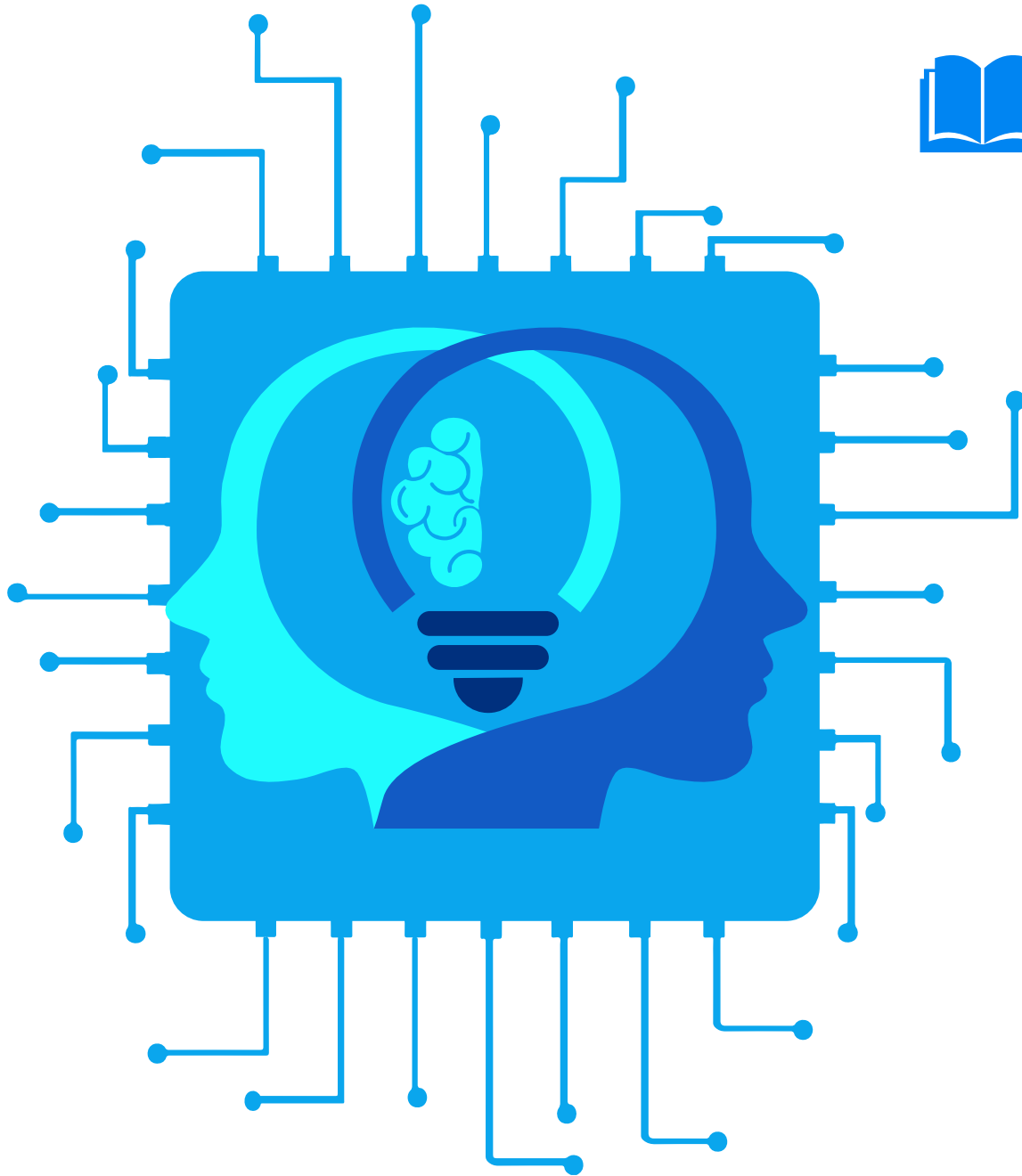
CONFIGURABLE NEUROMORPHIC PROCESSOR ARCHITECTURE FOR SPIKING NEURAL NETWORKS

E/17/286

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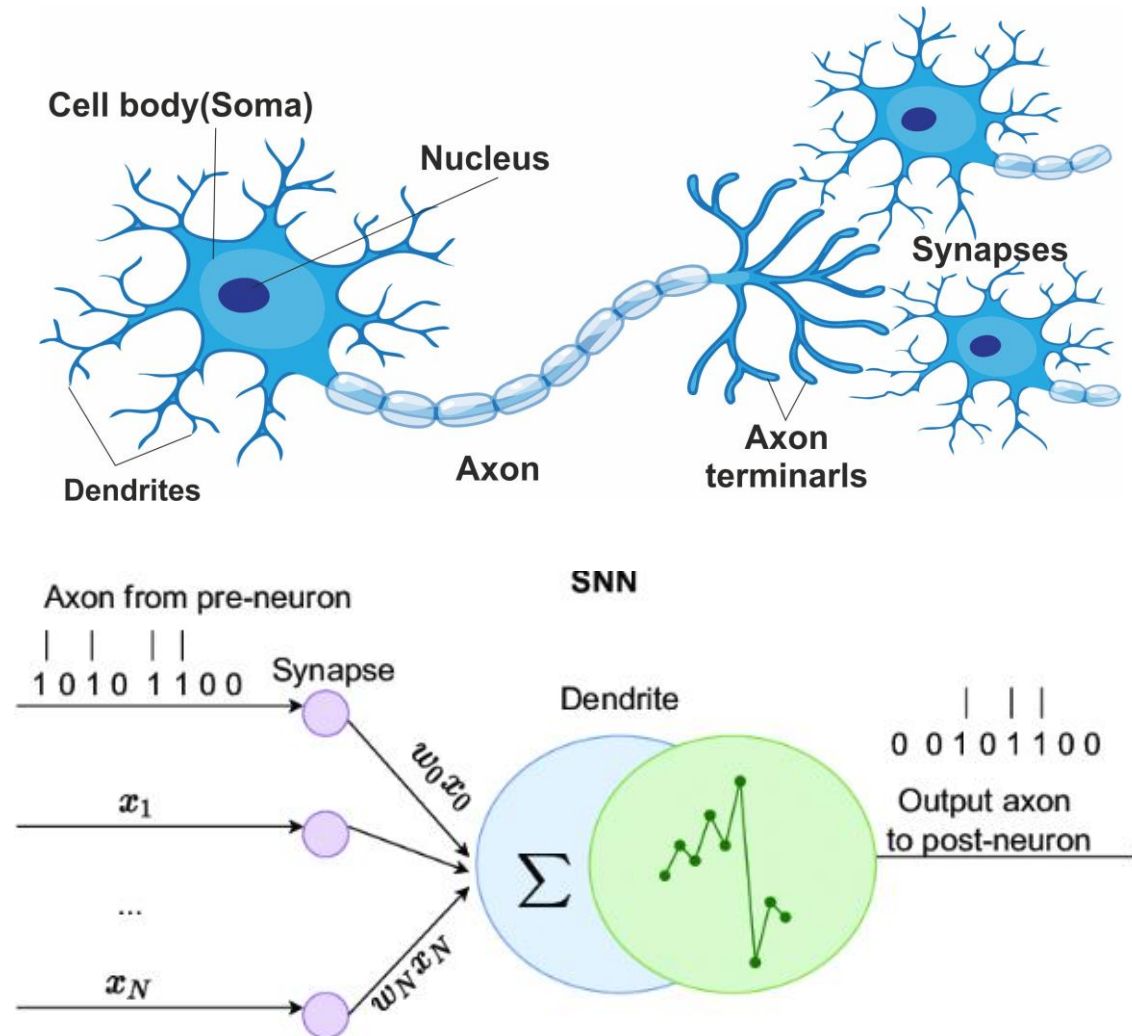
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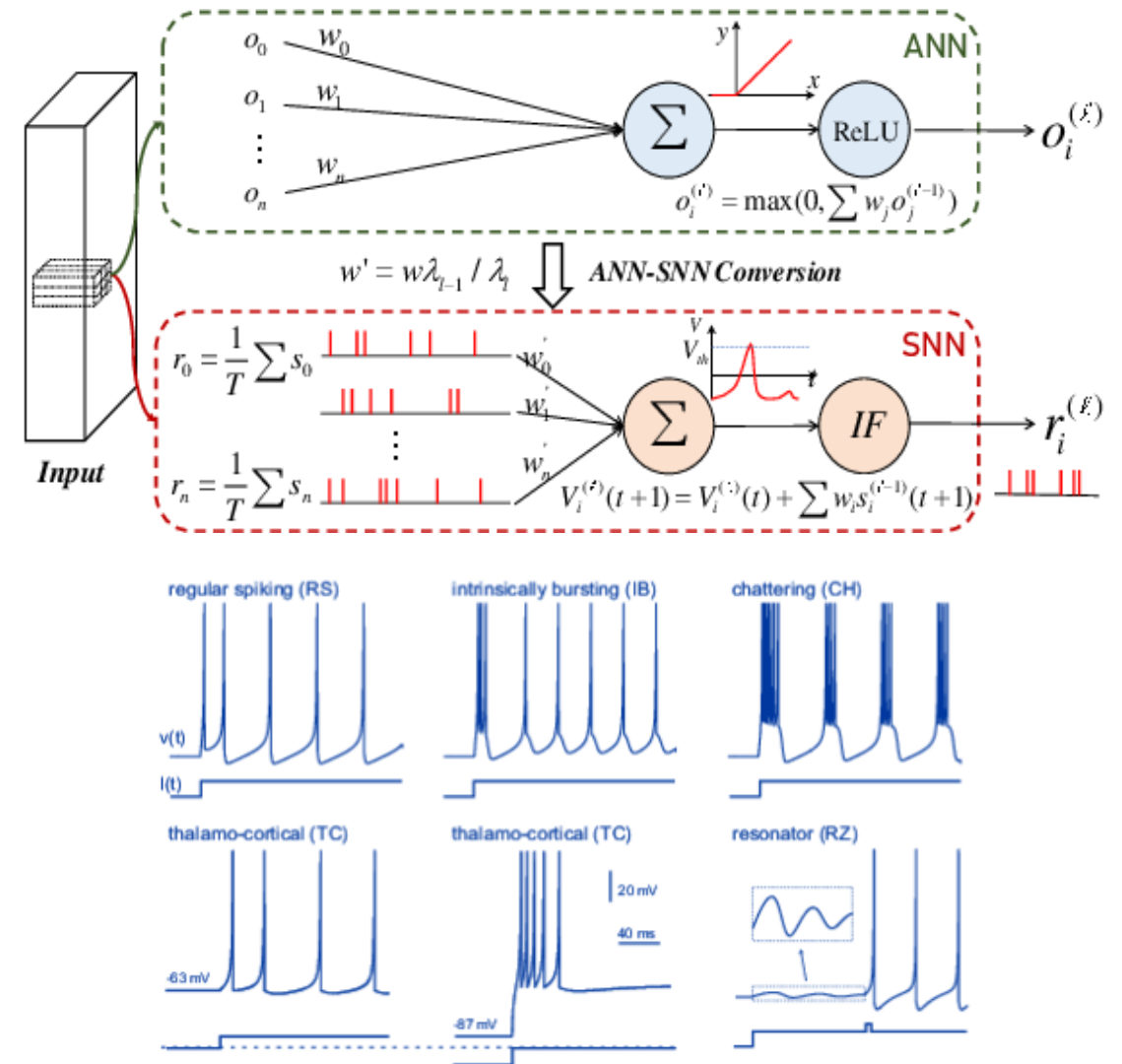
INTRODUCTION-SNN

- ❖ Spiking neural networks (SNNs) are a type of neural network that simulate the behavior of biological neurons and synapses.
- ❖ The significance of SNNs lies in their ability to mimic the behavior of biological neural networks and in their potential for improving machine learning and artificial intelligence.
- ❖ The basic components of an SNN include neurons, synapses, and input/output spikes.



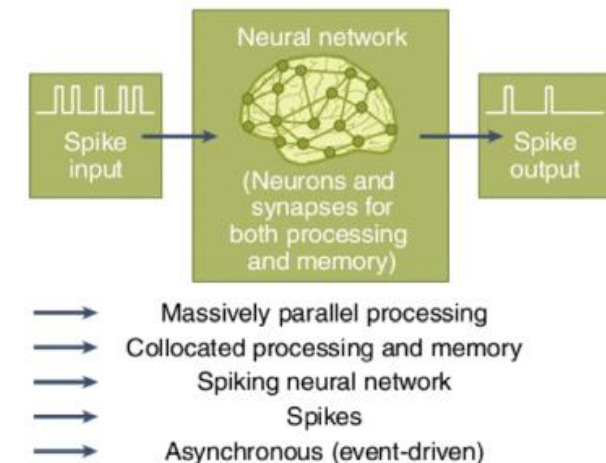
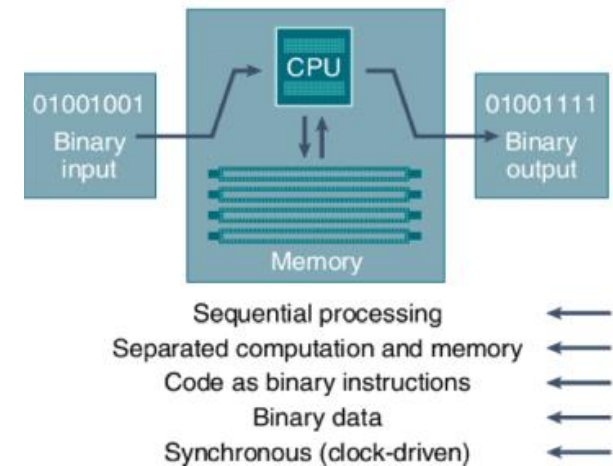
INTRODUCTION-SNN

- ❖ Unlike traditional artificial neural networks (ANNs), which use abstract mathematical models, SNNs process information through the timing and frequency of spikes.
- ❖ SNNs can be used for a variety of applications, such as speech recognition, image processing, and robotics.
- ❖ Compared to ANNs, SNNs offer potential advantages such as better energy efficiency and higher accuracy.



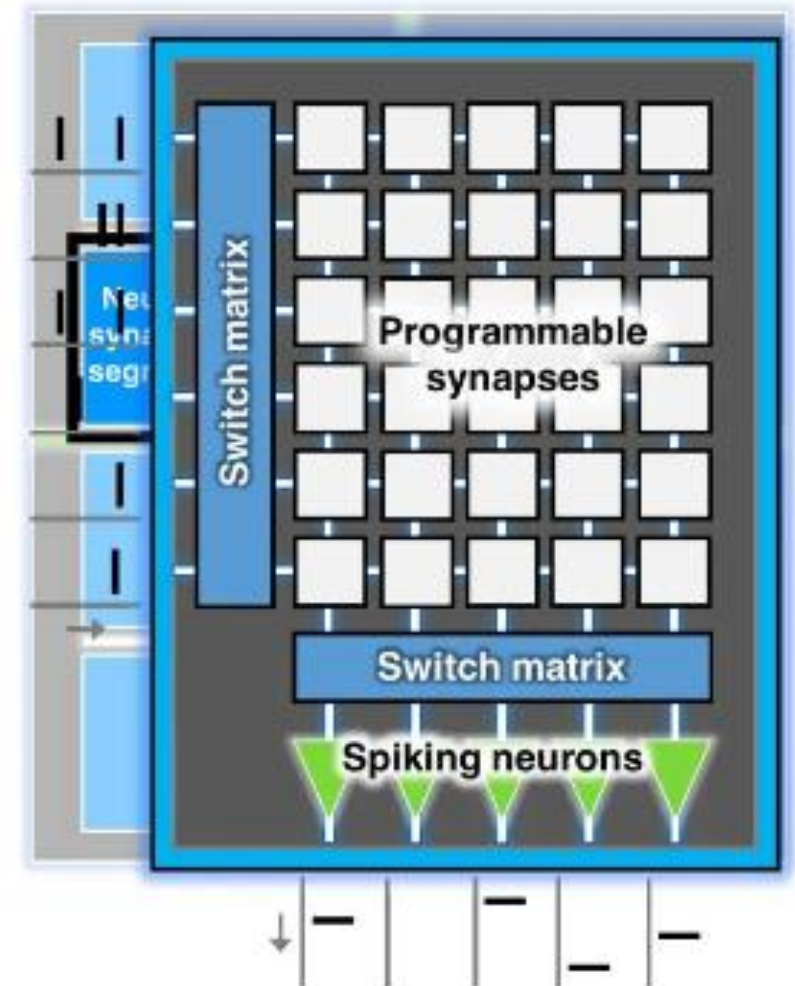
Neuromorphic computing

- ❖ Neuromorphic computing is an approach to computing that uses hardware and software inspired by the principles of the [human brain](#).
- ❖ The goal of neuromorphic computing is to develop computers that can perform complex tasks with [energy efficiency](#) and robustness similar to that of biological neural networks.
- ❖ Compared to traditional [von Neumann](#) architecture, neuromorphic computing offers potential advantages such as [lower power consumption](#), [faster processing](#), and more efficient use of memory



Neuromorphic computing

- ❖ Neuromorphic computing can be implemented using **digital, analog, or mixed-signal circuits**, as well as with specialized hardware such as memristors.
- ❖ Neuromorphic computing has potential applications in areas such as machine learning, robotics, and brain-computer interfaces.
- ❖ The significance of neuromorphic computing lies in its potential to revolutionize computing by enabling machines to process information in ways that are more **natural and human-like**.





LITERATURE REVIEW



- ❖ Literature review focuses on the available developments in [neuromorphic computing and spiking neural](#)
- ❖ Existing spiking neural network designs can be [difficult to use](#) for [non-experts](#).
- ❖ While there are existing hardware designs and accelerators for SNNs, there is a gap in the literature regarding the development of configurable neuromorphic processor architectures based on [RISC-V](#).
- ❖ Research addresses this gap by developing a configurable neuromorphic processor architecture that uses RISC-V and is easy to use for programmers of [various skill levels](#).
- ❖ Research demonstrates the effectiveness of using [RISC-V](#) for developing configurable neuromorphic architectures and provides a platform accessible to a [wider range of users and researchers](#).

AIM

- ❖ The aim of our research is to develop a **configurable neuromorphic** processor architecture for **spiking neural networks** that uses the **RISC-V** instruction set architecture, and to demonstrate that architecture is both **high-performing and low-power**, making it an attractive solution for a range of applications.





OBJECTIVES



- ❖ To design and implement a **configurable neuromorphic processor** architecture for spiking neural networks.
- ❖ To implement a **RV32IM pipelined** CPU in **Verilog** as a starting point for the design.
- ❖ To complete the current RISC-v **NOC (Network on Chip)** FPGA implementation for SNNs and integrate it into the processor architecture.
- ❖ To create a test SNN application to verify the functionality and performance of the processor architecture.
- ❖ To evaluate the **power consumption and speed** of the configurable neuromorphic processor architecture and compare it with existing solutions in the literature



LEARNING OUTCOMES

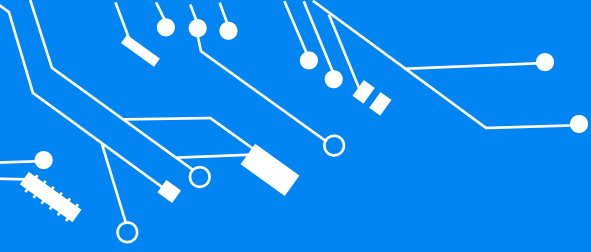


- ❖ To gain a deep understanding of the **principles and concepts** of spiking neural networks and neuromorphic computing.
- ❖ To become familiar with the **RISC-V instruction** set architecture and its implementation in hardware.
- ❖ To gain experience in developing and testing **SNN applications**.
- ❖ To understand the trade-offs between **power consumption, performance, and area** in processor architecture design.

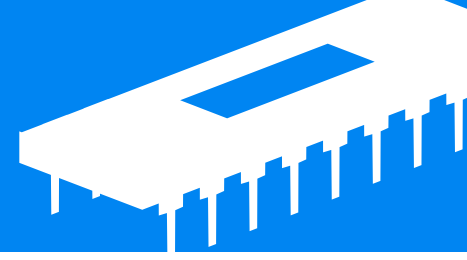
METHODOLOGY

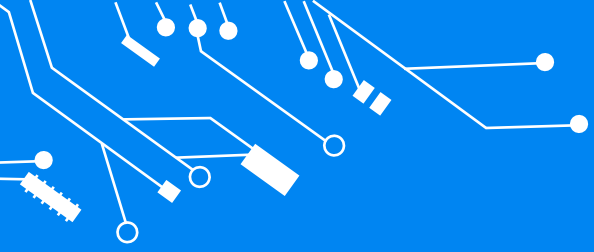
- ❖ Our research methodology consists of two main stages:
 - Implementing a RV32IM pipelined CPU in Verilog as a starting point for the design.
 - Completing the current RISC-v NoC (Network on Chip) FPGA implementation for spiking neural networks (SNNs) and integrating it into the processor architecture
- ❖ For the first stage, we will use Verilog as the hardware description language to implement the RV32IM pipelined CPU. This will serve as a foundation for the design and will allow us to build upon existing RISC-v architecture.
- ❖ For the second stage, we will use FPGA to implement the NoC for SNNs and integrate it into the processor architecture. This will enable us to develop a configurable neuromorphic processor architecture for spiking neural networks.



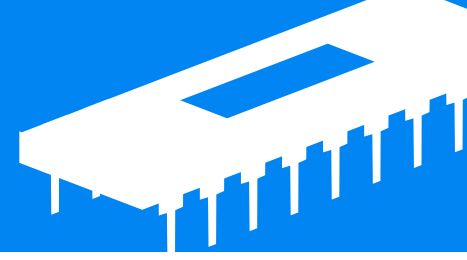


TIMELINE





REFFRENCES





THANK YOU

