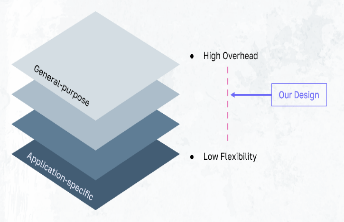
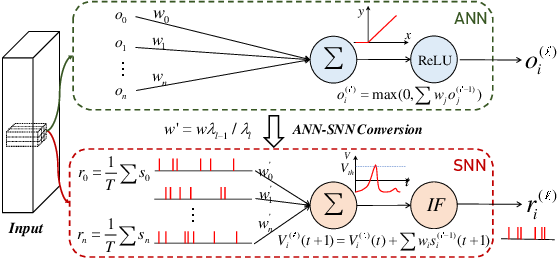
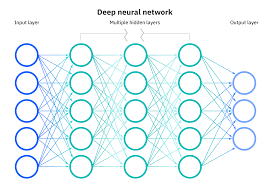
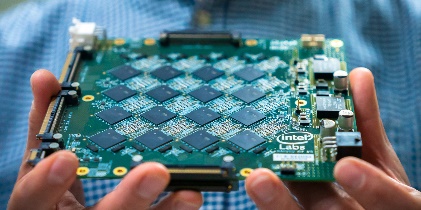
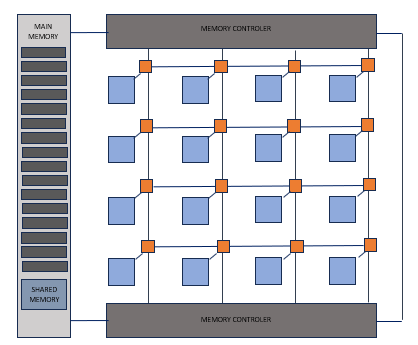
ME420 -MECHANICAL ENGINEERING RESEARCH PROJECT -PROGRESS EVALUATION 2023

**CONFIGURABLE NEUROMORPHIC PROCESSOR ARCHITECTURE FOR SPIKING NEURAL NETWORKS**



**INTRODUCTION**

In our quest to harness the extraordinary potential of Spiking Neural Networks (SNNs) for artificial intelligence applications, this research project introduces a Configurable Neuromorphic Processor architecture. Tailored for SNNs, our design prioritizes flexibility, configurability, and power efficiency, providing a dynamic framework for adapting hardware to diverse neural network models. Utilizing a Network on Chip (NoC) driven by RISC-V cores, our approach optimizes communication and data flow, enhancing both performance and energy efficiency.

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Approach to computing that uses hardware and software inspired by the principles of the human brain

* Energy efficiency
* Fast Processing
* Robustness
* Efficient use of memory

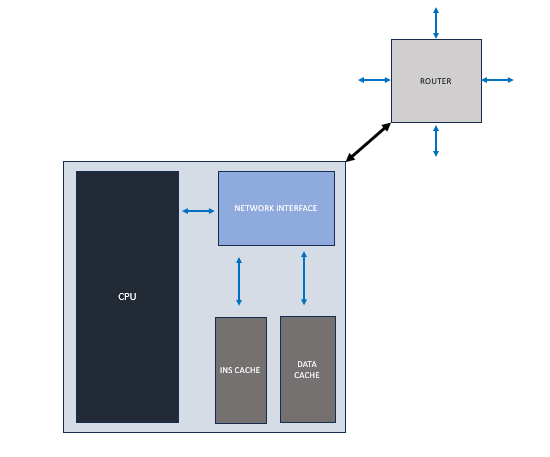
**OUR APPROACH**

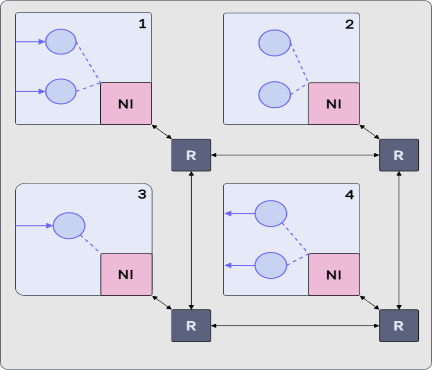
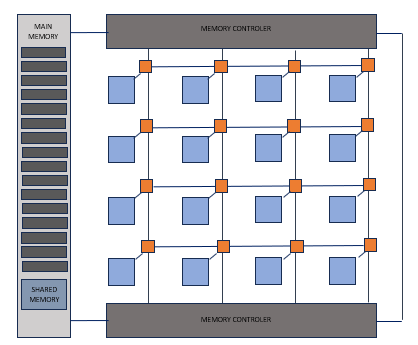
**NEUROMORPHIC COMPUTING**

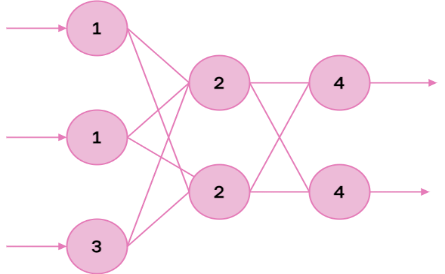
* Network on chip Architecture
* RISC V Pipelined Corers
* Energy efficiency
* Fast Processing
* Robustness
* Efficient use of memory
* Configurable and Flexible
* Easy to uses

**METHODOLOGY**

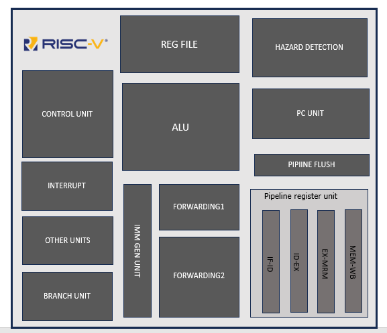
**PROGRASS SO FAR**



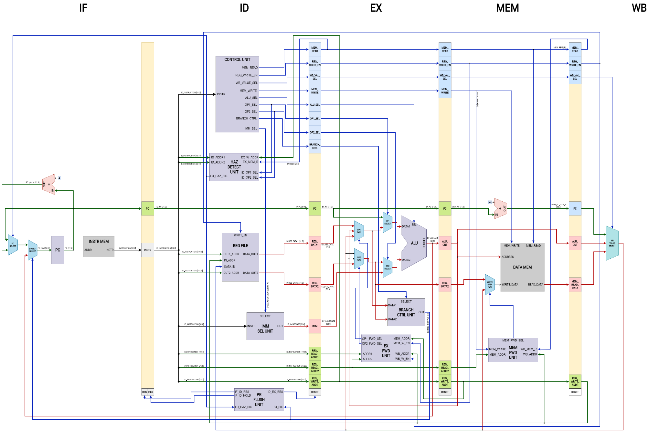
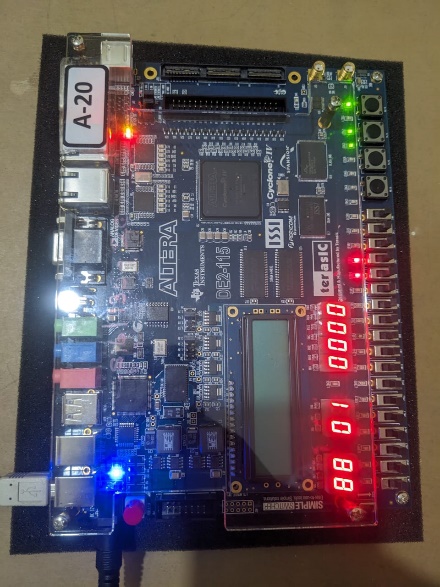
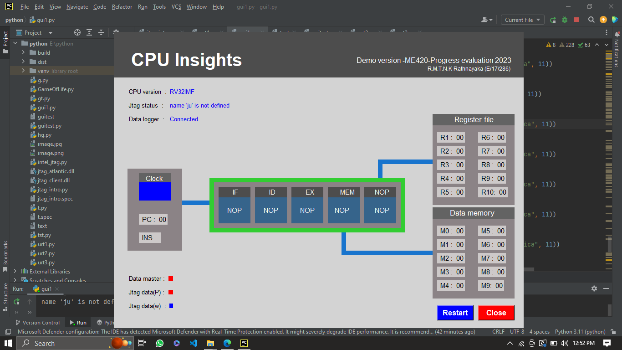




* Each node consist with Processing element, Router Network interface and local memory
* At first stage RISC V CPU was implemented
* And Started implementing the NoC



* Multiple numbers of neurons are assigned to each RISCV processing core within the neural network. These neurons function in an event-driven manner, mirroring the processes found in the human brain.
* In the neural network, these neurons work collectively to process information efficiently,



R.M.T.N.K Rathnayaka

E/17/286

Supervised by

Dr Isuru Nawinne and J.C Rajaguru

**IMPLMENTATION**

I implemented the RISC-V datapath and all associated components using Verilog HDL. I verified the functionality through rigorous testing with test benches and subsequently deployed the design onto an FPGA for hardware execution. Additionally, I created a desktop application to effectively demonstrate the CPU and the Network-on-Chip (NoC) in action.