Assignment 1

Design a circuit with two selection lines s1 and s0 to perform the following operations as shown in table with the inputs and outputs are A, B, C and Y respectively. The selection lines s1 and s0 are single bit lines and whereas the inputs are 64 bit format. Determine the size of the output Y. Design the circuit in generic form i.e., use the parameter keyword to declare the inputs and outputs.

Hint: parameter N=8,M=8;
The operations are as follows;

Selection lines	Operation (Y)
s1 s0	
0 0	A+B
0 1	A-B
1 0	A*B
1 1	C+A*B

Implement the circuit by using Verilog HDL and verify the functionality by writing its self checking testbench.