ECEN 5613 | **Embedded System Design** | **Fall 2023**

Lab #2 Signoff Sheet

You will need to obtain the signature of your instructor or TA on the following items in order to receive credit for your lab assignment. Signatures are due by **Friday, September 29, 2023 (Part 1 Elements) and Friday, October 6, 2023 (Part 2 Elements)**.

Print your name below, sign the honor code pledge, and then demonstrate your working hardware & firmware in order to obtain the necessary signatures.

Student Name: Tharuni Galli

Honor Code Pledge: "On my honor, as a University of Colorado student, I have neither given nor received unauthorized assistance on this work. I have clearly acknowledged work that is not my own."

Student Signature: Tharuni

Signoff Checklist

Part 1 Required Elements

- ☑ Schematic of acceptable quality, correct memory map, SPLD .PLD file
- ☑ Pins and signals labeled, decoupling capacitors, and two 28-pin wire wrap sockets present on board
- ☑ NVRAM (as EPROM substitute), decode logic, and LED functional
- ☑ Understands device programmer.
- ☑ Demonstrated ability to use logic analyzer to capture bus cycles and view fetches from NVRAM. Shows detailed knowledge of both state and timing modes. Captures latched address lines A[15:0], data lines D[7:0], ALE, /PSEN, and NVRAM chip select signal on the logic analyzer display.
- ☑ Shows and discusses logic analyzer screen captures:
- ☑ Assembly program and timer ISR functional:

09/29/2023

TA signature and date

Part 2 Required and Supplemental Elements

- ☑ AT89C51RC2, RS-232, and FLIP functional
- ☐ 74LS374 debug port functional
- ☑ Understands timing analysis, setup/hold/propagation
- ☑ ARM code build process, LED program, version control

Instructor/TA Comments: ☐ ☐ ☐

Keshpande 10/05/23

TA signature and date

FOR INSTRUCTOR USE ONLY **Part 1 Elements**	Not Applicable	Poor/Not Complete	Meets Requirements	Exceeds Requirements	Outstanding
Schematics, SPLD code	☐	☐	☐	☑	☐
Hardware physical implementation	☐	☐	☐	☑	☐
Part 1 Required Elements functionality	☐	☐	☑	☐	☐
Sign-off done without excessive retries		☐	☑		
Student understanding and skills	☐	☐	☑	☐	☐
Overall Demo Quality (Part 1 Elements)	☐	☐	☐	☑	☐

FOR INSTRUCTOR USE ONLY **Part 2 Elements**	Not Applicable	Poor/Not Complete	Meets Requirements	Exceeds Requirements	Outstanding
Schematics, SPLD code	☐	☐	☐	☑	☐
Hardware physical implementation	☐	☐	☐	☑	☐
Part 2 Required Elements functionality	☐	☐	☐	☑	☐
Supplemental Elements functionality	☐	☐	☐	☐	☐
Sign-off done without excessive retries		☐	☑		
Student understanding and skills	☐	☐	☐	☐	☐
Overall Demo Quality (Part 2 Elements)	☐	☐	☐	☐	☐

NOTE: This signoff sheet should be the top/first sheet of your submission.

[+] Schematic is clean and correct.
  [+] NSRAM dec cap is missing.
[+] Logic Analyzer probes connected well. Good use of timing mode.
  [-] State mode not prepared.
[+] LED frequency is within that range (≈1.70Hz) but simulation seems fine.
[+] Hardware assembly is good.

(+) Good Schematic.
(+) Flip functional.
(+) ARM code functional

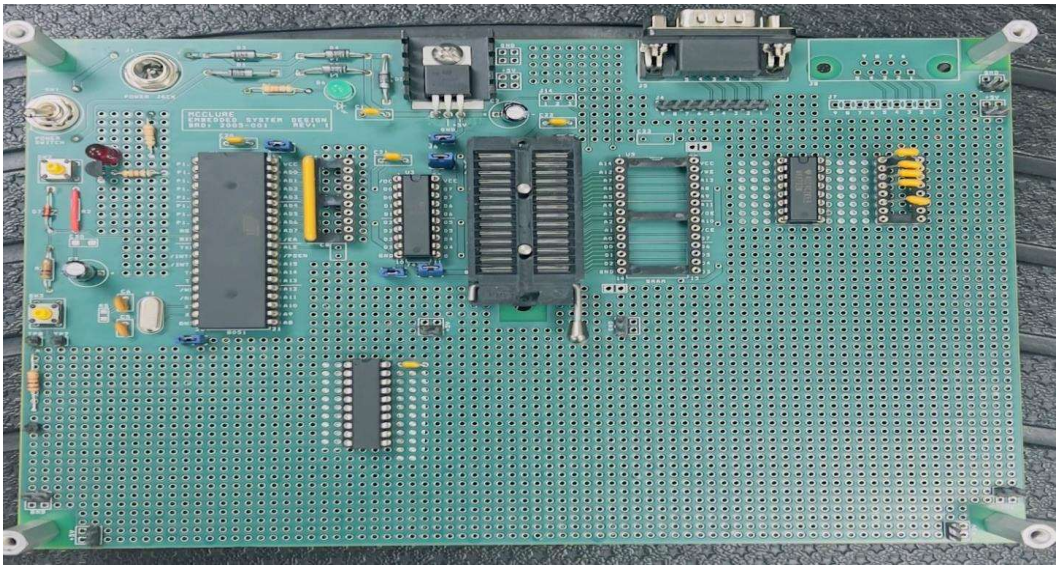
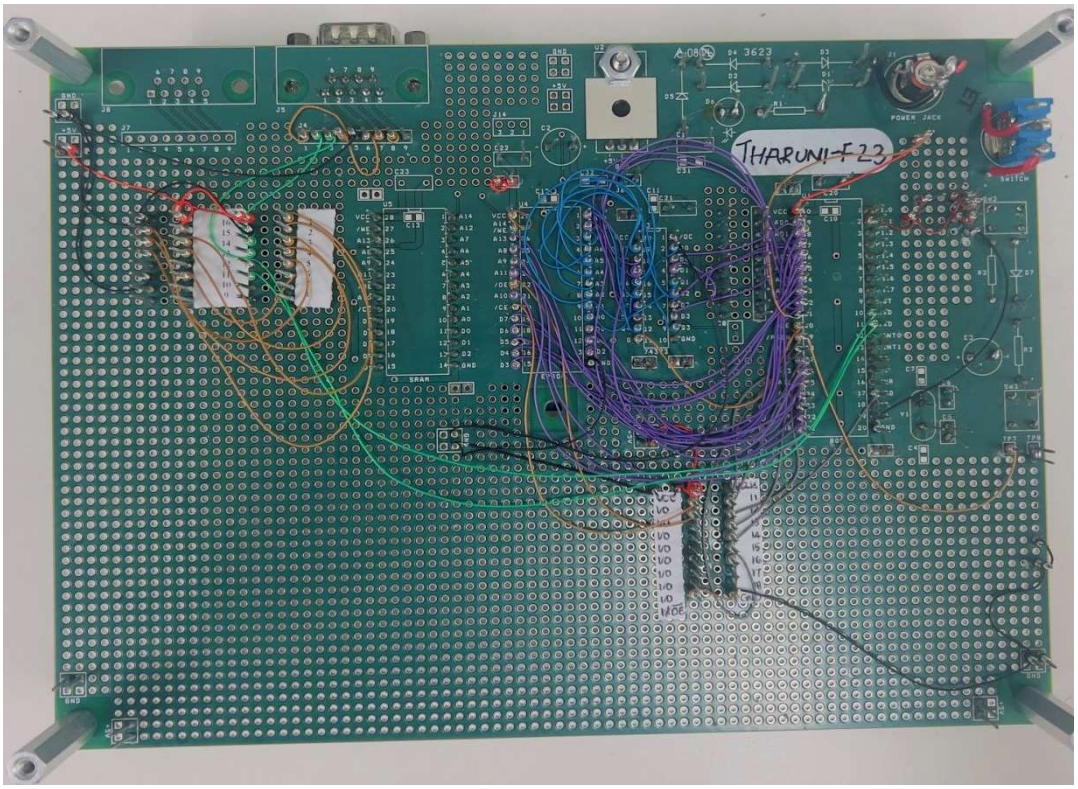


Fig: 8051 Board build up front image Fig: 8051 Board build up front image and back image



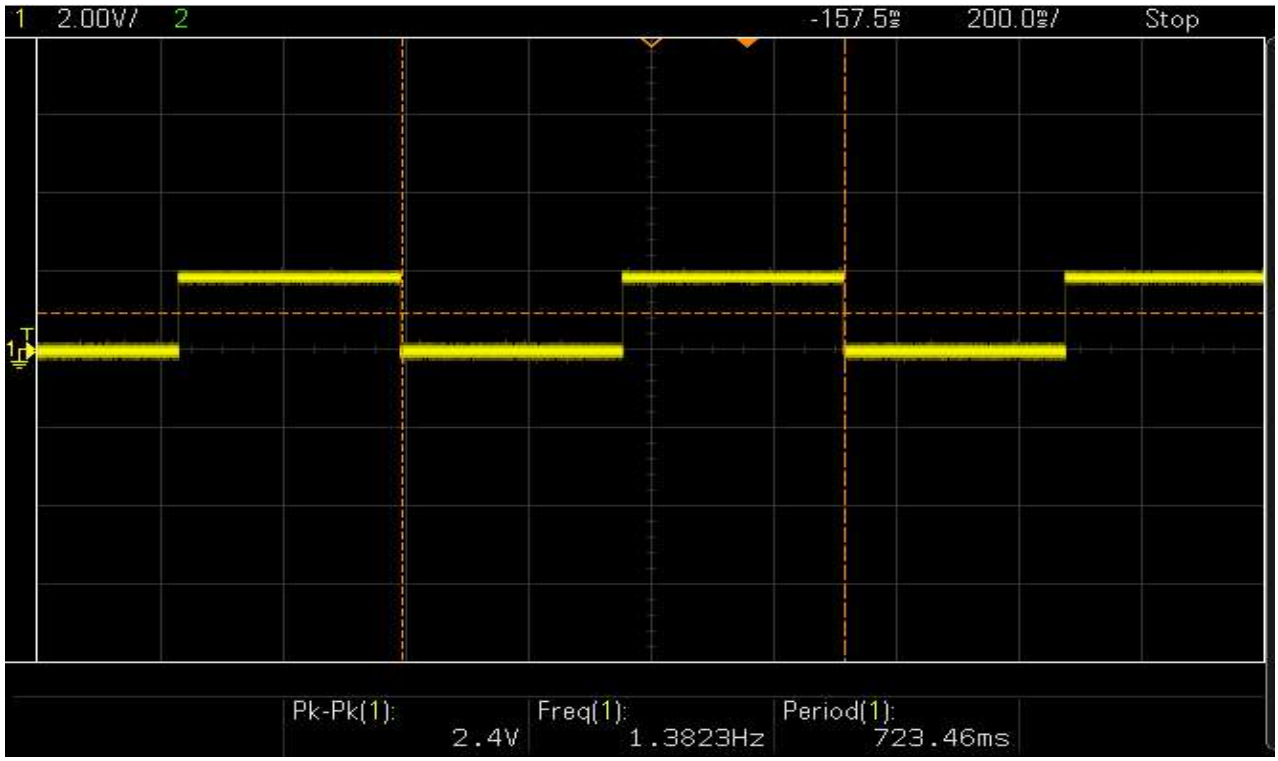


Fig: Toggling a LED which is connected to one unused pin of port 0 (p0.1) at 1.38hz frequency (0.362msec ON and 0.362msec OFF) – LAB2PART1

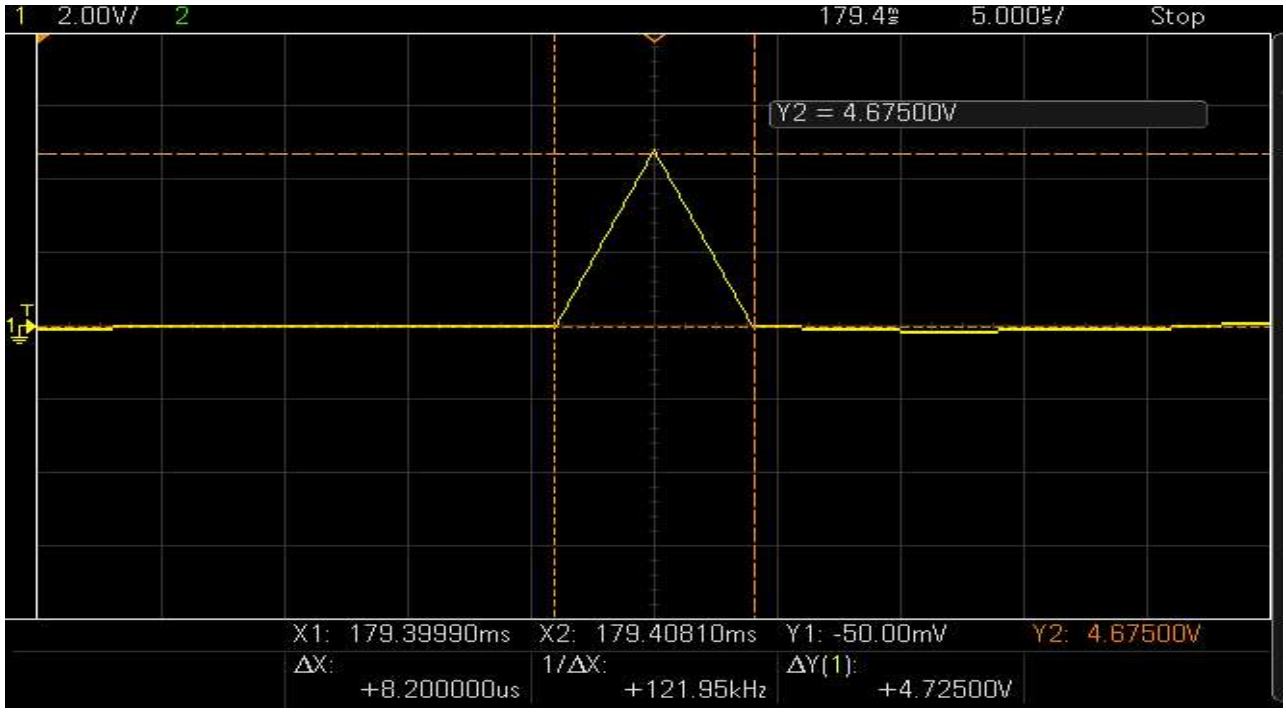


Fig: Toggling a unused port pin (p0.0) whenever ISR is executed (duration of this pin is equal to time taken for ISR to execute T_{Ilpl} is 8.2µsecs which is verified at calculation section– LAB2PART1

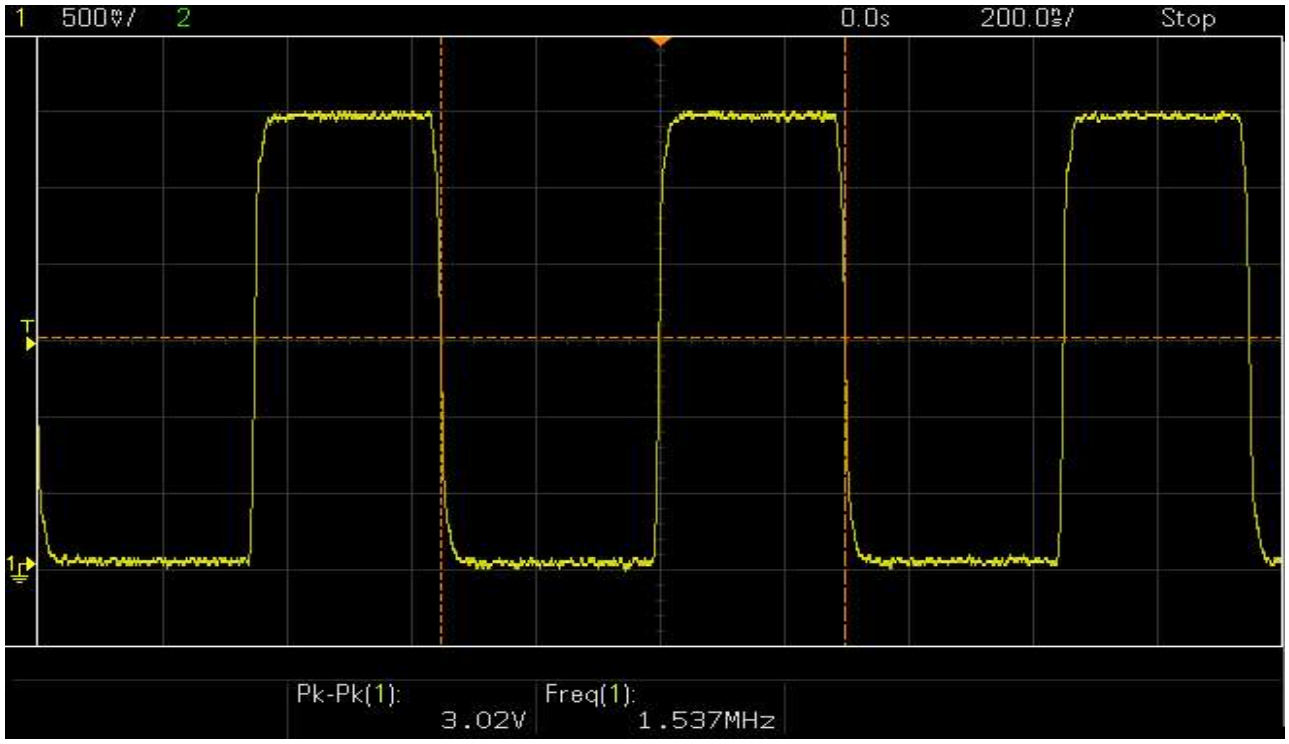


Fig: Toggling a onboard LED of STM32 – LAB2PART1 (demo program to get used for bare metal programming)

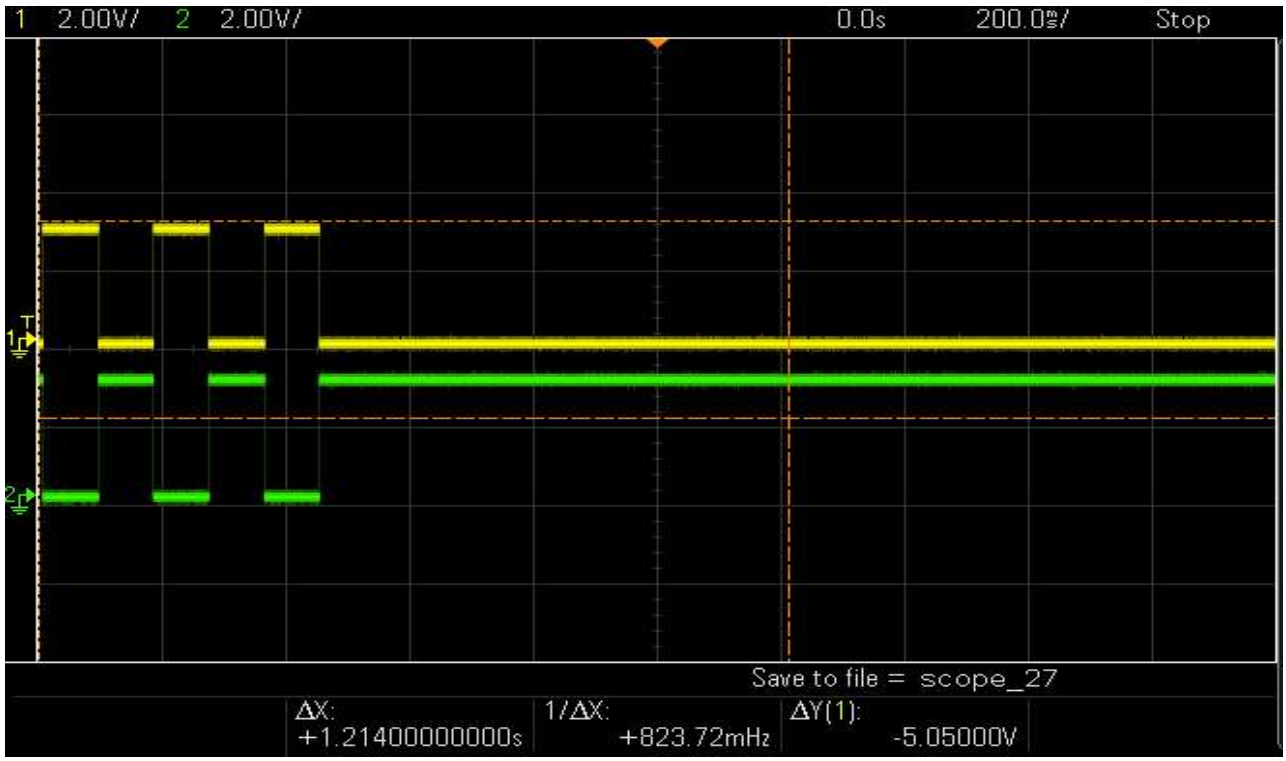


Fig: Toggling two onboard leds of STM32 with push button as external interrupt

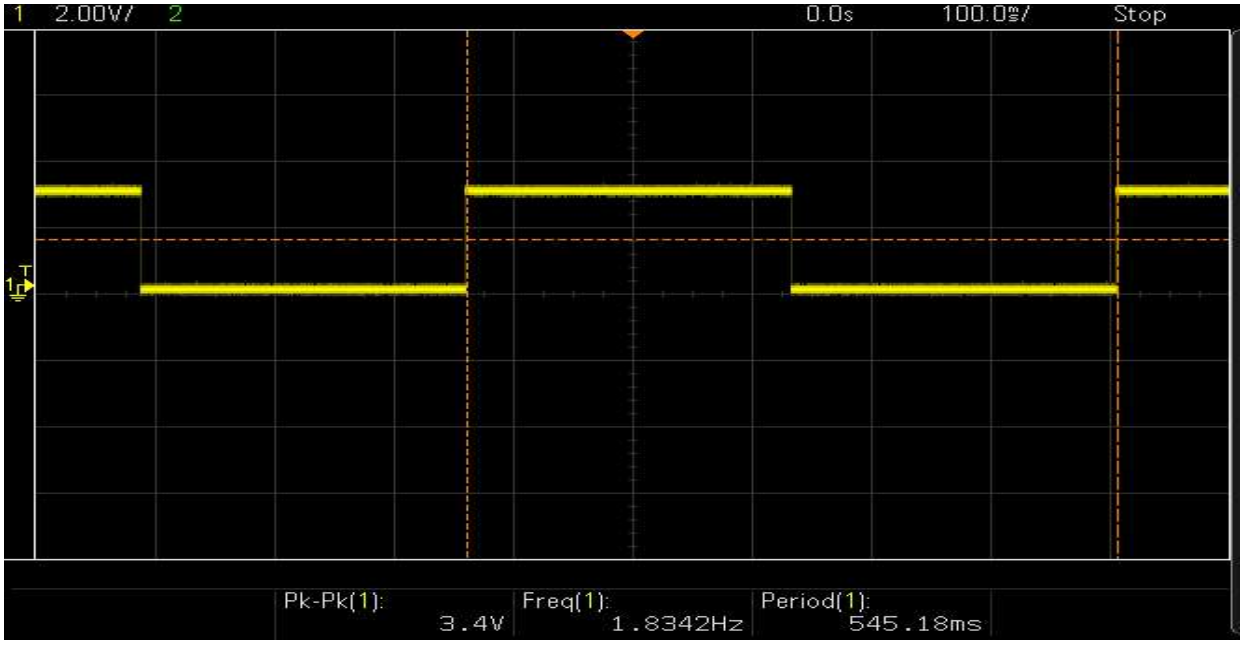


Fig: Toggling onboard led of STM32 with delay of 270ms of on and off time each using timer interrupt

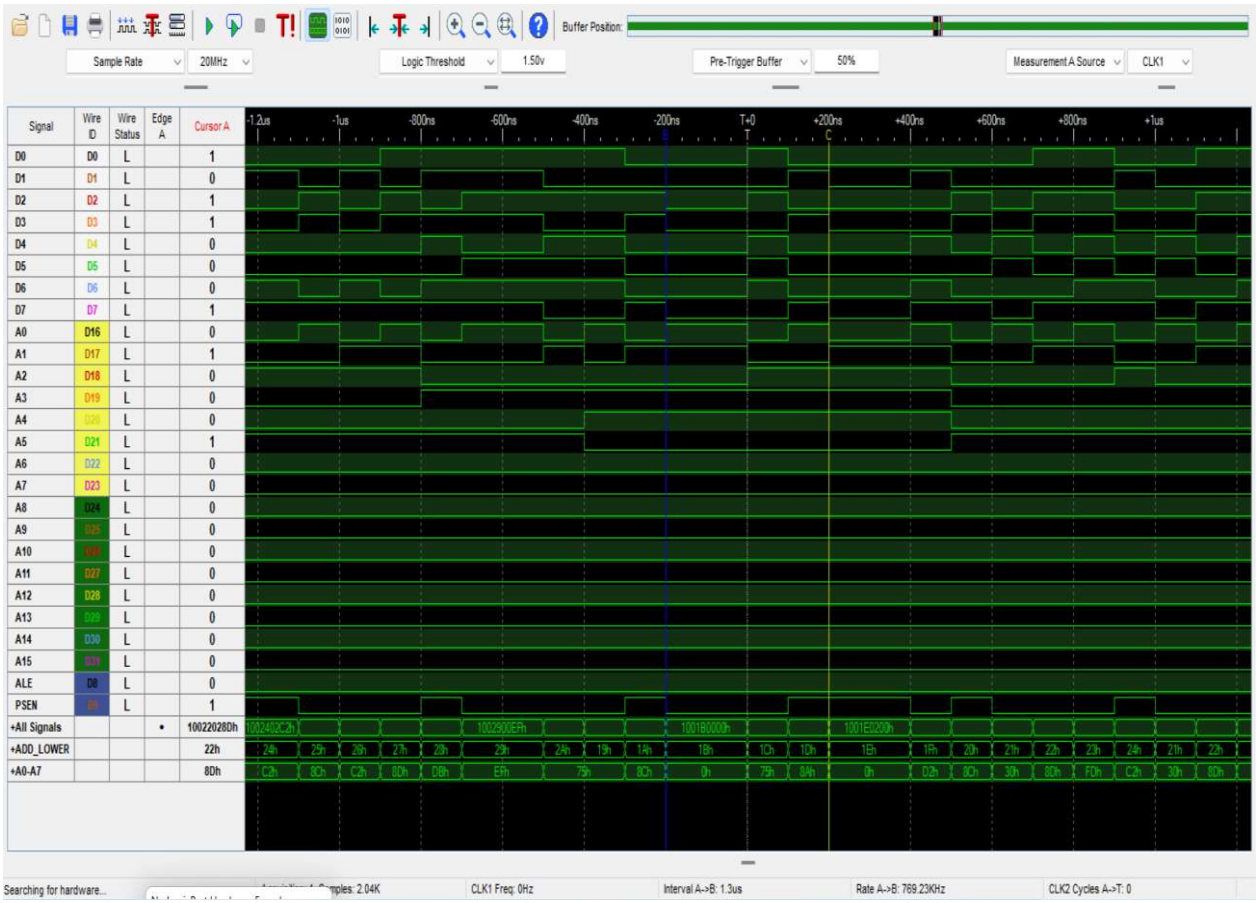
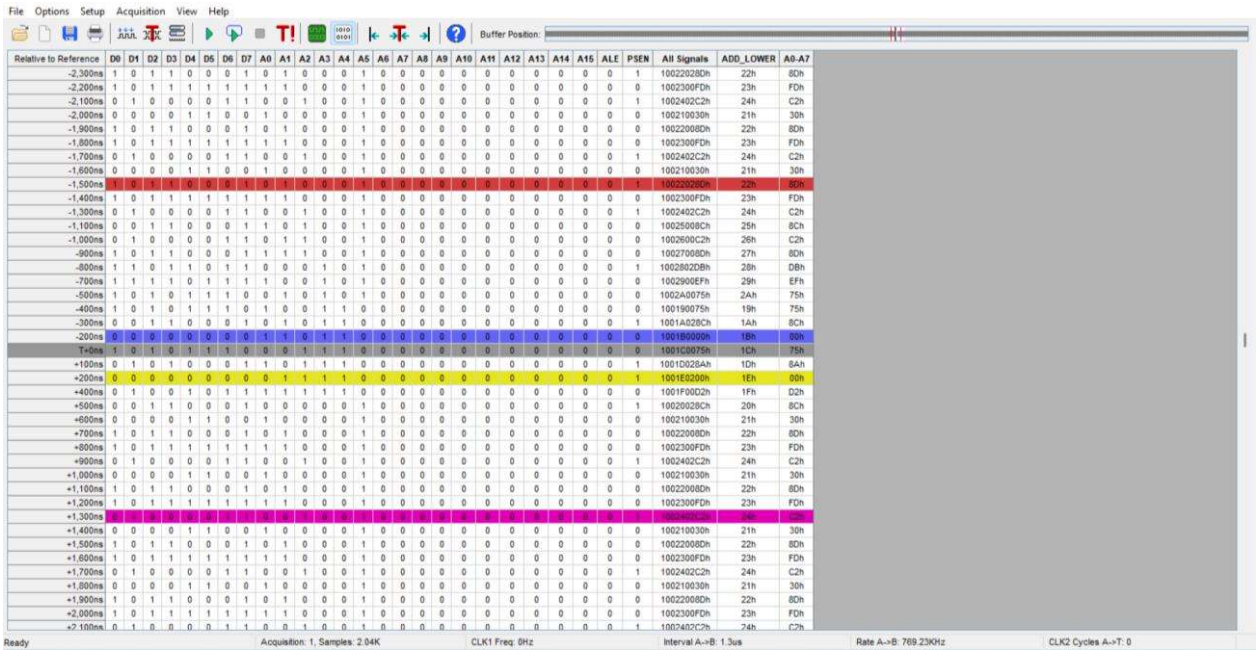


Fig: Logic analyzer output for verifying hex file with timing and state modes



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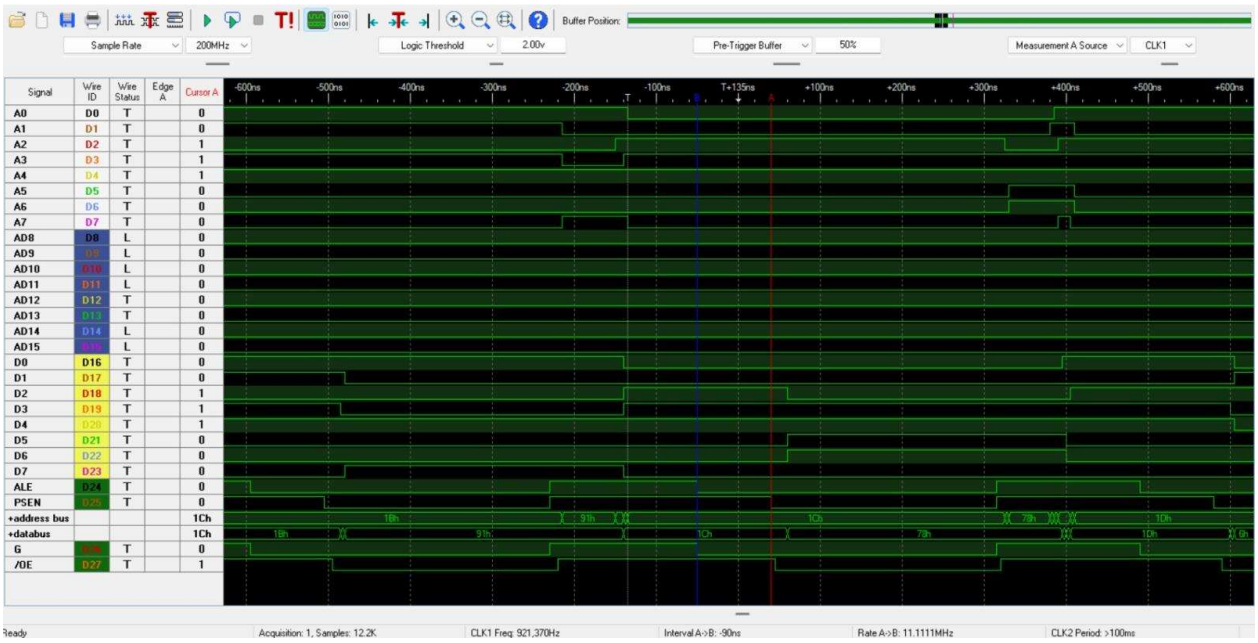

Fig: Toggling time difference of ALE and PSEN.

CALCULATIONS:

Here the time difference between ALE & PSEN falling edges gives the $t_{llpl:}$ value is measured by using the A and B marker. The time difference between them is 90nsecs. As per datasheet the minimum value is 58 nsecs for the clock frequency of 11.0592Mhz. Hence its verified with datasheet as 90nsecs is allowable value.

Lab 2 Submission questions:

1) What operating system (including revision) did you use for your 8051 code development?

Ans: Windows 11 operating system is used.

2) What assembler(s) (including revision) did you use?

Ans: Keil µvision (AX51) is used.

3) What ARM development tools did you use?

Ans: STM32 Cube IDE development tool is used for ARM development.

4) Did you install and use any other software tools to complete your lab assignment?

Ans: No

5) Did you experience any problems or challenges with this lab assignment or any of the software tools? If so, describe the issues.

Ans: I faced one particular issue with logic analyzer where its state mode of operation was asked in lab2part1 signoff itself which was conducted ahead of its demo session. So in that sign off I couldn't answer about the state mode (I have searched in online resources as well, but didn't find any info regarding it, so the reason for not answering about it) which gave me a minus remark in lab2part1 signoff. So my opinion is, if we are dealing with any new equipment or software related to lab, expecting its demo sessions ahead of the signoffs so that it will be easy to analyze and explain to TA's during signoff.

6) If you have any suggestions for changes to this lab assignment for the future, please include those ideas in your submission.

Ans: No

MAJOR LEARNINGS:

Things learned in this lab 2 consist of:

1) One of my major learning would be bare metal programming of ARM.

2) Calculating precise delays and generating interrupts in order to gain that delay.

3) Logic analyzer tool usage.

4) FLIP programmer for programming ATMEL chip.

Calculations: Verifying time taken by ISR with the port pin of 8051 toggling period.

Time taken for unused pin of 8051 – P1.0 is = 8.2 usecs.

ISR: CLR – 1 clk cycle Ljmp – 2 clk cycle.
Setb – 1 clk cycle
Cpl – 1 clk cycle
SJmp – 2 clk cycle

Total no. of clk cycles all = 7.

time for each clock cycle is 1.085 usecs.

therefore, 7 x 1.085 usecs = 7.895 ≈ 8.00 usecs.

Hence, the toggling period matches with ISR.

Delay calculation for LED blink (0.362secs ON - 0.362secs OFF)

Frequency of 8051 controller = 11.0592 MHz.

each machine cycle has 12 clock cycles.

clock cycle freq = 11.0592 MHz / 12 = 0.9216 MHz.

Time period = 1/clk. freq = 1/0.9216 MHz = 1.085 micro secs.

for delay of 0.362 secs,

$$\text{count}(N) = \frac{0.362}{1.085} \times 10^6 = 333640.$$

FFFFH → Max value that times can hold.

= 65536 = To hit count of 333640 -

we need to run loop of this for '5' times

and remaining count can be of 5963

which can be loaded as E8 B9 H

Hence TH = E8H TL = B9H

Delay calculation for on boaed LED of Stm32!

Delay of 270mses = frequency = 3.7 Hz.

Formula,

$$\text{Req. freq} = \frac{\text{TIM clk}}{(\text{PSC}+1) * (\text{ARR}+1)}$$

→ which is 48 MHz.

$$(\text{PSC}+1)(\text{ARR}+1) = \frac{48 \times 10^6 \text{ Hz}}{3.7 \text{ Hz}} = \cancel{16 \times 10^6 \text{ Hz}} = 12972972.9 \text{ Hz}.$$

Max value that a prescalar can hold is = ffffH

$$(\text{ARR}+1) = \frac{12972972}{\cancel{16000000}\ 65536} = \cancel{244.14.}\ 197.$$

which is = C8H → can be used as auto reloader.

Hence, Timer 2 prescaler and auto reloader values for interrupt generation are:-

TIM2 → PSC = ffffH

TIM2 → ARR = C8H.