IDS - Homework 5

Athazahra Nabila Ruby - KK1 - 2306173113

1. out of the 3 methods, 2's complement has the largest range.

   a) 2's complement
   - for an n-bit representation, it can represent values from -2^{n-1} to $2^{n-1}-1$.
   - it has one more negative number compared to 1's complement and signed magnitude because it doesn't have a seperate representation for positive zero and negative zero

   b) 1's complement
   - for an n-bit representation it can represent values from $-(2^{n-1}-1)$ to $2^{n-1}-1$.
   - it has 2 represention for zero: all-one bit pattern and all-zero bit pattern. This redundancy limits the range and causes issues with zero representation

   c) Signed magnitude
   - for an n-bit representation it can represent values from $-(2^{n-1}-1)$ to $2^{n-1}-1$.
   - it suffers the same issues as 1's complement, with 2 representations for zero.

2. a. $-(3113)_{10} \xrightarrow{\text{binary}} -(2048+1024+32+8+1) = -(0000110000101001)_2$

   1's complement ↓ invert all bits

   $= (1111001111010110)_{1\text{'s comp}}$

   2's complement ↓ add 1

   $= (1111001111010111)_{2\text{'s}}$

   b. $-(1C9B)_{16} \xrightarrow{\text{binary}} -(\underbrace{0100}_{4}\ \underbrace{1100}_{C}\ \underbrace{1001}_{9}\ \underbrace{1011}_{B})_2 \xrightarrow[\text{because (-), sign = 1}]{\text{signed magnitude}} (1100\ 1100\ 1001\ 1011)_{sm}$

   c. $-(505)_7 \xrightarrow{\text{decimal}} -(5.\underbrace{7^2}_{49} + 0.\underbrace{7^1}_{7} + 5.\underbrace{7^0}_{1}) = (-250)_{10} \xrightarrow{\text{binary}} -(128+64+32+16+8+2)$

   $= -(1111\ 1010)_2$

   1's comp ↓

   needs 16 bits so that -250 is within the range

   $= (1111\ 1111\ 0000\ 0101)_{1\text{'s}}$

Athazahra Nabila Ruby - KK1 - 2306173113

3. a. $-(7783)_9 \xrightarrow{\text{decimal}} -(7.9^3 + 7.9^2 + 8.9^1 + 3.9^0) = -(5745)_{10} \xrightarrow{\text{binary}} -(4096 + 1024 + 512 + 64 + 32 + 16 + 1)$

$= -(0001\ 0110\ 0111\ 0001)_2$

1's comp ↓

$= (1110\ 1001\ 1000\ 1110)_{1's}$

2's comp ↓

$= (1110\ 1001\ 1000\ 1111)_{2's}$

2's comp of a positive number is the same

$(11011\ 0010)_2 - (7783)_9 = (0000\ 0001\ 1011\ 0010)_{2's} + (1110\ 1001\ 1000\ 1111)_{2's}$

$$\begin{array}{r} 0000\ 0001\ 1011\ 0010 \\ 1110\ 1001\ 1000\ 1111 \\ \hline (1\ 1101\ 0011\ 0100\ 0001)_{2S} \end{array} +$$

1's (subtract 1) → $(1110\ 1011\ 0100\ 0000)_{1's}$

b. $(ADD)_{16} \xrightarrow{\text{binary}} (1010\ \ 1101\ \ 1101)_2 \xrightarrow{\text{2's comp}} (0000\ 1010\ 1101\ 1101)_{2's}$

$-(12104)_7 \xrightarrow{\text{decimal}} -(1.7^4 + 2.7^3 + 1.7^2 + 0.7^1 + 4.7^0) = -(3140)_{10} \xrightarrow{\text{binary}} -(2048 + 1024 + 64 + 4)$

$= -(0000\ 1100\ 0100\ 0100)_2$

1's comp ↓

$= (1111\ 0011\ 1011\ 1011)_{1's}$

2's comp ↓ $\quad 1 + 100$

$= (1111\ 0011\ 1011\ 1100)_{2's}$

$(ADD)_{16} - (12104)_7 = (0000\ 1010\ 1101\ 1101)_{2's} + (1111\ 0011\ 1011\ 1100)_{2's}$

$$\begin{array}{r} 0000\ 1010\ 1101\ 1101 \\ 1111\ 0011\ 1011\ 1100 \\ \hline (1111\ 1110\ 1001\ 1001)_{2's} \end{array} +$$

c. $(10)_6 \xrightarrow{\text{decimal}} (1.6^1 + 0.6^0) = (24)_{10} \xrightarrow{\text{binary}} (16 + 8) = (11000)_2 \xrightarrow{\text{2's comp}} (0001\ 1000)_{2's}$

$-(19)_{16} \xrightarrow{\text{binary}} -(0001\ \ 1001)_2 \xrightarrow{\text{1's comp}} (1110\ 0110)_{1S} \xrightarrow{\text{2's comp}} (1110\ 0111)_{2's}$

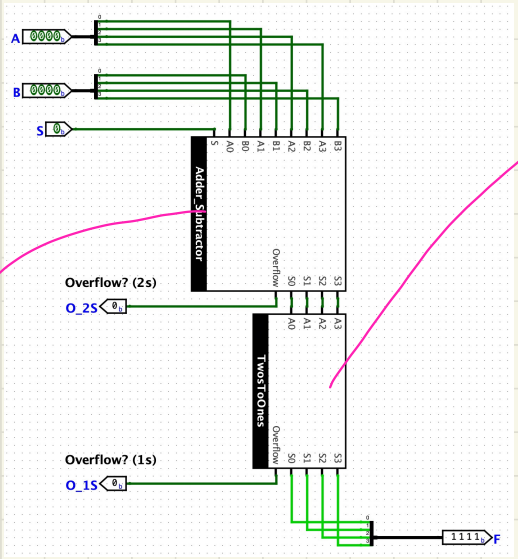
$(10)_6 - (19)_{16} = (0001\ 1000)_{2's} + (1110\ 0111)_{2's}$

$$\begin{array}{r} 0001\ 1000 \\ 1110\ 0111 \\ \hline (1111\ 1111)_{2S} \end{array} +$$

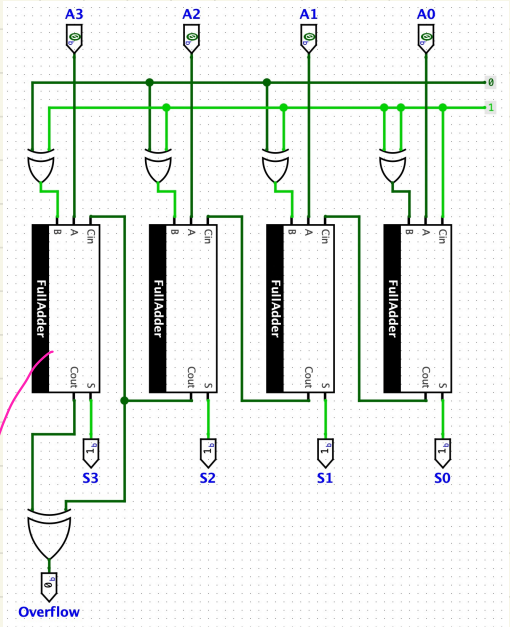
1's comp → $(1111\ 1110)_{1's}$ → binary → $-(0000\ 0001)_2$ → signed magnitude (sign bit = 1 bc (−)) → $(11)_{SM}$

1. Main Circuit

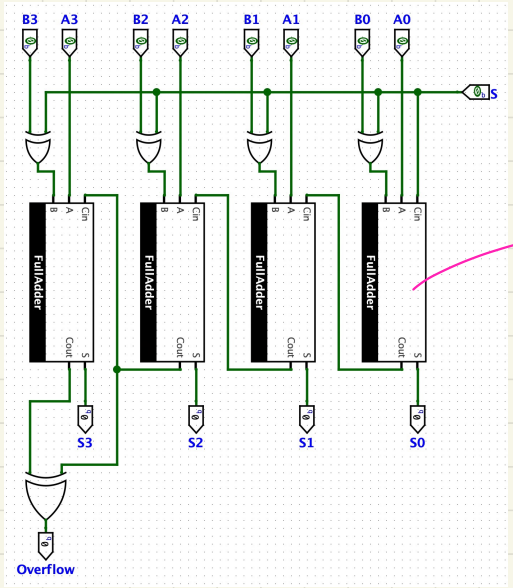
Athazahra Nabila Ruby - KK1 - 2306173113



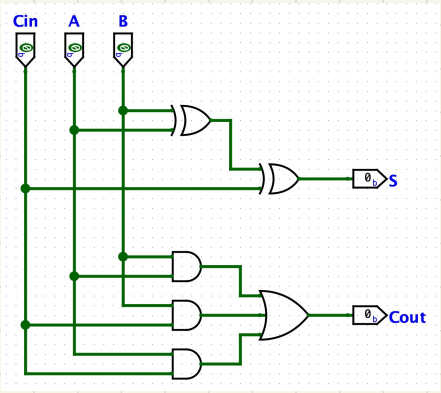
1-bit 2's complement to 1's complement converter



1-bit Adder-Com Subtractor



Full adder



Athazahra Nabila Ruby - KK1 - 2306173113

5. a. Synchronous Sequential Circuit = digital circuit that use clock signals to synchronize changes in the state of the circuit at discrete points in time

Asynchronous Sequential Circuit = digital circuits that can change state at any time in response to change in inputs (does not use clock signals).

Differences :

Synchronous	Asynchronous
•) uses clock signals	•) does not use clock
•) state changes to next state when clock is active	•) state changes to next state when it receives input (instant)
•) speed of circuit depends on the clock delay	•) speed of circuit depends on the received input

b. A sequential circuit that only uses latches is Asynchronous, because latches can change their state as soon as their input changes (because latches are level-sensitive), without being synchronized to a clock signal.

Athazahra Nabila Ruby - KK1 - 2306173113

6. $D(t) = \overline{A(t)} \cdot B(t)$

$S(t+1) = (Q_D(t) \cdot A(t)) \oplus \overline{(Q_D(t) + \overline{B(t)})} = (Q_D(t) \cdot A(t)) \oplus (\overline{Q_D(t)} \cdot B(t))$

$R(t+1) = \overline{S(t+1)}$

$Y = \overline{Q_D(t)} + Q_{SR}(t)$

$Z = Q_D(t) \cdot \overline{Q_{SR}(t)}$