

Homework 6

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1. a) one-dimensional

Present State	Input	next state		output
		A(t)	B(t)	
0 0	0	1	0	0
0 0	1	0	0	1
0 1	0	1	1	1
0 1	1	0	0	0
1 0	0	0	0	1
1 0	1	0	0	0
1 1	0	1	0	0
1 1	1	1	0	1

b) two-dimensional

Present State	next state		output	
	X(t)=0	X(t)=1	X(t)=0	X(t)=1
A(t) B(t)	A(t+1) B(t+1)	A(t+1) B(t+1)	Y(t)	Y(t)
0 0	1 0	0 0	0	1
0 1	1 1	0 0	1	0
1 0	0 0	0 0	1	0
1 1	1 0	1 0	0	1

2. a. D Flip-flop

Clock	D	Q(t)	Q(t+1)	Characteristic	
↑	0	0	0	D=0	reset
↑	0	1	0		
↑	1	0	1	D=1	set
↑	1	1	1		

b. SR Flip-flop

Clock	S	R	Q(t)	Q(t+1)	Characteristic	
↑	0	0	0	0	S=0, R=0	no change
↑	0	0	1	1		
↑	0	1	0	0	S=0, R=1	reset
↑	0	1	1	0		
↑	1	0	0	1	S=1, R=0	Set
↑	1	0	1	1		

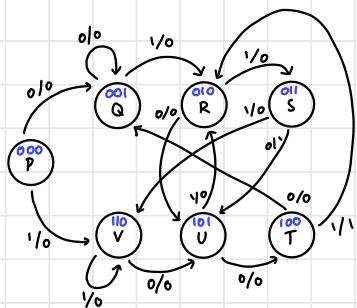
c. T Flip-flop

Clock	T	Q(t)	Q(t+1)	Characteristic	
↑	0	0	0	T=0	no Change
↑	0	1	1		no Change
↑	1	0	1	T=1	complement
↑	1	1	0		complement

d. JK Flip-flop

Clock	J	K	Q(t)	Q(t+1)	Characteristic	
↑	0	0	0	0	J=0, K=0	no Change
↑	0	0	1	1		
↑	0	1	0	0	J=0, K=1	reset
↑	0	1	1	0		
↑	1	0	0	1	J=1, K=0	Set
↑	1	0	1	1		
↑	1	1	0	1	J=1, K=1	complement
↑	1	1	1	0		

3. a.



$P = 000$

$Q = 001$

$R = 010$

$S = 011$

$T = 100$

$U = 101$

$V = 110$

b.

Present State			Next State						Output	
			x=0			x=1			x=0	x=1
A	B	C	A'	B'	C'	A'	B'	C'	Y	Y
0	0	0	0	0	1	1	1	0	0	0
0	0	1	0	0	1	0	1	0	0	0
0	1	0	1	0	1	0	1	1	0	0
0	1	1	1	0	1	1	1	0	1	0
1	0	0	0	0	1	0	1	0	0	1
1	0	1	1	0	0	0	1	0	0	0
1	1	0	1	0	1	1	1	0	0	0
1	1	1	X	X	X	X	X	X	X	X

c. 1) Specification:

- "0110" or "1001" sequence recognizer
- circuit outputs 1 when "0110" or "1001" is detected
- state uses 3-bit binary: A, B, C (A being the MSB)
- implementation: positive edge-triggered D flip-flop, AND gate, OR gate, NOT gate
- input: X
- output: Y

2) Formulation

- State diagram and state assignment is on 4.a
- State table is on 4.b

) Flip-Flop Input determination table

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Present State			Next State						Output	
			x=0			x=1			x=0	x=1
A	B	C	D2	D1	D0	D2	D1	D0	Y	Y
0	0	0	0	0	1	1	1	0	0	0
0	0	1	0	0	1	0	1	0	0	0
0	1	0	1	0	1	0	1	1	0	0
0	1	1	1	0	1	1	1	0	1	0
1	0	0	0	0	1	0	1	0	0	1
1	0	1	1	0	0	0	1	0	0	0
1	1	0	1	0	1	1	1	0	0	0
1	1	1	X	X	X	X	X	X	X	X

3) Optimization

			D ₂				
			CX	̄C	C		
			00	01	11	10	
Ā	00	00	0	1	1	2	̄B
	01	1	1	1	1	1	B
	11	1	1	1	X	X	̄B
	10	8	9	11	10	10	̄B
			̄X	X	̄X		

			D ₁				
			CX	̄C	C		
			00	01	11	10	
A	00	0	1	1	1	2	̄B
	01	1	1	1	1	1	B
	11	1	1	1	X	X	̄B
	10	8	9	11	10	10	̄B
			̄X	X	̄X		

$$\begin{aligned}
 D_2 &= AB + BC + B\bar{X} + AC\bar{X} + \bar{A}\bar{B}\bar{C}X \\
 &= B(A + C + \bar{X}) + AC\bar{X} + \bar{A}\bar{B}\bar{C}X
 \end{aligned}$$

			D ₀				
			CX	̄C	C		
			00	01	11	10	
Ā	00	00	1	1	1	2	̄B
	01	1	1	1	1	1	B
	11	1	1	1	X	X	̄B
	10	1	6	9	11	10	̄B
			̄X	X	̄X		

$$\begin{aligned}
 D_0 &= \bar{C}\bar{X} + \bar{A}\bar{X} + \bar{A}\bar{B}\bar{C} \\
 &= \bar{X}(\bar{A} + \bar{C}) + \bar{A}\bar{B}\bar{C}
 \end{aligned}$$

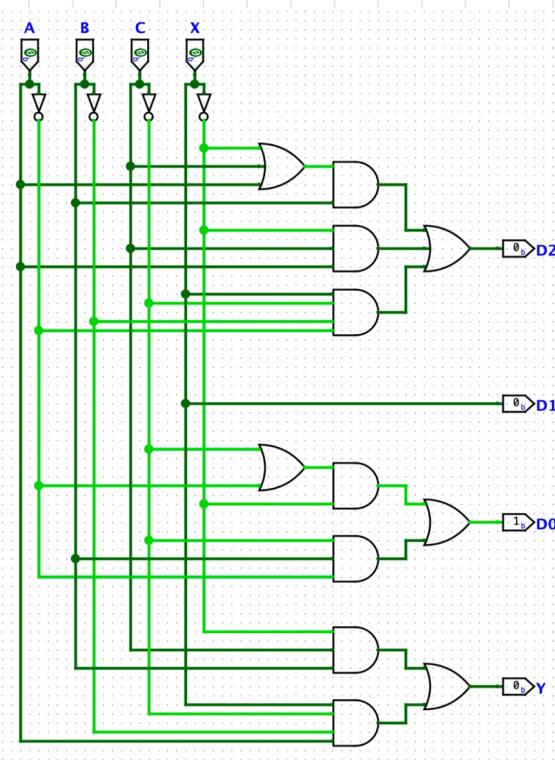
			Y				
			CX	̄C	C		
			00	01	11	10	
Ā	00	0	1	1	1	2	̄B
	01	4	5	7	6	6	B
	11	12	13	X	X	14	̄B
	10	8	9	11	10	10	̄B
			̄X	X	̄X		

$$Y = BC\bar{X} + A\bar{B}\bar{C}X$$

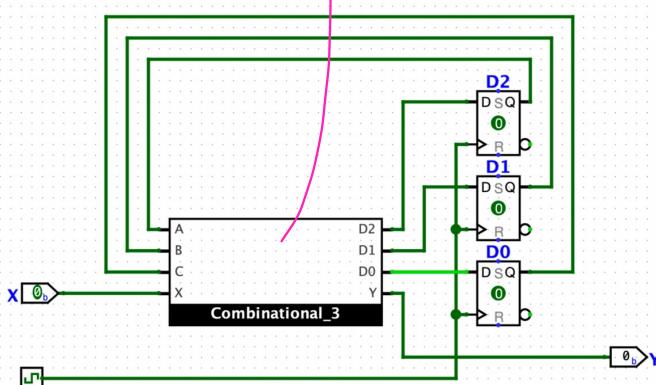
1) Technology Mapping

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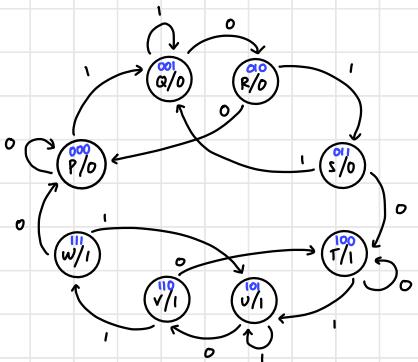
Combinational Circuit



Sequential Circuit



1. a.



$P = 000$

$Q = 001$

$R = 010$

$S = 011$

$T = 100$

$U = 101$

$V = 110$

$W = 111$

b.

Present State			Next State						Output
			x = 0			x = 1			
A	B	C	A'	B'	C'	A'	B'	C'	Y
0	0	0	0	0	0	0	0	1	0
0	0	1	0	1	0	0	0	1	0
0	1	0	0	0	0	0	1	1	0
0	1	1	1	0	0	0	0	1	0
1	0	0	1	0	0	1	0	1	1
1	0	1	1	1	0	1	0	1	1
1	1	0	1	0	0	1	1	1	1
1	1	1	0	0	0	1	0	1	1

C. i) Specification

-) non-overlap odd "1010" sequence recognizer
-) outputs 1 when an odd amount of non-overlapping "1010" is detected
-) State uses 3-bit binary : A, B, C (A being the MSB)
-) implementation: positive edge-triggered JK flip-flop, AND gate, OR gate, NOT gate
-) input: x
-) output: y

2) Formulation

-) State diagram and State assignment is on 1.a
-) State table is on 1.b

•) Flip-Flop input determination table

Present State			Input	Next State			Flip Flop Input						Output
A	B	C	x	A'	B'	C'	JA	KA	JB	KB	JC	KC	Y
0	0	0	0	0	0	0	0	X	0	X	0	X	0
0	0	0	1	0	0	1	0	X	0	X	1	X	0
0	0	1	0	0	1	0	0	X	1	X	X	1	0
0	0	1	1	0	0	1	0	X	0	X	X	0	0
0	1	0	0	0	0	0	0	X	X	1	0	X	0
0	1	0	1	0	1	1	0	X	X	0	1	X	0
0	1	1	0	1	0	0	1	X	X	1	X	1	0
0	1	1	1	0	0	1	0	X	X	1	X	0	0
1	0	0	0	1	0	0	X	0	0	X	0	X	1
1	0	0	1	1	0	1	X	0	0	X	1	X	1
1	0	1	0	1	1	0	X	0	1	X	X	1	1
1	0	1	1	1	0	1	X	0	0	X	X	0	1
1	1	0	0	1	0	0	X	0	X	1	0	X	1
1	1	0	1	1	1	1	X	0	X	0	1	X	1
1	1	1	0	0	0	0	X	1	X	1	X	1	1
1	1	1	1	1	0	1	X	0	X	1	X	0	1

3) Optimization

JA

		CX		\bar{C}		C			
		00	01	11	10				
		0	1	2	3				
\bar{A}	00	0	1	2	3				\bar{B}
	01	4	5	6	7	14			\bar{B}
\bar{A}	11	X ¹²	X ¹³	X ¹⁵	X ¹⁴				\bar{B}
\bar{A}	10	X ⁸	X ⁹	X ¹¹	X ¹⁰				\bar{B}
		X	X	X	X				

KA

		CX		\bar{C}		C			
		00	01	11	10				
		0	1	2	3				
\bar{A}	00	0	1	2	3	X	X	X	\bar{B}
	01	4	5	6	7	X	X	X	\bar{B}
\bar{A}	11	X ¹²	X ¹³	X ¹⁵	X ¹⁴				\bar{B}
\bar{A}	10	X ⁸	X ⁹	X ¹¹	X ¹⁰				\bar{B}
		X	X	X	X				

$$JA = BC\bar{x}$$

$$KA = BC\bar{x}$$

		JB			
		\bar{C}	C		
AB		00	01	11	10
\bar{A}	00	0	1	3	2
	01	4	5	7	6
	11	12	13	15	14
	10	8	9	11	10
\bar{B}		\bar{x}	x	\bar{x}	

		KB			
		\bar{C}	C		
AB		00	01	11	10
\bar{A}	00	x	x	x	x
	01	1	5	7	6
	11	12	13	15	14
	10	x	x	x	x
\bar{B}		\bar{x}	x	\bar{x}	

$$JB = C\bar{x}$$

$$KB = C + \bar{x}$$

		JC			
		\bar{C}	C		
AB		00	01	11	10
\bar{A}	00	0	1	x	x
	01	4	5	x	x
	11	12	13	x	x
	10	8	9	x	x
\bar{B}		\bar{x}	x	\bar{x}	

		KC			
		\bar{C}	C		
AB		00	01	11	10
\bar{A}	00	x	x	x	x
	01	x	x	x	x
	11	x	x	x	x
	10	x	x	x	x
\bar{B}		\bar{x}	x	\bar{x}	

$$JC = x$$

$$KC = \bar{x}$$

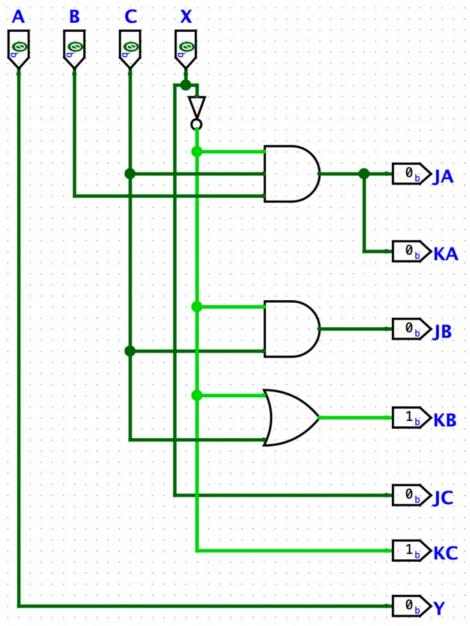
		Y			
		\bar{C}	C		
AB		00	01	11	10
\bar{A}	00	0	1	3	2
	01	4	5	7	6
	11	12	13	15	14
	10	x	x	x	x
\bar{B}		\bar{x}	x	\bar{x}	

$$Y = A$$

4) Technology Mapping

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Combinational Circuit



Sequential Circuit

