Homework 8

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1. a.

Ripple Counter	Synchronous Counter
•) flip-flops are triggered by different clocks (non-simultaneous)	•) flip-flops are triggered by the same clock (simultaneous)
•) can produce decoding error	•) cannot produce an error
•) high delay	•) low delay
•) fixed counting order	•) counting order can be specified
•) also known as Serial Counter	•) also known as parallel counter

b. The register transfer operations are specified by the following 3 basic components:

•) Set of Registers
= the set of registers in the system

•) Operations
= the operations that are performed on the data stored in the registers

•) Control of Operations
= the control that supervises the sequence of operations in the system

C. It won't be be able to do the mentioned register transfer.

A MUX can select between different input sources and route the selected input to the output. However, in the given scenario ($R_0 \leftarrow R_1$; $R_1 \leftarrow R_0$), a MUX alone cannot perform both transfers simultaneously because it operates based on a single selection.

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2.

Input ke-	Cx	Cy	Serial Output	Serial Input	Operation	Register Content
Awal	-	-	-	-	-	01101
1	1	0	1	0	Shift right	00110
2	0	1	0	1	Shift left	01101
3	1	0	1	0	Shift right	00110
4	1	0	0	1	Shift right	10011
5	1	0	1	0	Shift right	01001
6	1	1	-	-	A v B	11011
7	0	1	1	0	Shift left	10110
8	0	0	-	-	hold	10110
9	1	1	-	-	A v B	10110
10	0	1	1	0	Shift left	01100
11	0	1	0	1	Shift left	11001
12	1	0	1	0	Shift right	01100
13	1	1	-	-	A v B	11110
14	0	1	1	0	Shift left	11100
15	0	0	-	-	hold	11100

3.

Input				next state
Cx	Cy	A	B	A(t+1)
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	0
1	1	1	0	1
1	1	1	1	0

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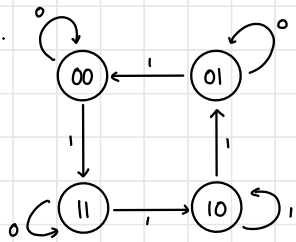
4. a.

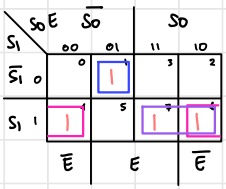


b.

Present state		input	next state	
$S_1(t)$	$S_0(t)$	E	$S_1(t+1)$	$S_0(t+1)$
0	0	0	0	0
0	0	1	1	1
0	1	0	0	1
0	1	1	0	0
1	0	0	1	0
1	0	1	0	1
1	1	0	1	1
1	1	1	1	0

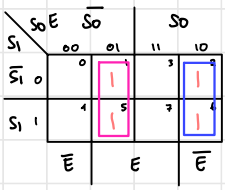
c.

$S_1(t+1)$



$S_1(t+1) = S_1\overline{E} + \overline{S_1}\,\overline{S_0}\,E + S_1 S_0$

$S_0(t+1)$



$S_0(t+1) = \overline{S_0}E + S_0\overline{E} = S_0 \oplus E$

d.