Report

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1 Motive

Through this assignment, we have upgraded the processor we have built to include caches to the memory system. We have added one cache between the IF stage and the main memory. This is the level 1 instruction cache. We also added one more cache between the MA stage and the main memory. This is the level 1 data cache.

1.1 IPC Values For Different Cache Parameters

Program	IPC	L1d = 1024 B				L1i = 1024 B			
	Without Cache	L1i=8B	L1i=32B	L1i=128B	L1i=1024B	L1d=8B	L1d=32B	L1d=128B	L1d=1024B
descending	0.009	0.015	0.017	0.018	0.017	0.016	0.018	0.020	0.017
evenorodd	0.012	0.013	0.014	0.015	0.014	0.014	0.015	0.016	0.014
fibonacci	0.011	0.012	0.015	0.017	0.014	0.013	0.015	0.018	0.014
palindrome	0.016	0.016	0.017	0.019	0.012	0.015	0.018	0.019	0.012
prime	0.012	0.014	0.015	0.016	0.013	0.014	0.016	0.017	0.013

Table 1: IPC Values for Different Cache Parameters

2 Graphs and Observations

As the L1i cache size varies while the L1d cache size remains fixed at 1kB, the graph in Figure 1 demonstrates an increase in latency alongside higher hit rates. Notably, there exists an optimal L1i cache size where the instructions per cycle (IPC) reach their maximum.

In Figure 2, when the L1d cache size is kept at 1kB and the L1i cache size is adjusted, the graph illustrates a rise in latency with increasing L1d cache size until reaching a threshold, beyond which the latency remains constant. This suggests that enhancing the instruction cache size doesn't necessarily improve performance beyond a certain point.

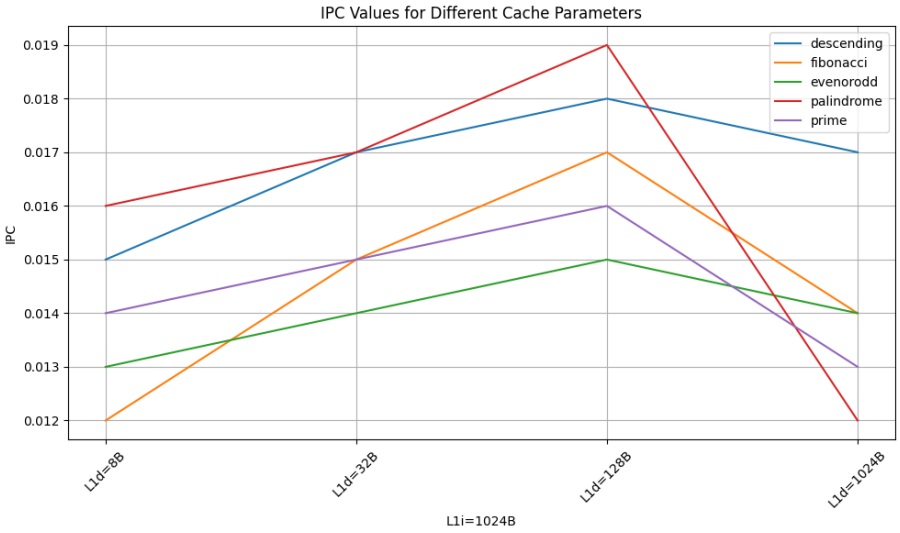

Figure 1: IPC when L1i = 1024B

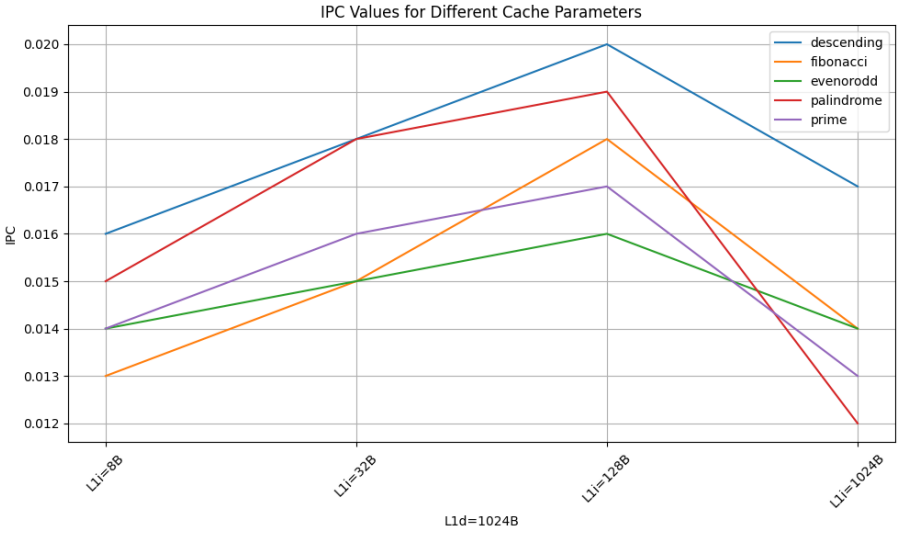

Figure 2: IPC when L1d = 1024B