Report Assignment 5

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The table below shows the number of cycles, and the throughput (Instruction per cycle) for the program that was submitted in assignment 1.

Program	**Number of Cycles**	**IPC**
descending.asm	13196	0.009
even-odd.asm	246	0.012
fibonnaci.asm	3464	0.011
palindrome.asm	2274	0.016
prime.asm	1218	0.012

Observations In this assignment we have upgraded the processor to handle discrete events.We have Event Queue that stores all the events and triger the HandleEvent() function when the current clock time plus latency equals the current time.We have implemented event calls for instruction fetch and memory access stages. Because of latency of fetching memory from main memory, clock cycle increases which leads of decrease in IPC.