B. E. ECE
Choice Based Credit System (CBCS) and Outcome Based Education (OBE)
SEMESTER – VII

COMPUTER NETWORKS

Course Code	**18EC71**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**3**	**SEE Marks**	**60**
Total Number of Lecture Hours	**40 (08 Hours / Module)**	**Exam Hours**	**03**

CREDITS – 03

Course Learning Objectives: This course will enable students to:

- Understand the layering architecture of OSI reference model and TCP/IP protocol suite.
- Understand the protocols associated with each layer.
- Learn the different networking architectures and their representations.
- Learn the functions and services associated with each layer.

Module-1	RBT Level
Introduction: Data communication: Components, Data representation, Data flow, Networks: Network criteria, Physical Structures, Network types: LAN, WAN, Switching, The Internet. **(1.1,1.2, 1.3(1.3.1to 1.3.4 of Text).** **Network Models:** Protocol Layering: Scenarios, Principles, Logical Connections, TCP/IP Protocol Suite: Layered Architecture, Layers in TCP/IP suite, Description of layers, Encapsulation and Decapsulation, Addressing, Multiplexing and Demultiplexing, The OSI Model: OSI Versus TCP/IP. **(2.1, 2.2, 2.3 of Text)**	**L1, L2**
Module-2	
Data-Link Layer: Introduction: Nodes and Links, Services, Two Categories' of link, Sublayers, Link Layer addressing: Types of addresses, ARP. Data Link Control (DLC) services: Framing, Flow and Error Control, Data Link Layer Protocols: Simple Protocol, Stop and Wait protocol, Piggybacking. **(9.1, 9.2(9.2.1, 9.2.2), 11.1, 11.2of Text)** **Media Access Control:** Random Access: ALOHA, CSMA, CSMA/CD, CSMA/CA.**(12.1 of Text).** **Wired and Wireless LANs:** Ethernet Protocol, Standard Ethernet. Introduction to wireless LAN: Architectural Comparison, Characteristics, Access Control. **(13.1, 13.2(13.2.1 to 13.2.5), 15.1 of Text)**	**L1,L2, L3**
Module-3	
Network Layer: Introduction, Network Layer services: Packetizing, Routing and Forwarding, Other services, Packet Switching: Datagram Approach, Virtual Circuit Approach, IPV4 Addresses: Address Space, Classful Addressing, Classless Addressing, DHCP, Network Address Resolution, Forwarding of IP Packets: Based on destination Address and Label. **(18.1, 18.2, 18.4, 18.5.1, 18.5.2 of Text)** **Network Layer Protocols:** Internet Protocol (IP): Datagram Format, Fragmentation, Options, Security of IPv4 Datagrams. **(19.1of Text).** **Unicast Routing:** Introduction, Routing Algorithms: Distance Vector Routing, Link State Routing, Path vector routing. **(20.1, 20.2of Text)**	**L1,L2, L3**
Module-4	
Transport Layer: Introduction: Transport Layer Services, Connectionless and Connection oriented Protocols, Transport Layer Protocols: Simple protocol, Stop and wait protocol, Go-Back-N Protocol, Selective repeat protocol. **(23.1, 23.2.1, 23.2.2, 23.2.3, 23.2.4 of Text)** **Transport-Layer Protocols in the Internet:** User Datagram Protocol: User Datagram, UDP Services, UDP Applications, Transmission Control	**L1,L2, L3**

Protocol: TCP Services, TCP Features, Segment, Connection, State Transition diagram, Windows in TCP, Flow control, Error control, TCP congestion control. **(24.2, 24.3.1, 24.3.2, 24.3.3, 24.3.4, 24.3.5, 24.3.6, 24.3.7, 24.3.8, 24.3.9 of Text)**	
Module-5	
Application Layer: Introduction: providing services, Application- layer paradigms, Standard Client –Server Protocols: World wide web, Hyper Text Transfer Protocol, FTP: Two connections, Control Connection, Data Connection, Electronic Mail: Architecture, Wed Based Mail, Telnet: Local versus remote logging.Domain Name system: Name space, DNS in internet, Resolution, DNS Messages, Registrars, DDNS, security of DNS. **(25.1, 26.1, 26.2, 26.3, 26.4, 26.6 of Text)**	**L1, L2**
Course Outcomes: At the end of the course, the students will be able to: • Understand the concepts of networking thoroughly • Identify the protocols and services of different layers. • Distinguish the basic network configurations and standards associated with each network. • Analyze a simple network and measurement of its parameters.	
Question paper pattern: • Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks. • Each full question can have a maximum of 4 sub questions. • There will be 2 full questions from each module covering all the topics of the module. • Students will have to answer 5 full questions, selecting one full question from each module. • The total marks will be proportionally reduced to 60 marks as SEE marks is 60.	
TEXT BOOK: Forouzan, "Data Communications and Networking" , 5th Edition, McGraw Hill, 2013, ISBN: 1-25-906475-3.	
REFERENCE BOOKS: 1. James J Kurose, Keith W Ross, Computer Networks, , Pearson Education. 2. Wayarles Tomasi, Introduction to Data Communication and Networking,Pearson Education. 3. Andrew Tanenbaum, "Computer networks", Prentice Hall. 4. William Stallings, "Data and computer communications", Prentice Hall,	

B. E. ECE
Choice Based Credit System (CBCS) and Outcome Based Education (OBE)
SEMESTER – VII

VLSI DESIGN

Course Code	**18EC72**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**03**	**SEE Marks**	**60**
Total Number of Lecture Hours	**40 (08 Hours / Module)**	**Exam Hours**	**03**

CREDITS – 03

Course Learning Objectives: The objectives of the course is to enable students to:

- Impart knowledge of MOS transistor theory and CMOS technologies
- Learn the operation principles and analysis of inverter circuits.
- Design Combinational, sequential and dynamic logic circuits as per the requirements
- Infer the operation of Semiconductors Memory circuits.
- Demonstrate the concepts of CMOS testing

Module-1	**RBT Level**
Introduction: A Brief History, MOS Transistors, CMOS Logic **(1.1 to 1.4 of TEXT2)** **MOS Transistor Theory:** Introduction, Long-channel I-V Characteristics, Non-ideal I-V Effects, DC Transfer Characteristics **(2.1, 2.2, 2.4 and 2.5 of TEXT2).**	**L1, L2**
Module-2	
Fabrication: CMOS Fabrication and Layout, VLSI Design Flow, Introduction, CMOS Technologies, Layout Design Rules, **(1.5 and 3.1 to 3.3 of TEXT2).** MOSFET Scaling and Small-Geometry Effects, MOSFET Capacitances **(3.5 to 3.6 of TEXT1)**	**L1, L2,**
Module-3	
Delay: Introduction, Transient Response, RC Delay Model, Linear Delay Model, Logical Efforts of Paths **(4.1 to 4.5 of TEXT2, except sub-sections 4.3.7, 4.4.5, 4.4.6, 4.5.5 and 4.5.6).** **Combinational Circuit Design:** Introduction, Circuit families **(9.1 to 9.2 of TEXT2, except subsection 9.2.4).**	**L1, L2, L3**
Module-4	
Sequential Circuit Design: Introduction, Circuit Design for Latches and Flip-Flops **(10.1 and 10.3.1 to 10.3.4 of TEXT2)** **Dynamic Logic Circuits:** Introduction, Basic Principles of Pass Transistor Circuits, Synchronous Dynamic Circuit Techniques, Dynamic CMOS Circuit Techniques **(9.1, 9.2, 9.4 to 9.5 of TEXT1)**	**L1, L2, L3**
Module-5	
Semiconductor Memories: Introduction, Dynamic Random Access Memory (DRAM) and Static Random Access Memory (SRAM), **(10.1 to 10.3 of TEXT1)** **Testing and Verification:** Introduction, Logic Verification Principles, Manufacturing Test Principles, Design for testability **(15.1, 15.3, 15.5 15.6.1 to 15.6.3 of TEXT 2).**	**L1, L2**

Course outcomes: At the end of the course, the students will be able to:

- Demonstrate understanding of MOS transistor theory, CMOS fabrication flow and technology scaling.
- Draw the basic gates using the stick and layout diagrams with the knowledge of physical design aspects.
- Demonstrate ability to design Combinational, sequential and dynamic logic circuits as per the requirements
- Interpret Memory elements along with timing considerations
- Interpret testing and testability issues in VLSI Design

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

TEXT BOOKS:

1. "CMOS Digital Integrated Circuits: Analysis and Design" - **Sung Mo Kang & Yosuf Leblebici,** Third Edition, Tata McGraw-Hill.

2. **"CMOS VLSI Design- A Circuits and Systems Perspective"-** Neil H. E. Weste, and David Money Harris4th Edition, Pearson Education.

REFERENCE BOOKS:

1. Adel Sedra and K. C. Smith, "Microelectronics Circuits Theory and Applications", 6th or 7th Edition, Oxford University Press, International Version, 2009.
2. Douglas A Pucknell & Kamran Eshragian, "Basic VLSI Design", PHI 3rd Edition, (original Edition – 1994).
3. Behzad Razavi, "Design of Analog CMOS Integrated Circuits", TMH, 2007.

B. E. (EC/TC)
Choice Based Credit System (CBCS) and Outcome Based Education (OBE)
SEMESTER – VII

DIGITAL IMAGEPROCESSING

Course Code	**18EC733**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**03**	**SEE Marks**	**60**
Total Number of Lecture Hours	**40 (08 Hours per Module)**	**Exam Hours**	**03**

CREDITS– 03

Course Learning Objectives: This course will enable students to

- Understand the fundamentals of digital image processing.
- Understand the image transforms used in digital image processing.
- Understand the image enhancement techniques used in digital image processing.
- Understand the image restoration techniques and methods used in digital image processing.
- Understand the Morphological Operations used in digital image processing.

Module1	**RBT Level**
Digital Image Fundamentals: Whatis Digital Image Processing?, Origins of Digital Image Processing, Examples of fields that use DIP, Fundamental Steps in Digital Image Processing, Components of an Image Processing System, Elements of Visual Perception, Image Sensing and Acquisition. **(Text:Chapter1andChapter2:Sections2.1to2.2,2.6.2)**	**L1,L2**
Module-2	
Image Enhancement in the Spatial Domain: Image Sampling and Quantization, Some Basic Relationships Between Pixels, Linear and Nonlinear Operations. Some Basic Intensity Transformation Functions, Histogram Processing, Fundamentals of Spatial Filtering, Smoothing Spatial Filters, Sharpening Spatial Filters **(Text:Chapter2:Sections 2.3to2.62,Chapter3:Sections3.2to3.6)**	**L1,L2**
Module-3	
Frequency Domain: Preliminary Concepts, The Discrete Fourier Transform (DFT)ofTwoVariables,Propertiesofthe2-DDFT,Filteringinthe FrequencyDomain,ImageSmoothingandImageSharpeningUsingFrequencyDomainFilters,SelectiveFiltering. **(Text:Chapter4: Sections4.2, 4.5to 4.10)**	**L1,L2**
Module-4	
Restoration:Noisemodels,RestorationinthePresenceofNoiseOnlyusingSpatialFilteringandFrequencyDomainFiltering,Linear,Position-Invariantdegradations,EstimatingtheDegradationFunction,InverseFiltering,MinimumMeanSquareError(Wiener)Filtering,ConstrainedLeastSquares Filtering. **(Text:Chapter5:Sections5.2,to5.9)**	**L1,L2**
Module-5	
Morphological Image Processing: Preliminaries, Erosion and Dilation, Opening and Closing. Color Image Processing: Color Fundamentals, Color Models, Pseudo color Image Processing. **(Text: Chapter 6: Sections 6.1 to 6.3 Chapter 9: Sections9.1to9.3)**	**L1,L2**

Course Outcomes: At the end of the course, students should be able to:

- Understand image formation and the role human visual system plays in perception of gray and color image data.
- Apply image processing techniques in both the spatial and frequency (Fourier) domains.
- Design and evaluate image analysis techniques
- Conduct independent study and analysis of Image Enhancement and restoration techniques.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Book:

DigitalImageProcessing-RafelCGonzalezandRichardE.Woods,PHI3rd Edition 2010.

Reference Books:

1. Digital Image Processing- S. Jayaraman, S. Esakkirajan,T. Veerakumar,Tata Mc GrawHill2014.
2. FundamentalsofDigitalImageProcessing-A.K.Jain,Pearson2004.
3. Image Processing analysis and Machine vision with Mind Tap by Milan Sonka and Roger Boile, Cengage Publications, 2018.

Professional Electives – 3

B. E. (EC/TC)
Choice Based Credit System (CBCS) and Outcome Based Education (OBE)
SEMESTER – VII

IoT & WIRELESS SENSOR NETWORKS

Course Code	**18EC741**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**03**	**SEE Marks**	**60**
Total Number of Lecture Hours	**40 (8 Hours / Module)**	**Exam Hours**	**03**

CREDITS – 03

Course Learning Objectives: This course will enable students to:

- Describe the OSI Model for IoT/M2M Systems.
- Understand the architecture and design principles for device supporting IoT.
- Develop competence in programming for IoT Applications.
- Identify the uplink and downlink communication protocols which best suits the specific application of IOT / WSNs.

Module-1	**RBT Levels**
Overview of Internet of Things: IoT Conceptual Framework, IoT Architectural View, Technology Behind IoT, Sources of IoT,M2M communication, Examples of IoT. Modified OSI Model for the IoT/M2M Systems, data enrichment, data consolidation and device management at IoT/M2M Gateway, web communication protocols used by connected IoT/M2M devices, Message communication protocols (CoAP-SMS, CoAP-MQ, MQTT,XMPP) for IoT/M2M devices. – Refer Chapter 1, 2 and 3 of Text 1.	**L1, L2**
Module-2	
Architecture and Design Principles for IoT: Internet connectivity, Internet-based communication,IPv4, IPv6,6LoWPAN protocol, IP Addressing in the IoT, Application layer protocols: HTTP, HTTPS,FTP,TELNET and ports. **Data Collection, Storage and Computing using a Cloud Platform:** Introduction, Cloud computing paradigm for data collection, storage and computing, Cloud service models, IoT Cloud- based data collection, storage and computing services using Nimbits. - Refer Chapter 4 and 6 of Text 1.	**L1, L2**
Module-3	
Prototyping and Designing Software for IoT Applications: Introduction, Prototyping Embedded device software, Programming Embedded Device Arduino Platform using IDE, Reading data from sensors and devices, Devices, Gateways, Internet and Web/Cloud services software development. Programming MQTT clients and MQTT server. Introduction to IoT privacy and security. Vulnerabilities, security requirements and threat analysis, IoT Security Tomography and layered attacker model. - Refer Chapter 9 and 10 of Text 1.	**L1, L2, L3**
Module-4	
Overview of Wireless Sensor Networks: Challenges for Wireless Sensor Networks, Enabling Technologies for Wireless Sensor Networks. **Architectures**: Single-Node Architecture - Hardware Components, Energy Consumption of Sensor Nodes, Operating Systems and Execution Environments, Network Architecture-Sensor Network Scenarios, Optimization Goals and Figures of Merit, Design principles for WSNs, Service interfaces of WSNs Gateway Concepts. - Refer Chapter 1, 2, 3 of Text 2.	**L1, L2, L3**
Module-5	

Communication Protocols: Physical Layer and Transceiver Design Considerations, MAC Protocols for Wireless Sensor Networks, Low Duty Cycle Protocols And Wakeup Concepts - S-MAC , The Mediation Device Protocol, Wakeup Radio Concepts, Contention based protocols(CSMA,PAMAS), Schedule based protocols (LEACH, SMACS, TRAMA) Address and Name Management in WSNs, Assignment of MAC Addresses, Routing Protocols- Energy-Efficient Routing, Geographic Routing, Hierarchical networks by clustering. - Refer Chapter 4, 5, 7 and 11 of Text 2.	**L1, L2, L3**

Course Outcomes: At the end of the course, students will be able to:

- Understand choice and application of IoT & M2M communication protocols.
- Describe Cloud computing and design principles of IoT.
- Awareness of MQTT clients, MQTT server and its programming.
- Develop an architecture and its communication protocols of of WSNs.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4sub questions.
- There will be2 full questions from each module covering all the topics of the module.
- Students will have to answer 5full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. Raj Kamal, "Internet of Things-Architecture and design principles", McGraw Hill Education.
2. Holger Karl & Andreas Willig, "Protocols And Architectures for Wireless Sensor Networks", John Wiley, 2005.

Reference Books:

1. Feng Zhao & Leonidas J. Guibas, "Wireless Sensor Networks- An Information Processing Approach", Elsevier, 2007.
2. Kazem Sohraby, Daniel Minoli, & Taieb Znati, "Wireless Sensor Networks- Technology, Protocols, And Applications", John Wiley, 2007.
3. Anna Hac, "Wireless Sensor Network Designs", John Wiley, 2003.

B. E. (EC/TC)
Choice Based Credit System (CBCS) and Outcome Based Education (OBE)
SEMESTER – VII

CRYPTOGRAPHY

Course Code	**18EC744**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**03**	**Exam Marks**	**60**
Total Number of Lecture Hours	**40 (08 Hours per Module)**	**Exam Hours**	**03**

CREDITS – 03

Course Learning Objectives: This course will enable students to:

- Understand the basics of symmetric key and public key cryptography.
- Explain classical cryptography algorithms.
- Acquire knowledge of mathematical concepts required for cryptography.
- Describe pseudo random sequence generation technique.
- Explain symmetric and asymmetric cryptography algorithms.

Module -1	RBT Level
Classical Encryption Techniques: Symmetric cipher model, Substitution techniques, Transposition techniques **(Text 1: Chapter 1)** **Basic Concepts of Number Theory and Finite Fields:** Euclidean algorithm, Modular arithmetic **(Text 1: Chapter 3)**	**L1,L2**
Module -2	
SYMMETRIC CIPHERS: Traditional Block Cipher structure, Data encryption standard (DES), The AES Cipher. **(Text 1: Chapter 2: Section1, 2, Chapter 4:Section 2, 3, 4)**	**L1,L2**
Module -3	
Basic Concepts of Number Theory and Finite Fields: Groups, Rings and Fields, Finite fields of the form GF(p), Prime Numbers, Fermat's and Euler's theorem, discrete logarithm. **(Text 1: Chapter 3 and Chapter 7: Section 1, 2, 5)**	**L1,L2**
Module -4	
ASYMMETRIC CIPHERS: Principles of Public-Key Cryptosystems, The RSA algorithm, Diffie - Hellman Key Exchange, Elliptic Curve Arithmetic, Elliptic Curve Cryptography **(Text 1: Chapter 8, Chapter 9: Section 1, 3, 4)**	**L1,L2,L3**
Module -5	
Pseudo-Random-Sequence Generators and Stream Ciphers: Linear Congruential Generators, Linear Feedback Shift Registers, Design and analysis of stream ciphers, Stream ciphers using LFSRs, A5, Hughes XPD/KPD, Nanoteq, Rambutan, Additive generators, Gifford, Algorithm M,PKZIP **(Text 2: Chapter 16)**	**L1,L2, L3**

Course Outcomes: After studying this course, students will be able to:

- Explain basic cryptographic algorithms to encrypt and decrypt the data.
- Use symmetric and asymmetric cryptography algorithms to encrypt and decrypt the information.
- Apply concepts of modern algebra in cryptography algorithms.
- Apply pseudo random sequence in stream cipher algorithms.

Question paper pattern:

- Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
- Each full question can have a maximum of 4 sub questions.
- There will be 2 full questions from each module covering all the topics of the module.
- Students will have to answer 5 full questions, selecting one full question from each module.
- The total marks will be proportionally reduced to 60 marks as SEE marks is 60.

Text Books:

1. William Stallings , "Cryptography and Network Security Principles and Practice", Pearson Education Inc., 6th Edition, 2014, ISBN: 978-93-325-1877-3
2. Bruce Schneier, "Applied Cryptography Protocols, Algorithms, and Source code in C", Wiley Publications, 2nd Edition, ISBN: 9971-51-348-X.

Reference Books:

1. Cryptography and Network Security, Behrouz A. Forouzan, TMH, 2007.
2. Cryptography and Network Security, Atul Kahate, TMH, 2003.

B. E. ECE
Choice Based Credit System (CBCS) and Outcome Based Education (OBE)
SEMESTER – VII

COMPUTER NETWORKS LAB

Course Code	**18ECL76**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**02Hr Tutorial (Instructions) + 02 Hours Laboratory**	**SEE Marks**	**60**
RBT Levels	**L1, L2, L3**	**Exam Hours**	**03**

CREDITS – 02

Course Learning Objectives: This course will enable students to:

- Choose suitable tools to model a network and understand the protocols at various OSI reference levels.
- Design a suitable network and simulate using a Network simulator tool.
- Simulate the networking concepts and protocols using C/C++ programming.
- Model the networks for different configurations and analyze the results.

Laboratory Experiments

PART-A: Simulation experiments using NS2/ NS3/ OPNET/ NCTUNS/ NetSim/QualNet or any other equivalent tool

1. Implement a point to point network with four nodes and duplex links between them. Analyze the network performance by setting the queue size and varying the bandwidth.
2. Implement a four node point to point network with links n0-n2, n1-n2 and n2-n3. Apply TCP agent between n0-n3 and UDP between n1-n3. Apply relevant applications over TCP and UDP agents changing the parameter and determine the number of packets sent by TCP/UDP.
3. Implement Ethernet LAN using n (6-10) nodes. Compare the throughput by changing the error rate and data rate.
4. Implement Ethernet LAN using n nodes and assign multiple traffic to the nodes and obtain congestion window for different sources/ destinations.
5. Implement ESS with transmission nodes in Wireless LAN and obtain the performance parameters.
6. Implementation of Link state routing algorithm.

PART-B: Implement the following in C/C++

1. Write a program for a HLDC frame to perform the following.

i) Bit stuffing
ii) Character stuffing.

2. Write a program for distance vector algorithm to find suitable path for transmission.
3. Implement Dijkstra's algorithm to compute the shortest routing path.
4. For the given data, use CRC-CCITT polynomial to obtain CRC code. Verify the program for the cases
   a. Without error
   b. With error
5. Implementation of Stop and Wait Protocol and Sliding Window Protocol
6. Write a program for congestion control using leaky bucket algorithm.

Course outcomes: On the completion of this laboratory course, the students will be able to:

- Use the network simulator for learning and practice of networking algorithms.
- Illustrate the operations of network protocols and algorithms using C programming.
- Simulate the network with different configurations to measure the performance parameters.
- Implement the data link and routing protocols using C programming.

B. E. ECE
Choice Based Credit System (CBCS) and Outcome Based Education (OBE)
SEMESTER – VII

VLSI LAB

Course Code	**18ECL77**	**CIE Marks**	**40**
Number of Lecture Hours/Week	**02Hr Tutorial (Instructions) + 02 Hours Laboratory**	**SEE Marks**	**60**
RBT Levels	**L1, L2, L3**	**Exam Hours**	**03**

CREDITS – 02

Course Learning Objectives: This course will enable students to:

- Design, model, simulate and verify CMOS digital circuits
- Design layouts and perform physical verification of CMOS digital circuits
- Perform ASIC design flow and understand the process of synthesis, synthesis constraints and evaluating the synthesis reports to obtain optimum gate level netlist
- Perform RTL-GDSII flow and understand the stages in ASIC design

Experiments can be conducted using any of the following or equivalent design tools: Cadence/Synopsis/Mentor Graphics/Microwind

Laboratory Experiments
Part – A
Analog Design

Use any VLSI design tools to carry out the experiments, use library files and technology files below 180 nm.

1. a) Capture the schematic of CMOS inverter with load capacitance of 0.1pF and set the widths of inverter with Wn = Wp, Wn = 2Wp, Wn = Wp/2 and length at selected technology. Carry out the following:
   a. Set the input signal to a pulse with rise time, fall time of 1ns and pulse width of 10ns and time period of 20ns and plot the input voltage and output voltage of designed inverter?
   b. From the simulation results compute tpHL, tpLH and td for all three geometrical settings of width?
   c. Tabulate the results of delay and find the best geometry for minimum delay for CMOS inverter?

1. b)Draw layout of inverter with Wp/Wn = 40/20, use optimum layout methods. Verify for DRC and LVS, extract parasitic and perform post layout simulations, compare the results with pre-layout simulations. Record the observations.

2. a) Capture the schematic of 2-input CMOS NAND gate having similar delay as that of CMOS inverter computed in experiment 1. Verify the functionality of NAND gate and also find out the delay td for all four possible combinations of input vectors. Table the results. Increase the drive strength to 2X and 4X and tabulate the results.

2.b)Draw layout of NAND withWp/Wn = 40/20, use optimum layout methods. Verify for DRC and LVS, extract parasitic and perform post layout simulations, compare the results with pre-layout simulations. Record the observations.

3.a) Capture schematic of Common Source Amplifier with PMOS Current Mirror Load and find its transient response and AC response? Measures the Unity Gain Bandwidth (UGB), amplification factor by varying transistor geometries, study the impact of variation in width to UGB.

1. b) Draw layout of common source amplifier, use optimum layout methods. Verify for DRC and LVS, extract parasitic and perform post layout simulations, compare the results with pre-layout simulations. Record the observations.

4. a)Capture schematic of two-stage operational amplifier and measure the following:
   a. UGB
   b. dB bandwidth
   c. Gain margin and phase margin with and without coupling capacitance
   d. Use the op-amp in the inverting and non-inverting configuration and verify its functionality
   e. Study the UGB, 3dB bandwidth, gain and power requirement in op-amp by varying the stage wise

transistor geometries and record the observations.

4. b) Draw layout of two-stage operational amplifier with minimum transistor width set to 300 (in 180/90/45 nm technology), choose appropriate transistor geometries as per the results obtained in 4.a. Use optimum layout methods. Verify for DRC and LVS, extract parasitic and perform post layout simulations, compare the results with pre-layout simulations. Record the observations.

Part - B

Digital Design

Carry out the experiments using semicustom design flow or ASIC design flow, use technology library 180/90/45nm and below

Note: The experiments can also be carried out using FPGA design flow, it is required to set appropriate constraints in FPGA advanced synthesis options

1.Write verilog code for 4-bit up/down asynchronous reset counter and carry out the following:

a. Verify the functionality using test bench

b. Synthesize the design by setting area and timing constraint. Obtain the gate level netlist, find the critical path and maximum frequency of operation. Record the area requirement in terms of number of cells required and properties of each cell in terms of driving strength, power and area requirement.

c. Perform the above for 32-bit up/down counter and identify the critical path, delay of critical path, and maximum frequency of operation, total number of cells required and total area.

2.Write verilog code for 4-bit adder and verify its functionality using test bench. Synthesize the design by setting proper constraints and obtain the net list. From the report generated identify critical path, maximum delay, total number of cells, power requirement and total area required. Change the constraints and obtain optimum synthesis results.

3.Write verilog code for UART and carry out the following:

a. Perform functional verification using test bench

b. Synthesize the design targeting suitable library and by setting area and timing constraints

c. For various constrains set, tabulate the area, power and delay for the synthesized netlist

d. Identify the critical path and set the constraints to obtain optimum gate level netlist with suitable constraints

4.Write verilog code for 32-bit ALU supporting four logical and four arithmetic operations, use case statement and if statement for ALU behavioral modeling.

a. Perform functional verification using test bench

b. Synthesize the design targeting suitable library by setting area and timing constraints

c. For various constrains set, tabulate the area, power and delay for the synthesized netlist

d. Identify the critical path and set the constraints to obtain optimum gate level netlist with suitable constraints

Compare the synthesis results of ALU modeled using IF and CASE statements.

5. Write verilog code for Latch and Flip-flop, Synthesize the design and compare the synthesis report (D, SR, JK).

6.For the synthesized netlist carry out the following for any two above experiments:

a. Floor planning (automatic), identify the placement of pads

b. Placement and Routing, record the parameters such as no. of layers used for routing, flip method for placement of standard cells, placement of standard cells, routes of power and ground, and routing of standard cells

c. Physical verification and record the LVS and DRC reports

d. Perform Back annotation and verify the functionality of the design

e. Generate GDSII and record the number of masks and its color composition

Course Outcomes: On the completion of this laboratory course, the students will be able to:

- Design and simulate combinational and sequential digital circuits using Verilog HDL
- Understand the Synthesis process of digital circuits using EDA tool.
- Perform ASIC design flow and understand the process of synthesis, synthesis constraints and evaluating the synthesis reports to obtain optimum gate level net list
- Design and simulate basic CMOS circuits like inverter, common source amplifier and differential amplifiers.
- Perform RTL-GDSII flow and understand the stages in ASIC design.

PYTHON APPLICATION PROGRAMMING
(OPEN ELECTIVE)
(Effective from the academic year 2018 -2019)
SEMESTER – VI

Course Code	**18CS752**	**IA Marks**	40
Number of Lecture Hours/Week	3:0:0	**Exam Marks**	60
Total Number of Lecture Hours	40	**Exam Hours**	03

CREDITS – 03

Course Learning Objectives: This course (18CS752) will enable students to

- Learn Syntax and Semantics and create Functions in Python.
- Handle Strings and Files in Python.
- Understand Lists, Dictionaries and Regular expressions in Python.
- Implement Object Oriented Programming concepts in Python
- Build Web Services and introduction to Network and Database Programmingin Python.

Module – 1	**Teaching Hours**
Why should you learn to write programs, Variables, expressions and statements, Conditional execution, Functions **Textbook 1: Chapters 1 – 4** **RBT: L1, L2, L3**	08
Module – 2	
Iteration, Strings, Files **Textbook 1: Chapters 5– 7** **RBT: L1, L2, L3**	08
Module – 3	
Lists, Dictionaries, Tuples, Regular Expressions **Textbook 1: Chapters 8 - 11** **RBT: L1, L2, L3**	08
Module – 4	
Classes and objects, Classes and functions, Classes and methods **Textbook 2: Chapters 15 – 17** **RBT: L1, L2, L3**	08
Module – 5	
Networked programs, Using Web Services, Using databases and SQL **Textbook 1: Chapters 12– 13, 15** **RBT: L1, L2, L3**	08

Course Outcomes: After studying this course, students will be able to

- Examine Python syntax and semantics and be fluent in the use of Python flow control and functions.
- Demonstrate proficiency in handling Strings and File Systems.
- Create, run and manipulate Python Programs using core data structures like Lists, Dictionaries and use Regular Expressions.
- Interpret the concepts of Object-Oriented Programming as used in Python.
- Implement exemplary applications related to Network Programming, Web Services and Databases in Python.

Question paper pattern:

- The question paper will have ten questions.
- Each full Question consisting of 20 marks

- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module.
- The students will have to answer 5 full questions, selecting one full question from each module.

Text Books:

1. Charles R. Severance, **"Python for Everybody: Exploring Data Using Python 3",** 1st Edition, CreateSpace Independent Publishing Platform, 2016. (http://do1.dr-chuck.com/pythonlearn/EN_us/pythonlearn.pdf)
2. Allen B. Downey, **"Think Python: How to Think Like a Computer Scientist",** 2nd Edition, Green Tea Press, 2015. (http://greenteapress.com/thinkpython2/thinkpython2.pdf) (Download pdf files from the above links)

Reference Books:

1. Charles Dierbach, **"Introduction to Computer Science Using Python",**1st Edition, Wiley India Pvt Ltd, 2015. ISBN-13: 978-8126556014
2. Gowrishankar S, Veena A, **"Introduction to Python Programming",** 1st Edition, CRC Press/Taylor & Francis, 2018. ISBN-13: 978-0815394372
3. Mark Lutz, **"Programming Python",**4th Edition, O'Reilly Media, 2011.ISBN-13: 978-9350232873
4. Roberto Tamassia, Michael H Goldwasser, Michael T Goodrich, **"Data Structures and Algorithms in Python",**1stEdition, Wiley India Pvt Ltd, 2016. ISBN-13: 978-8126562176
5. Reema Thareja, **"Python Programming Using Problem Solving Approach",** Oxford university press, 2017. ISBN-13: 978-0199480173

SAMBHRAM
INSTITUTE OF TECHNOLOGY

Department of Electronics and Communication Engineering

With Effective from 01.10.2021 Time Table for 7th Sem (2018 Scheme) & (2015 / 17 Scheme)

Day	Scheme	9:00 -10:00	10:00 -11:00	11:00 -11:15	11:15 -12:15	12:15 -01:15	01:15 -02:00	02:00 -03:00	03:00 -04:00	04:00 -05:00
Mon	2018	CCN	DIP	BREAK	VLSI	PYTH	LUNCH BREAK	Project		
	2015/17	MWA	DIP		PE	CRYP		Project		
Tue	2018	DIP	VLSI		PYTH	PYTH		VLSI B1 / CCN B2		
	2015/17	DIP	PE		CRYP	CRYP		AdC Lab		
Wed	2018	VLSI	CCN		IOT	IOT		VLSI B2 / CCN B1		
	2015/17	PE	MWA		IOT	IOT		Project		
Thu	2018	VLSI	DIP		PYTH	PYTH		Project		
	2015/17	PE	DIP		CRYP	CRYP		VLSI Lab		
Fri	2018	CCN	DIP		IOT	IOT		Project		
	2015/17	MWA	DIP		IOT	IOT		Project		
Sat	2018	VLSI	DIP		CCN					
	2015/17	PE	DIP		MWA					

Subject & Code	Faculty Name
Computer Networks	Prof. Anupama
VLSI Design	Prof. Sudha J
Digital Image Processing	Prof. X1
IoT and Wireless Sensor Networks	Dr. Ravishankar C V
Python Application Programming	Prof. Priyanka S T
Microwave and Antennas	Prof. Sowndeswari S
Power Electronics	Prof. Yoganandini
Cryptography	Dr. Ravishankar C V
Computer Networks Lab	Prof. Anupama
VLSI Lab	Prof. Sudha J
Project Work Phase 1	Prof. Sudha J
Advanced Communication Lab	Prof. Manjula Hegde
VLSI Lab	Prof. Sudha J
Intrenship	Prof. Manjula Hegde

Faculty Coordinator:

Lab Incharges: VLSI Lab: Prof. Sudha
CCN Lab: Prof: Anupama
Ad C Lab: Prof Manjula Hegde

Class Room Regular : B208

Class Room Parallel: B207