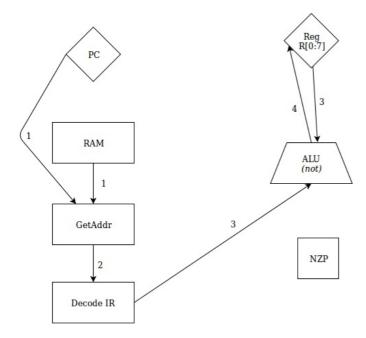
Projet Circuits & Architecture

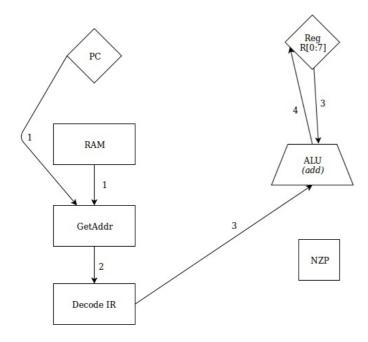
François Gaudré - Thomas Hautier

Diagrammes temporels

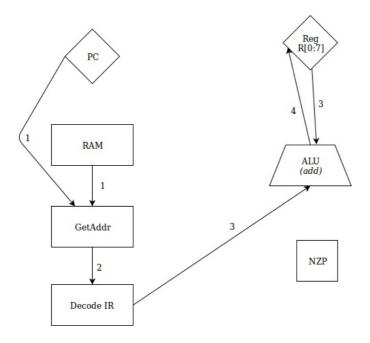
NOT



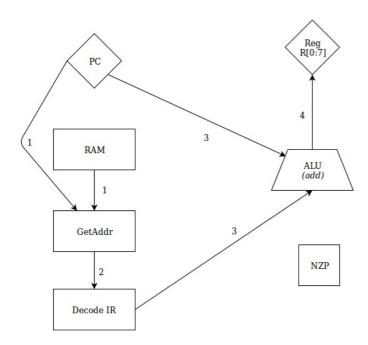
ADD



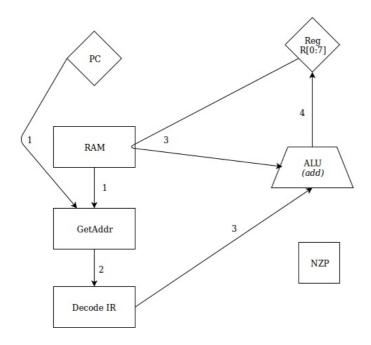
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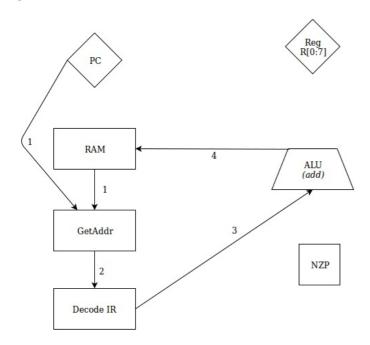
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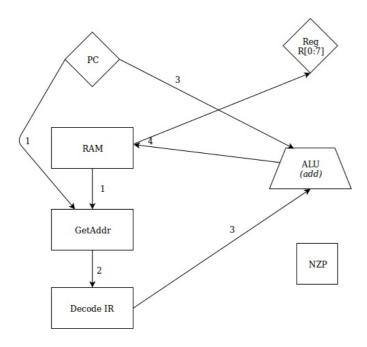
LDR



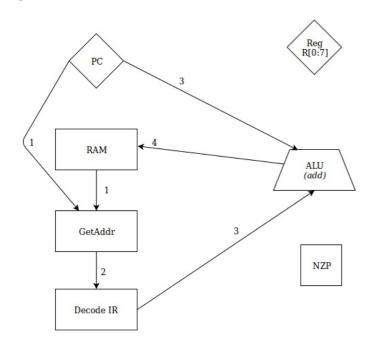
STR



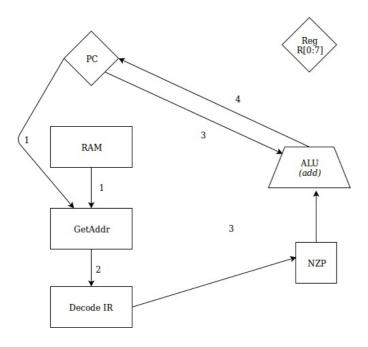
LD



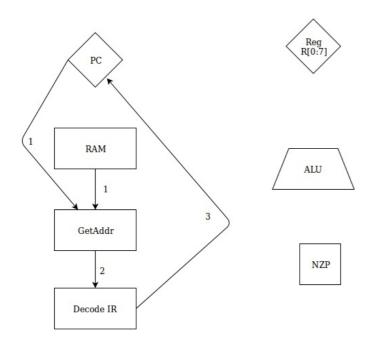
ST



BR



JMP



SETB / RSTB

