Projet Circuits & Architecture
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###Thomas Hautier

Diagrammes temporels

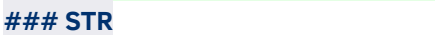
NOT

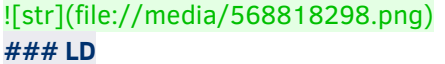

ADD


AND


###LEA


LDR


STR


LD


ST


BR


JMP


SETB / RSTB