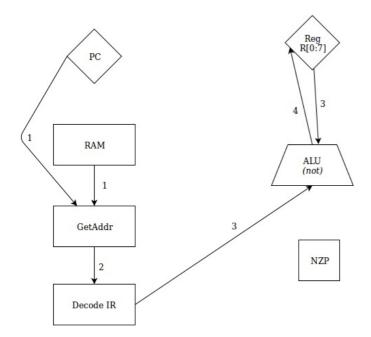
# **Projet Circuits & Architecture**

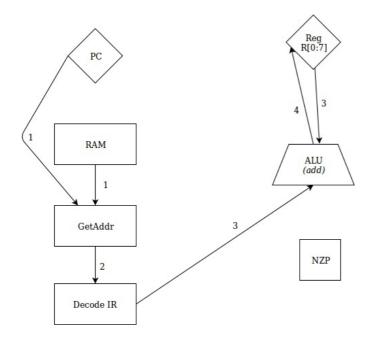
#### **Thomas Hautier**

## **Diagrammes temporels**

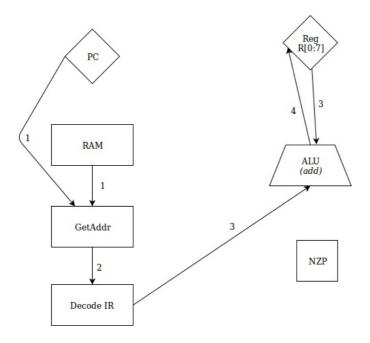
#### NOT



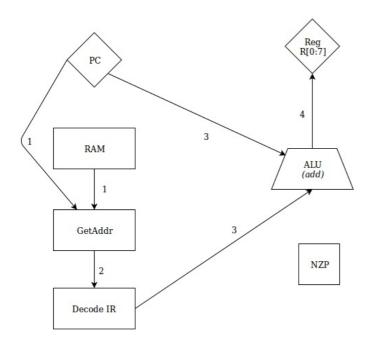
#### ADD



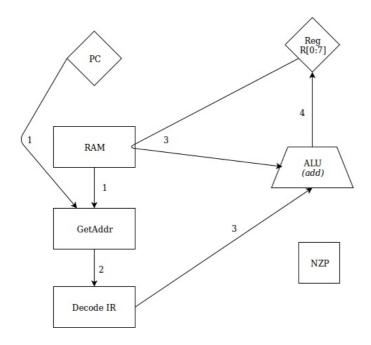
**AND** 



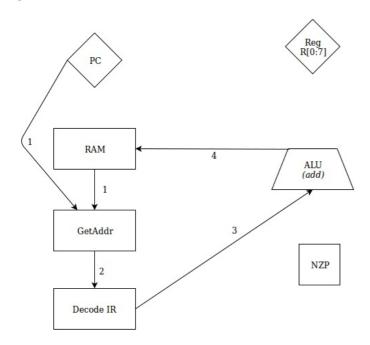
### LEA



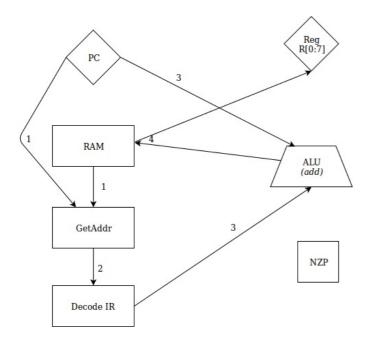
LDR



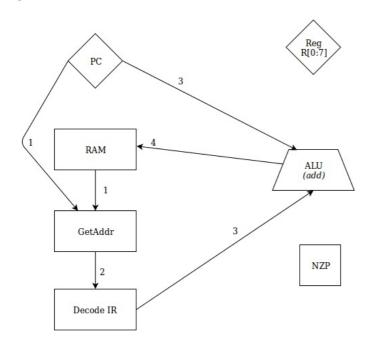
#### STR



LD



ST



BR

JMP

**SETB** 

**RSTB**