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CALCULATION OF LATERAL DISTRIBUTION OF INTERFACE TRAPS ALONG AN MIS CHANNEL

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ABSTRACT

The lateral distribution of interface traps, averaged over the semiconductor band gap, is calculated in an MIS structure. The calculation is based on the well-known charge-pumping technique. The calculation has been applied to P-channel MOSFET's.

INTRODUCTION

Understanding the location of interface trap generation in MOSFET's under stress has become critical for building reliability into device operation at the microscopic design level. Interface traps cause direct changes in transconductance, subthreshold slope, and noise figure [1-4]. They are also indirect evidence of hot carriers in MOSFET's, and can aid in creating physical, microscopic models of hot carrier transport.

In MOSFET's, interface traps have been characterized in three ways: as an average value over both the surface energy band gap and channel length, N_{it} (cm^{-2}) [5,6]; as an average over the band gap, but not channel length, $N_{it}(x)$ (cm^{-2}) [6]; and as an average over channel length, but not surface potential energy in the band gap, $D_{it}(\Psi)$ ($eV^{-1}cm^{-2}$) [7-9]. [No work to date has looked at the full $D_{it}(x,\Psi)$.]

Lately, the method of choice for characterization of interface traps has been the charge-pumping technique [10,11,6]. In particular, we develop here an alternate method to [7] for finding $N_{it}(x)$ (cm^{-2}). As before, the method is based on profiling the interface traps versus position near the drain by varying the junction reverse bias. Peak charge-pumping current is measured versus reverse junction bias. Increasing reverse bias causes the source-drain space-charge regions to grow. Their extension effectively reduces the channel length. For charge-pumping applications, this means a smaller channel area will contribute to the charge-pumping current. Any interface traps located in the depleted region will be effectively masked and unable to contribute to I_{cp}. The combination of changes in I_{cp} and channel length are used to extract $N_{it}(x)$ versus position along the channel. This alternate method appears simpler than the previous one, as shown in the derivation below; at the same time, it avoids the crucial assumption of constant $N_{it}(x)$ in prestressed devices made in [7].

Several assumptions are made. First, any damage, i.e. interface trap generation, is assumed to occur only on the drain side of the channel. Therefore, the interface trap distribution on the source side is assumed to be the same before and after stress. Second, the spatial distributions of interface traps are assumed to be the same (not necessarily constant) on both source and drain sides, prior to any stress.

To begin the derivation, energy-averaged interface traps may be expressed as:

$$N_{it}(x) = \int_{E_v}^{E_c} D_{it}(x,\Psi)\, d\Psi \qquad (1)$$

That is, the surface potential Ψ, controlled by the gate bias of the charge-pumping measurement, is assumed to span the entire semiconductor band gap. The energy-averaged interface traps then come from integrating $D_{it}(x,\Psi)$ over this band gap.

The charge-pumping current I_{cp} is calculated according to:

$$I_{cp} = q \bullet f \bullet W \int_{\frac{-L(V_r)}{2}}^{\frac{L(V_r)}{2}} dx \int_{E_v}^{E_c} D_{it}(x,\Psi)\, d\Psi \qquad (2)$$

Charge q, frequency f, and MOSFET channel width W control part of I_{cp}. The two integrals take $D_{it}(x,\Psi)$ into account, adding up contributions across the band gap and along the channel. Note that the reverse-bias-dependent source depletion edge is defined to be at $x=-L(V_r)/2$, with the drain edge at $+L(V_r)/2$. Thus, the center of the channel is defined to be x=0, and is independent of V_r.

$N_{it}(x)$ for an unstressed device can be found using these equations. Define the unstressed charge-pumping current I_{cp0} as:

$$I_{cp0} = 2 \bullet q \bullet f \bullet W \int_{0}^{\frac{L(V_r)}{2}} dx\ N_{it0}(x) \qquad (3)$$

Here, the factor of '2' and the change of the integral's lower limit stem from the assumption of $N_{it}(x)$ being symmetric at source and drain for the unstressed device.

Taking the derivative with respect to 'L' of I_{cp0} will allow calculation of $N_{it0}(x)$:

$$\frac{dI_{cp0}}{dL} = 2 \bullet q \bullet f \bullet W \bullet \frac{d}{2 \bullet d(\frac{L}{2})} \int_{0}^{\frac{L(V_r)}{2}} dx\ N_{it0}(x) \qquad (4)$$

$$= q \bullet f \bullet W \bullet N_{it0}(\frac{L}{2}) \qquad (5)$$

Inverting this last equation, and applying the chain rule ($d/dL=\{d/dV\}\{dV/dL\}$):

$$N_{it0}(\frac{L}{2}) = \frac{1}{q \bullet f \bullet W} \frac{dI_{cp0}}{dV_r} \frac{dV_r}{dL} \qquad (6)$$

Measurements of dI_{cp0}/dV_r, and measurements or simulation of dV_r/dL, thus allow extraction of $N_{it0}(x)$, where $x=L/2$ and is dependent on the applied reverse bias.

For a device after stress, $N_{it}(x)$ near the drain (injection region) no longer looks like its counterpart $N_{it0}(x)$ near the source. Proceeding as before:

$$I_{cp} = q \bullet f \bullet W \int_{\frac{-L(V_r)}{2}}^{\frac{L(V_r)}{2}} dx\ N_{it}(x) \qquad (7)$$

$$= q \bullet f \bullet W \left[\int_{\frac{-L(V_r)}{2}}^{0} dx\ N_{it}(x) + \int_{0}^{\frac{L(V_r)}{2}} dx\ N_{it}(x) \right] \qquad (8)$$

Since the first integral in Equation (8) is over the *unstressed* part of the channel, we may convert it:

$$\int_{-\frac{L(V_r)}{2}}^{0} dx\ N_{it}(x) \;=\; \int_{-\frac{L(V_r)}{2}}^{0} dx\ N_{it0}(x) \;=\; \int_{0}^{\frac{L(V_r)}{2}} dx\ N_{it0}(x) \qquad (9)$$

Making this substitution, and taking the derivative again with respect to channel length L, we get:

$$\frac{dI_{cp}}{dL} \;=\; q \bullet f \bullet W \left[\frac{d}{2 \bullet d(\frac{L}{2})} \int_{0}^{\frac{L(V_r)}{2}} dx\ N_{it0}(x) + \frac{d}{2 \bullet d(\frac{L}{2})} \int_{0}^{\frac{L(V_r)}{2}} dx\ N_{it}(x) \right] \qquad (10)$$

$$= \frac{q \bullet f \bullet W}{2} \left[N_{it0}(\tfrac{L}{2}) + N_{it}(\tfrac{L}{2}) \right] \qquad (11)$$

where the last step, as before, results from the derivative with respect to the limit of a definite integral. Re-arranging, and using the chain rule one last time, gives the final result:

$$N_{it}(\tfrac{L}{2}) = \frac{2}{q \bullet f \bullet W} \frac{dI_{cp}}{dV_r} \frac{dV_r}{dL} - N_{it0}(\tfrac{L}{2}) \qquad (12)$$

APPLICATION

The following experimental measurements and analysis steps are needed to evaluate $N_{it}(x)$. 1) Obtain I_{cp} vs. V_r data before and after stress. 2) Calculate dI_{cp}/dV_r. 3) Determine L vs. V_r with a one- or two-dimensional approximation, or by measurement. 4) Calculate dL/dV_r (using a curve fit from L vs. V_r). 5) Calculate N_{it} vs. V_r from the I_{cp} data obtained. 6) Calculate $N_{it}(x)$ from Equation (12).

We have applied the technique to determination of lateral interface traps in P-channel MOSFET's [12]. PISCES [13] was used to establish carrier density versus

lateral position along the interface, as a function of reverse junction bias. This was necessary in order to determine the channel length -- defined by the depletion edge in the channel -- as a function of reverse bias. Care was taken to identify the location of the depletion edge, as discussed elsewhere [14].

Figure 1 shows the experimental setup. Figure 2 shows the results of applying the new method to measurements on a PMOS transistor.

DISCUSSION

The new technique employed here allows determination of interface trap density, averaged over the band gap, as a function of position along the FET channel -- regardless of whether the device has been stressed or not. That is, no assumption is made of uniform $N_{it}(x)$ in the unstressed device, as in [7]. We note allusion to a technique was made in [9]. However, no calculations were presented in that work, which led us to attempt them independently, with the results presented above.

Our calculated $N_{it}(x)$ in the PMOS FET (Figure 2) reveals similarities to the NMOS device results presented in [9], both before and after stress, as we have discussed elsewhere [12]. In particular, we note a non-uniform interface trap density near the junctions of the *unstressed* device. We believe this is due to enhanced interface trap densities above heavily-doped junction regions. An alternative explanation exists for the increase [9]; that is, electric field-enhanced emission of trapped charges near junctions, rather than increased numbers of interface traps. Simulations of vertical field near the drain junction [12] appear to refute this explanation, leaving heavy doping effects as the likely candidate.

CONCLUSIONS

We have derived a new method for calculating lateral interface trap densities in MIS devices, based on measurements of charge-pumping current versus

junction reverse bias. The new method improves on previous ones by eliminating the critical assumption of uniform interface trap density prior to device stress. The method thus can be used to find lateral interface trap densities in unstressed devices. We have applied the new method to PMOS FET's, and obtained results similar to those reported in NMOS transistors.

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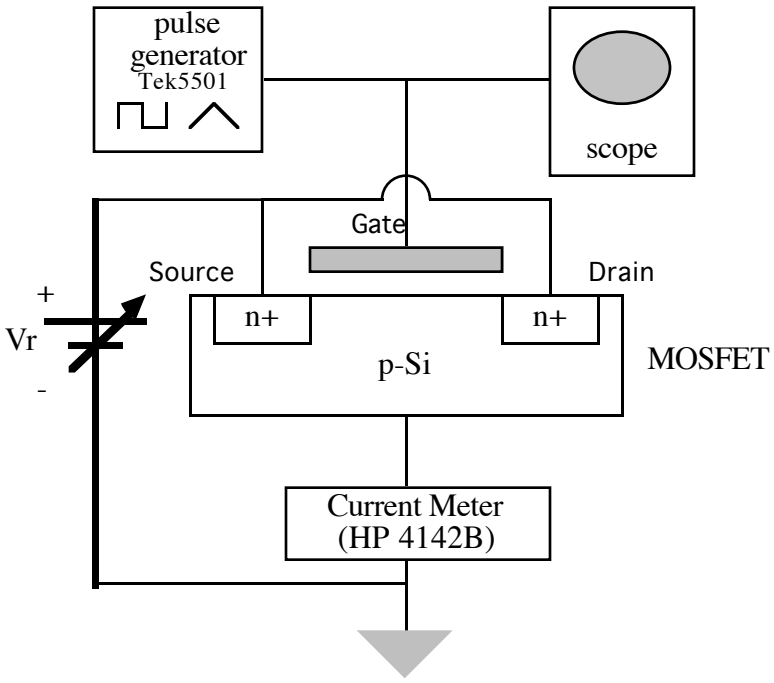
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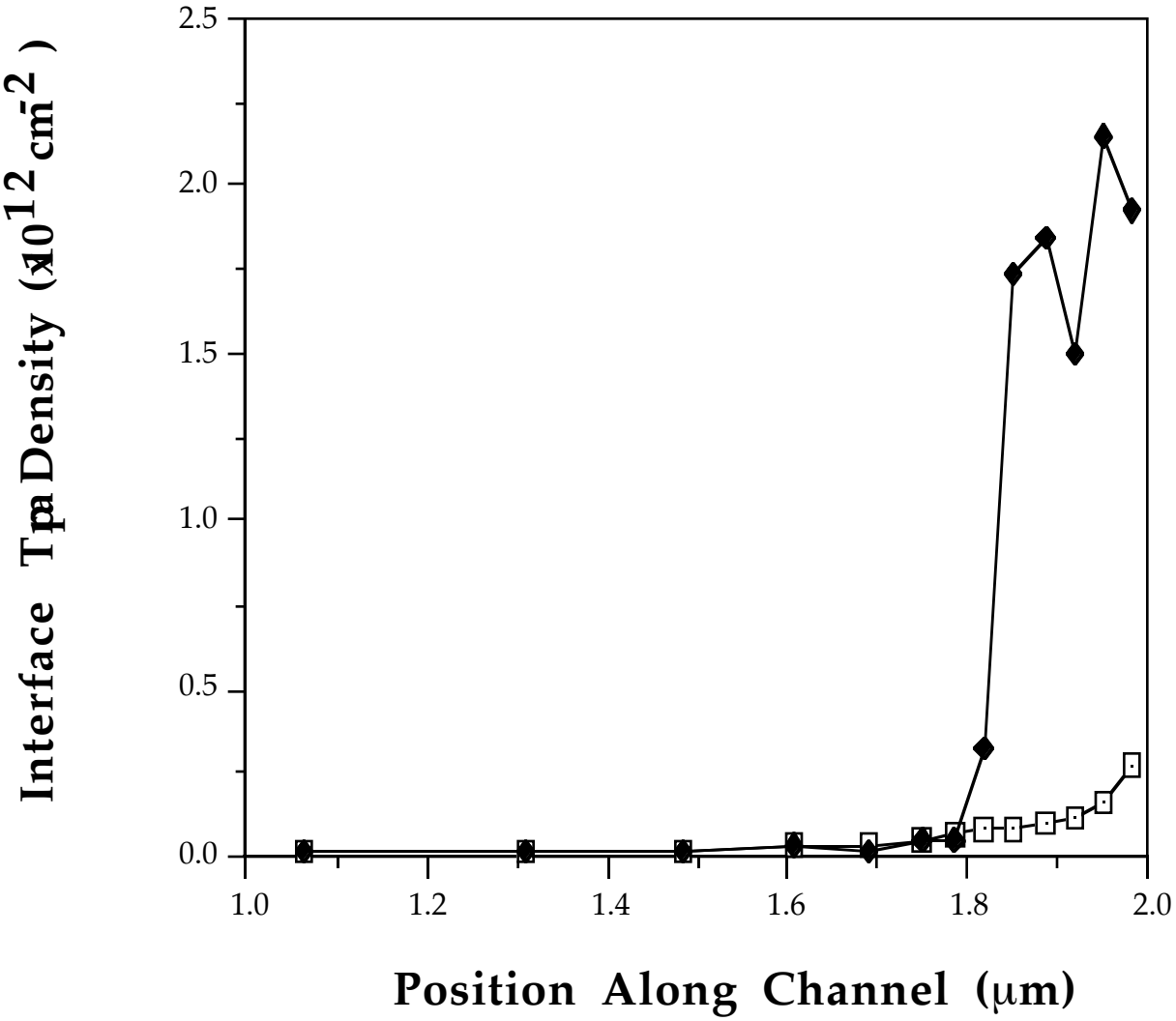
Interface Trap Density ($\times 10^{12}$ cm^{-2})
2.5
2.0
1.5
1.0
0.5
0.0
1.0
1.2
1.4
1.6
1.8
2.0
Position Along Channel (μm)

FIGURE CAPTIONS

Figure 1. Schematic of charge-pumping measurement set-up. Polarities for the PMOS devices measured in this work are reversed from the figure.

Figure 2. Interface trap density $N_{it}(x)$ versus channel position, before and after stress, for a PMOSFET with W=25μm, L_{eff}=1.7μm (300K). The drain metallurgical junction is located at 1.78μm on the scale above. Pre-stress trap density shown by open rectangles. Post-stress trap density shown by filled diamonds. Stress condition was 120 min., V_{DS}=-10V, V_{GS}=-2.5V.