Two-step Glass Wet-etching for Micro-fluidic Devices

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Abstract— **In this paper a two-step glass wet-etching process is presented. This process allows the fabrication of well-defined shallow recesses (typically 1-40μm) together with deep trenches or wafer-through holes (100-500μm) in the same glass wafer. The etching solutions and the masking materials used are described for the three glass types frequently used in sensor fabrication. This process is developed in such a way that anodic bonding to a second wafer is not disturbed by the wet etching process. The integration of micro-detectors in the etched micro-channels as well as the mounting of fluid connectors (capillaries) is therefore possible. In this way a complete micro-fluidic device can be realized.**

Keywords— **glass etching, micro-channels, micro-fluidic devices.**

I. Introduction

In a complete micro-fluidic device, channels have to be etched in glass wafers, micro-detectors for measuring fluid properties have to be integrated in such channels and sealing of the channels is obviously needed. Anodic bonding to another wafer is often used to seal the channels and very deep recesses or wafer-through holes are required for the mounting of fluid connectors (capillaries). The anodic bonding process requires smooth and clean surfaces as well as specific intermediate layers, while for wafer-through etching a masking material that can withstand the etchant for several hours is needed. Therefore, etching solutions that provide cavities of the desired shape and surface quality as well as proper masking layers are essential. Both these issues have been addressed and a process has been developed to overcome some of the problems frequently encountered in glass etching. This process is presented here. The most suitable masking layers, their deposition and patterning conditions are reported as well. Finally an etching scheme that allows a two-step glass wet etching is described.

II. Wet Etching of the Glass

Silicon etching techniques, both wet and dry, have already been studied extensively as they are widely used in IC and MEMS fabrication. Etching of glass is a much less investigated process. In addition, glass etching is more difficult because the glass wafers are not pure silicon oxide, but other components that have a different etch rate in the etching solutions are added to it. In fact, for microsystems using bonded stack of silicon and glass wafers, the glass wafers should have a thermal expansion coefficient close to that of silicon. This is achieved by altering the glass composition. Among the glass wafers most frequently used for sensors are Corning #7740, Schott #8330, and Hoya SD-2 glasses. Therefore, our experiments focus on the etching of these wafers.

Recesses, trenches, and holes as shallow as 10μm and as deep as 500μm are generally fabricated by wet etching in HF-based solutions. These solutions do etch glass at rather fast rates, but often produce irregular shapes and increase surface roughness. Moreover a masking layer to protect regions from undesired etching is required. Photoresist can only be used up to an etch depth of 5μm [1]. For deeper structures it does not withstand HF solution long enough. Thus alternative masking layers that can be deposited onto glass have to be found. For all three types of glass wafers used in this experiment (Corning #7740, Schott #8330, and Hoya SD-2), etching in HF solutions resulted in poor definition of the etched structures and in an increase in surface roughness. Both effects are due to the composition of the glass. In particular the aluminium oxide content in the glass wafer – content that can vary from one wafer type to the other – is responsible for the irregular shape and remaining roughness of the etched recesses.

In order to overcome this problem an etching solution that etches aluminium oxide as well as silicon

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oxide is investigated. Of course, a masking layer that can withstand wafer-through etching in such solution has to be found as well before such solution is considered acceptable.

A. Glass etching solution

The aluminium oxide content of the glasses used causes the remaining roughness and irregular shape of the recesses after the etching process. In fact as the aluminium oxide is not etched in HF, grains are remaining in the recess during etching hampering the contact between the silicon oxide and the fluoride ions. In the Corning #7740 and Schott #8330 glasses the aluminium oxide content is only 2.3% [2, 3]. However, the deposition of a polysilicon layer, generally used as masking layer, at 545°C is responsible for clustering of the aluminium oxide. The Hoya SD-2 glass wafers contain more than 20% aluminium oxide [4]. This large content results in recesses filled with a white powder after etching, indicating aluminium oxide residuals. From these observations it was clear that it is essential to find an etchant in which aluminium oxide can be removed, preferably with the same etch rate of the silicon oxide. Moreover, this etch rate should also be rather high as often very deep channels and wafer-through holes are needed.

A mixture of phosphoric acid (H_3PO_4), a known etchant for aluminium oxide [5], and HF is one possible solution. In order to find an optimal concentration of both compounds a closer look to the etch rate depending on concentration of the acids has been taken and etch tests have been performed. A fixed etch time of 1 h was selected while the bath temperature was kept at 70°C for all these experiments. The maximum and minimum etch depths obtained for various acid concentrations are reported in Table 1.

The etch rate does increase substantially with increasing HF vol%. The uniformity is rather good for HF vol% larger then 2. These considerations together with the effect on surface quality made us select a 5:70 vol.% ratio for further experiments.

TABLE I
GLASS ETCHING IN HF/H_3PO_4 MIXTURES AT 70°C.

HF vol.%	H_3PO_4 vol.%	Min. depth μm	Max. depth μm
0.5	84	3.2	6
1	82.8	6.5	10.5
1.5	81.8	11	15
2.5	79.5	34	34
5	70	49	49

B. Masking materials

Among the materials available in IC-technology only a few can withstand hydrofluoric acid and phosphoric acid. As the glass wafers cannot be brought to high temperatures, the possible candidates as masking layer have to be layers that can be deposited at temperatures close to or lower than the softening point of the glass. LPCVD amorphous silicon, PECVD silicon carbide and sputtered titanium nitride have been investigated. Titanium nitride can be sputtered at 250°C and patterned by dry etching. Thin films of TiN sputtered on glass have a rather large compressive stress and also show poor adhesion. In fact even for a relatively short etch time of 30 minutes, a severe deformation of the patterned area is obtained as illustrated in Fig. 1. Therefore TiN is not suitable as masking layer for glass etching.

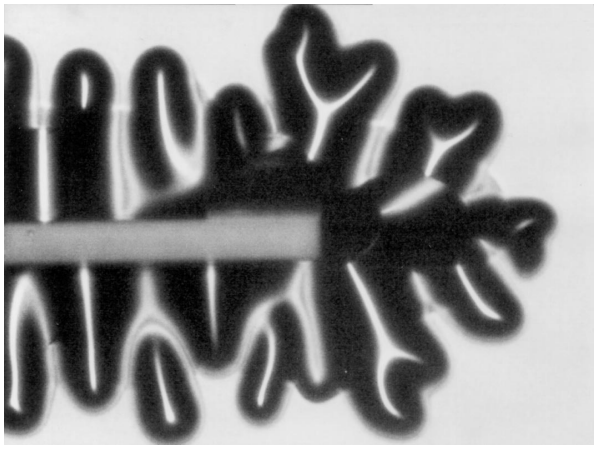

Fig. 1. Titanium nitride mask after 30 minutes etching in a 70% H_3PO_4 and 5% HF aqueous solution (Magnification 50×).

Amorphous silicon or silicon carbide deposited on the glass wafers although behaving much better than TiN in terms of adhesion and stress, cannot be used for a full wafer-through etching. In fact, due to the relatively low deposition temperatures used pinholes are present in these layers. These pinholes result in week spots in the masking behaviour. For amorphous silicon the effect of these pinholes is visible after a 3 - 4 hrs etch in the phosphoric acid/hydrofluoric acid mixture described in the previous section. For silicon carbide this is the case already after 1 hr. The effect of pinholes in these layers is even more pronounced in 40% HF solutions. However, a combination of both layers might offer a successful alternative. A double layer consisting of 400nm-thick amorphous silicon and 500nm-thick silicon carbide was tested. No damage or undesired etching was detected after 10 hrs in the HF/H_3PO_4-mixture. As this etch time is sufficient for wafer-through etching this double layer can be used as masking layer for deep recesses in glass wafers.

III. Two-step Etching Process

In micro-fluidic devices very often two different etch-depths on the same wafer are required. Shallow or deep channels as well as wafer-through holes for fluidic connectors have to be fabricated. A two-layer masking approach might be quite convenient in this case. As the surface topography is rather altered after a first etch step of several microns the masking layers for both recesses have to be patterned before the first etching starts. The fabrication sequence of a two-step etching is shown in Fig. 2.

The process starts with the deposition of a 600nm-thick LPCVD amorphous silicon layer on the glass wafer using the process parameters reported in Table 2. This layer is patterned on the wafer front-side to define the channels or shallow recesses. A conventional silicon dry etching step is used to remove the a-Si from the exposed windows (Fig.2b).

TABLE II
LPCVD amorphous silicon deposition parameters

Gas flow (sccm)	Pressure (Pa)	Temperature (°C)	Deposition rate (nm/min)
$SiH_4 = 45$	20	545	1.2

At this point the double layer consisting of 400nm-thick amorphous silicon and 500nm-thick PECVD silicon carbide is deposited as shown in Fig. 2c. The parameters used for the SiC deposition are summarized in Table 3.

TABLE III
PECVD SiC deposition parameters

Gas flow (sccm)	$SiH_4 = 100$, $CH_4 = 3000$
HF power (W)	500
LF power (W)	500
Pressure (Pa)	300
Temperature (°C)	400
Deposition rate (nm/min)	70

The second mask is now applied to pattern the stack of three layers (double a-Si and SiC) to define the deeper recesses or wafer-through holes. Once more dry etching is used to etch the layer stack from the exposed windows (see Fig.2d). At this point the first glass etch step is performed. This will be the deeper of the two etching steps.

After this first glass etch step the SiC/a-Si layer is removed by reactive ion etching in an ALCATEL-system using the parameters reported in Table 4. In this step the amorphous silicon and the silicon carbide have to be removed without applying a mask, while

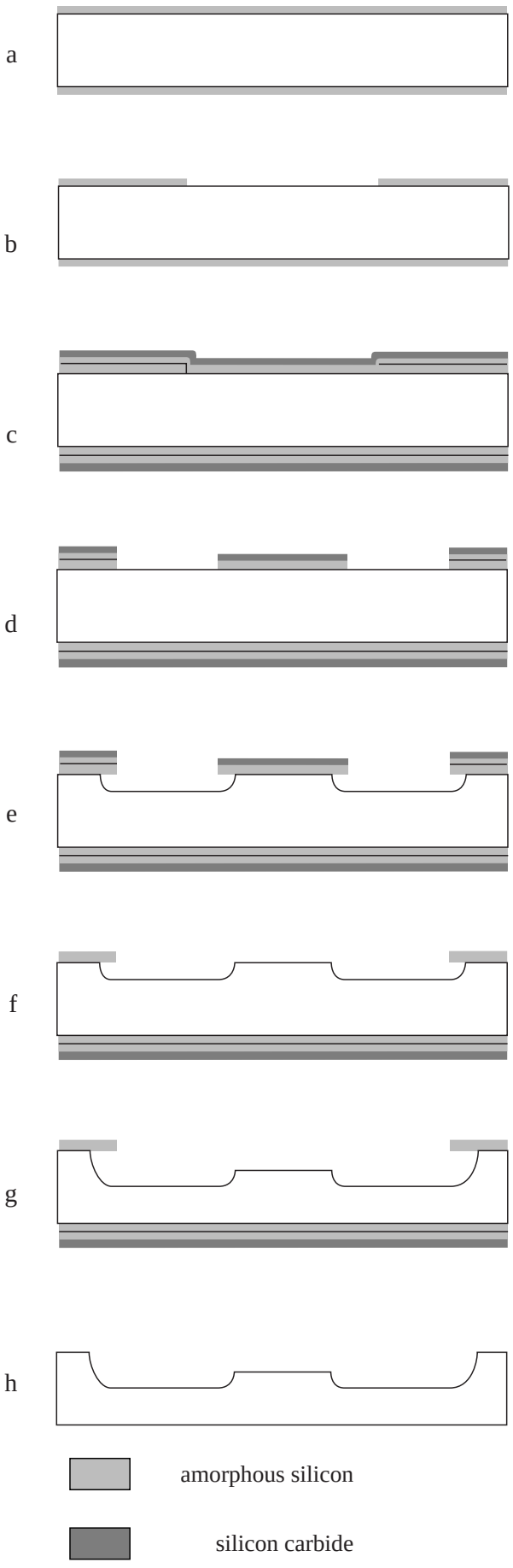

Fig. 2. Fabrication sequence of wet-etched shallow and deep recesses in glass.

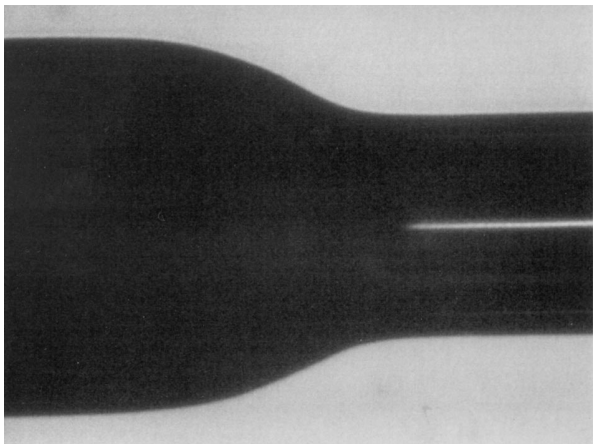

Fig. 3. Optical image of a 400 μm-deep recess (left), together with a 100 μm deep and 200 μm wide channel (right) fabricated by two-step etching.

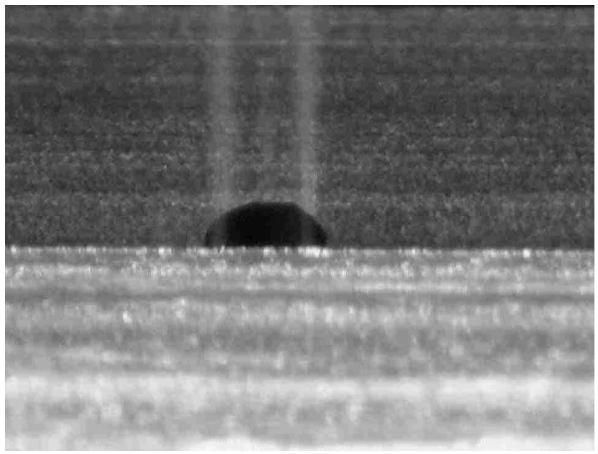

Fig. 4. Optical image of a cross-section of a 100 μm deep and 200 μm wide channel etched in glass.

the underlying amorphous silicon is left to protect the area outside the recesses (see Fig.2f). Because of the higher etch rate of amorphous silicon in a plasma containing fluoride ions the participation of a chemical reaction has to be excluded, otherwise the timing of the etch step would be very critical. That's why a Cl chemistry is preferred as it results in the same etch rate for both materials.

TABLE IV
RIE parameters for a-Si and SiC

Gas flow (sccm)	Pressure (Pa)	Power (W)	Etch rate (nm/min)
$BCl_3 = 22$ $Cl_2 = 7$ $N_2 = 100$	3	40	50

With the remaining a-Si layer as mask, the glass etch is resumed to define the shallow recesses, while the etching of the deep recess is continued (Fig. 2g). Finally the silicon carbide is removed by reactive ion etching, using the RIE process in Table 4. The remaining amorphous silicon layer is stripped in a 25wt% Tetra Methyl Ammonium Hydroxide (TMAH) water solution with a very high selectivity to the glass in order to avoid any damage to the glass surface that could negatively affect the bonding.

An example of a two-level etched structure is shown in Fig. 3. The 400μm-deep recess is the wide structure on the left, while the 100μm- deep micro-channel is visible on the right. Fig. 4 shows the cross section of a 100 μm deep and 200 μm wide channel etched in a glass wafer and bonded to a silicon wafer.

IV. Conclusions

An improved wet etching process for microstructuring of glass wafers has been developed. The effect of solution concentration on the shape and roughness of the etched structures has been presented. The best results are achieved for a 5%HF and 70%H_3PO_4 etch mixture at 70°C. A double masking layer is preferred for deep recesses or wafer-through etching as it offers a better protection against the etchants. LPCVD amorphous silicon and PECVD silicon carbide have been selected as suitable masking layers.

A two-etch step process has been developed that allows the fabrication of two different etch-depths on the same wafer. Shallow or deep channels as well as wafer-through holes for fluidic connectors can be realized in this way. This is achieved by patterning all the desired structures in a multi-layer mask before the etching starts so that a fully planar surface is used during lithography. Two etching steps with a masking layer removal in between are employed to fabricate well-defined and smooth shallow and deep recesses on the same wafer.

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