

# DEEP WET AND DRY ETCHING OF PYREX GLASS: A REVIEW

CIPRIAN ILIESCU<sup>1</sup>, KWONG LUCK TAN<sup>1</sup>, FRANCIS E.H. TAY<sup>1,2</sup>, and JIANMIN MIAO<sup>3</sup>

<sup>1</sup>Institute of Bioengineering and Nanotechnology, Singapore

<sup>2</sup>Department of Mechanical Engineering, National University of Singapore, Singapore

<sup>3</sup>Micromachines Center, School of MPE, Nanyang Technological University, Singapore

E-mail: [ciliescu@ibn.a-star.edu.sg](mailto:ciliescu@ibn.a-star.edu.sg)

## ABSTRACT

This paper is a review of wet and dry etching of one of the most common types of glass: Pyrex. The paper analyzes the methods for increasing the glass etch rate in HF solutions, namely, annealing, concentration, ultrasonic agitation and temperature. The limitations of the wet etching of glass are also presented. Masking layers commonly used for deep wet etching of glass are analyzed, in terms of the process time required until the defects are generated in the masking layer. The improvement of the surface roughness for deep wet etching of Pyrex glass is another subject that will be explored. The highest etch depth – 500  $\mu\text{m}$  – of annealed Pyrex glass is achieved by wet etching in highly concentrated HF solution, using Cr/Au with the assistance of photoresist as a masking layer. The paper also reports a new technique of dry etching of Pyrex glass in  $\text{C}_4\text{F}_8$  using bulk silicon mask.

**Keywords:** glass etching, masking layer,

## 1. INTRODUCTION

Glass is a widely used material in MEMS and biochip device fabrication. The classical piezoresistive pressure sensor chip is bonded on a glass substrate. A microgyroscope that is vacuum-sealed between two structured glasses at the wafer level is presented in [1]. A micro-XY-stage actuator made with glass has been reported in [2]. Most biochips are fabricated on a glass substrate due to its optical transparency and biocompatibility. A microflow of cells for the single molecule handling of DNA is presented in [3]. A microPCR for DNA amplification is shown in [4], while dielectrophoresis is represented in [5].

Three major groups of techniques are used in glass etching: mechanical, dry and wet. Mechanical methods include traditional drilling, ultrasonic drilling, electrochemical discharge or powder blasting. However, smooth surfaces cannot be generated using such methods. The dry etching technique of glass has been reported in [6] using  $\text{SF}_6$ . However, the etching rate is relatively low. Wet etching is the most common method. The type of masking layer that should be used depends on the application and "thermal budget" of the fabrication process of the device. Photoresist is very often used

as the mask layer [7-9], but its area of application is limited. A commonly used mask is Cr/Au [10, 11], where the Cr layer is used to improve the adhesion of gold to glass. Bu *et al* [11] reported the etching of a 500 $\mu\text{m}$ -thick glass wafer using multilayers of metal, Cr/Au/Cr/Au, in combination with a thick SPR220-7 photoresist, by etching from both sides of the wafer. Another commonly used mask material for glass etching is silicon – PECVD (amorphous silicon) [9,12], LPCVD (polysilicon) [10,13] or even bulk silicon [14] – all of which are deposited using different methods. The maximum reported depth was 320  $\mu\text{m}$  by Bien *et al* [9], using a mask of polished polysilicon and SU8 as the mask.

## 2. EXPERIMENTS AND MATERIALS

We focused our experiments on one of the most popular types of glass, Corning 7740. Two of its main properties make it suitable for microfabrication. Firstly, Corning 7740 is bondable to silicon and its thermal coefficient of expansion is similar to silicon. This can result in low residual stress being induced in the MEMS structure. Secondly, it contains a low concentration of oxides that gives insoluble products in HF solution. As presented in [15], these insoluble products can act as a micromasking layer and generate rough surfaces, or can drastically reduce the etch rate.

The technique used for the stress characterization of the layers deposited on glass is described in [12]. This technique consists of the deposition of a thin reflective layer (50 nm Cr) on both sides of the wafer. The stress induced by the deposition on one side of the wafer is compensated by the stress introduced by the same Cr layer on the opposite surface.

The experiment was performed on 500- $\mu\text{m}$  thick, unannealed and annealed 4" glass wafers. The annealing was performed at 560°C in a  $\text{N}_2$  environment for 6 hours. The wafers were first cleaned in piranha solution ( $\text{H}_2\text{SO}_4/\text{H}_2\text{O}_2$  2/1), then rinsed in DI water and spun-dried. The wet etching of the glass wafers was conducted in a sealed Teflon container with slow magnetic stirring. A silicon wafer was bonded to the glass wafer using wax to protect the side of the glass wafer that is uncovered by the masking layer. Dry etching was performed on an ICP system (Adixen) using  $\text{SF}_6$ ,  $\text{CHF}_3$ ,  $\text{CH}_4$  gases.

### 3. WET ETCHING OF PYREX GLASS

#### 3.1 Etch rate

An important factor in the deep wet etching of glass is the etch rate. In some cases of wet process, the selectivity of the etching is the preferred parameter of the process. In the wet etching of glass, some materials used as masking layers (mainly silicon and gold) are inert in the HF-based etchant. The etching process is limited by the defects of the masking layer and the penetration of the etchant through these defects. For this reason, a fast etch rate of glass will lead to a deeper etching, while the defect generation will be maintained at the same rate each time.

The main solution used for glass etching is based on HF. The etch rate is characteristic for each type of glass, especially due to the different oxides and compositions used during fabrication. The etch rate is determined by the concentration of HF etchants. To achieve a high etch rate, a standard (maxim) concentration of 49% should be used. Figure 1 presents the influence of HF concentration on the etch rate for Corning 7740 Pyrex glass. It should be noted that by increasing the HF concentration from 40% to 49%, a rapid increase of 50-60% of the etch rate can be achieved (4.4  $\mu\text{m}/\text{min}$  to 7.6  $\mu\text{m}/\text{min}$  for non-annealed glass). The annealing process has a strong influence on the etch rate of glass. Each type of glass has its optimum annealing point. The annealing influence is also presented in Figure 1. A similar variation was noted, but the increase in the etch rate was from 9.1  $\mu\text{m}/\text{min}$  to 14.3  $\mu\text{m}/\text{min}$  when the HF concentration was increased from 40% to 49%. We can conclude that annealing is an important parameter process not only for the reduction of the internal stress, but also for increasing the etch rate.

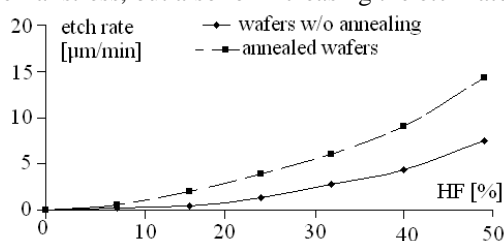


Fig. 1. Influence of HF concentration on glass etch rate

Other methods used, for increasing the etch rate were: warming the solution to 40-50°C and using ultrasonic for agitation. The first method was tested in a sealed Teflon container that was warmed with hot water at the above-mentioned temperature. The increase of the etch rate was significant (about twice). However, this method is not recommended for safety reasons. By applying ultrasonic agitation, we also noticed an increase of the etch rate, but the resistance of the masking layer in the etchant is drastically reduced.

#### 3.2 Masking layers

The main problems of wet etching are the pinholes and notching defects on the edges. These could be observed after a certain etch time, and were the result of the interaction between the etchant and mask. These defects presented in Fig. 2 limit the etch depth of glass. We will present in this chapter an analysis of the main masking layer that can be used for the wet etching of glass. The glass etchant that was used is HF 49%.

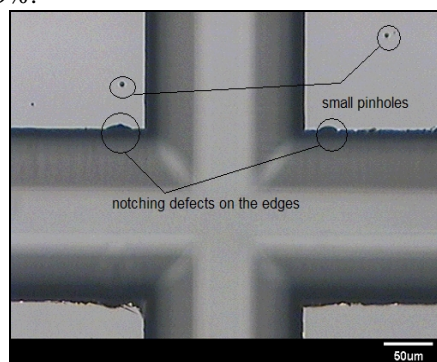


Fig. 2. Optical image of 100- $\mu\text{m}$  deep channels etched in glass with Cr/Au mask

**Photoresist masking layer.** Photoresist is mostly used for silicon oxide etching in diluted HF solutions (known widely as BOE). For our experiment, we used positive photoresist AZ7220 (from Clariant). In highly concentrated HF solutions, the quality of the photoresist mask was very poor. The maximum etching time – appreciated to be around 3 minutes (equivalent with a depth etch of 22  $\mu\text{m}$  on non-annealed wafers) – was achieved after the photoresist was hard-backed at 120°C for 30 minutes on a hot plate. A huge isotropy was noted (5:1). After etching for a long time, the photoresist mask would peel off. The technique could be used in cases where up to 20  $\mu\text{m}$  deep etching is required (capillary electrophoresis or packaging at wafer level).

**Amorphous silicon.** Silicon is an inert material in HF-based solutions. It also has the advantage of being a hydrophobic material. Hence, the penetration of etchant through the small impurities of the mask is relatively difficult. The amorphous silicon masking layer presents the advantage of deposition at low temperatures (almost room temperature for sputtering and 300°C for PECVD deposition), but as we analyzed in [12], the high value of compressive stress induced in this layer (400-600 MPa) limited its application to 15-20 minutes. The annealing of the masking layer could reduce the value of the stress and could improve the performance to up to 30 minutes – equivalent of 200  $\mu\text{m}$  [12]. The isotropy of the etching was 1:1.2. The influence of stress is presented in Figure 3, where wet etching of glass was performed using the same amorphous silicon mask, but this was annealed at 400°C at different times,

resulting in a different residual stress in the masking layer (600 MPa compressive to 100 MPa tensile).

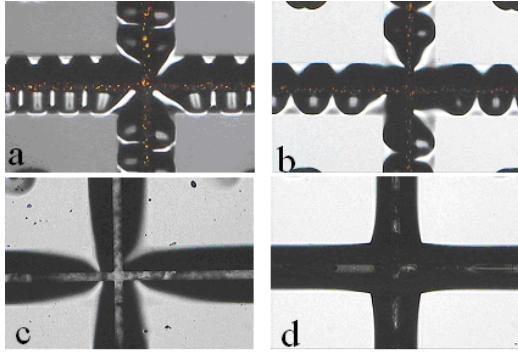


Fig. 3. Optical image with intersection of two microchannels etched in glass for 20 minutes (approx. 150  $\mu\text{m}$  in depth) in HF49% solution using amorphous silicon mask with different stress values: a) 600MPa b) 300 MPa c) 100 MPa d) 100MPa (tensile)

**Polysilicon.** The test layer was deposited at 530°C in a furnace. The resulting stress in the layer was 50 MPa compressive. The resistance of the mask in HF solution was 30-35 minutes (similar to results using low-stress amorphous silicon). The isotropy of the etching was very good – 1:1.

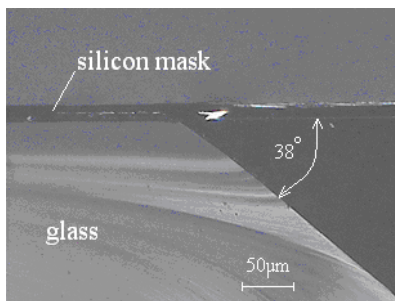


Fig. 4. Etching results with bulk silicon mask.

**Bulk silicon layer.** Single crystal silicon can also be used as a mask for glass etching. Wet etching with bulk silicon mask was first reported by Corman *et al* in [14]. In tests, a silicon wafer was anodically bonded on a glass wafer on an EVG 601 bonding system. The silicon wafer was thinned up to 30  $\mu\text{m}$  in an Adixen ICP-Deep RIE system. After patterning with photoresist, the mask was defined in the silicon layer using a classical Bosch process. The etching result indicated that the mask was perfectly inert in HF solution, but a huge isotropy of the etching process was observed. Figure 4 presents the results of wet etching in HF 49% solution of a Pyrex glass using a bulk silicon mask of 30  $\mu\text{m}$ . The resulting angle between the mask and glass surface (38°) indicated that the interface layer was removed quickly. The main reason for this could be the poor quality of the silicon oxide interface layer (between the silicon mask and glass wafer), which presented an increased etching rate. Similar results had been reported in [14].

**Cr/Cu.** The first reported result of etching with the Cr/Cu (50 nm/ 1 $\mu\text{m}$ ) masking layer is presented in [12]. The maximal time for a good quality etching process was around 15 minutes (about 100  $\mu\text{m}$  depth etch). The low value of residual stress of the Cr/Cu layer (50-80 MPa tensile) and the good selectivity of Cu in the HF etchant can make this layer very suitable for microfluidics applications, where the required depth is below 100  $\mu\text{m}$ . If the photoresist mask (the same AZ7220 from Clariant) used for Cr/Cu layer patterning is hard baked and kept for the glass wet etching process, the etching results can be improved sensitively.

**Cr/Au.** One of the most commonly used metal masks is Cr/Au because Au is an inert material in HF solutions. The best results initially obtained with the Cr/Au masking layer were in the range of 50-100  $\mu\text{m}$  depth [14] (7-15 minutes), as a function of the layer thickness. The mechanism of defect generation is very simple: due to the tensile stress in the deposited layer (250-300 MPa [14]), the masking layer crept and a large number of defects were generated in the mask. The mask surface was hydrophilic. Therefore, once the etchant solution was in contact with the mask, it would penetrate easily, to mask defects and to generate the pinhole. To minimize the effect of these cracks in the thick Au layer, a series of deposition/ cooling actions can be applied. After depositing 200-250 nm of gold, the deposition was stopped for 10 minutes. The temperature of the wafer would change and possible cracks were generated. The deposition process would then continue. The possibility of generating defects in the same position was reduced when the next layer of Au was deposited. This method of deposition generates a 1.2- $\mu\text{m}$  thick Au layer, and the etching time can be increased to 45 minutes. If the photoresist mask used for Cr/Au mask patterning is hard baked, the performance of the masking layer can also be improved. The photoresist will penetrate and fill the cracks generated by the tensile stress in the Cr/Au layer. Furthermore, the hard baked photoresist surface will make the mask surface hydrophobic. During etching, the photoresist is peeled off from the Cr/Au surface by the HF etchant. The photoresist inside these cracks, however, was removed very slowly due to its small contact surface with the etchant, or the increased adhesion forces on the channel walls of the cracks. Our experience indicated that the coating of the hard baked photoresist mask over the Cr/Au layer could improve the resistance of the mask in the etchant for more than 15-20 minutes. The improvement in the etching process when the thickness of the mask was increased was also reported in [14]. In their experiment, a double deposition of Cr/Au (60nm/ 400nm) and photoresist SPR220-7 was used. They attribute the improvement of the process to the covering of the small defects of the masking layer.



Figure 5 presents a hole with a diameter of 700  $\mu\text{m}$  that was etched through a 500  $\mu\text{m}$  Pyrex glass wafer Corning 7740 (annealed). The etching was performed in a Teflon beaker in the same HF solution, with magnetic stirring for 45 minutes. No defect was observed after the removal of the Cr/Au mask.

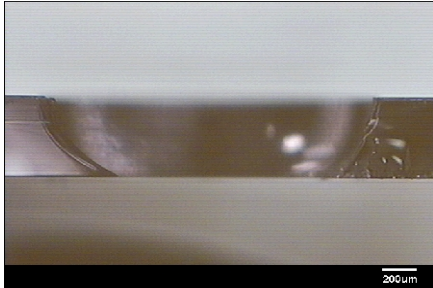


Fig. 5. Cross-section view of the through-etched hole with a Cr/Au/photoresist mask for an annealed glass.

#### 4. SURFACE ROUGHNESS

The roughness of generated surface can be an important issue for the wet polishing and deep wet etching of channels. Figure 6 shows the variation of roughness for Corning 7740 versus time for HF solution and when HCl was added (HF/HCl 10:1) solutions. The graph is almost linear for both solutions but with small values for HF/HCl solution. The purpose of HCl was to remove the insoluble products.

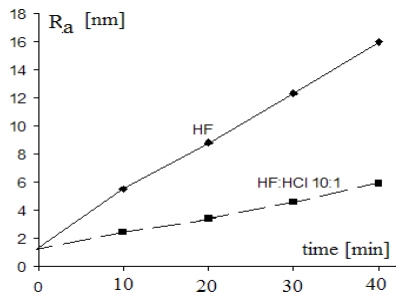


Fig. 6. Improving of surface roughness using HF/HCl solution

#### 5. DEEP DRY ETCHING OF PYREX GLASS

Previous work reported the etching of Pyrex glass using  $\text{SF}_6$  and electroplated Ni as the mask [6]. In our experiment we used a Fluorine gas  $\text{C}_4\text{F}_8$  as the gas etchant. The main advantage of using this gas is the presence of the generated plasma carbon-based radicals that can passivate the trench's walls and result in a profile with vertical walls. The experiments were performed on an Adixen Deep RIE ICP (oxide etcher). Other critical parameters were the pressure (we performed our experiments at 0.5 Pa) and coil power (we use the maximal RF power 2800W). We tested our experiment Al (6 $\mu\text{m}$ ) and bulk Si (40  $\mu\text{m}$ ) masks. For the Al mask, a selectivity of 1/10 was achieved, but after long processing (1

hour) we observed that the protected surface (after the mask removal) became rough and mate due to the ion bombardment. For this reason, we looked for a material that could be easily deposited and patterned in the thick layer: bulk silicon. Even though the selectivity was relatively similar (1:15), this masking layer presented some important advantages: its ability to work with a thick layer (30-100  $\mu\text{m}$ ), good patterning (vertical walls) using classical Bosch process in Deep RIE systems and easy removal in KOH solutions. The results of the etching of 80  $\mu\text{m}$ -tall glass pillars using a 40- $\mu\text{m}$  bulk silicon mask is presented in Figure 7.

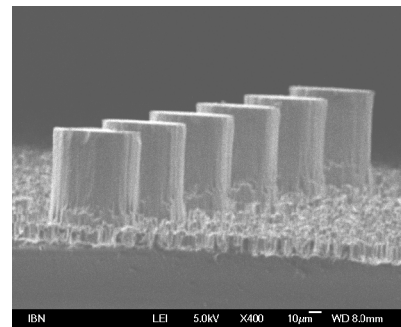


Fig. 7. Glass pillars etch in Deep RIE system using  $\text{C}_4\text{F}_8$ .

#### 6. CONCLUSION

This paper analyzes the main factors that affect the wet etching process of glass in HF-based solution. Our results show a deep wet glass etching of up to 500  $\mu\text{m}$ , using a Cr/Au mask and photoresist. The paper also reports a method to improve the quality of the generated surface using HF/HCl solution. A new method of dry etching of glass using bulk silicon mask and  $\text{C}_4\text{F}_8$  as etching gas is also reported.

#### REFERENCES

- [1] T Fujita, et al, *Sens. & Act. A* 82 (1-3), 198, 2000.
- [2] C Kim, Y Kim, , *J. Micromech. Microeng.* 12, 103, 2002.
- [3] C. Rusu, et al, *J. MEMS.* 10, 238, 2001.
- [4] PJ Obeid, et al, *Anal. Chem.* 75, 288, 2003.
- [5] C Iliescu, et al, *J. Micromech. Microeng.* 15/3, 494, 2005.
- [6] X Li, T Abe, M Esashi, *J. MEMS.* 1 (6), 625-630, 2002.
- [7] M Stjernström, J Roeraade, *J. Micromech. Microeng.* 8, 33, 1998.
- [8] A. Grosse, M Grewe and H Fouckhardt, *J. Micromech. Microeng.* 11, 257, 2001.
- [9] DCS Bien et al, *J. Micromech. Microeng.* 13, S34, 2003.
- [10] S Shoji, H Kikuchi, H Torigoe, *Sens. & Act. A* 64, 95, 1997.
- [11] M Bu, et al, *Sens. & Act. A* 115/2-3, 476, 2004.
- [12] C Iliescu, J Miao, FEH Tay, *Sens. & Act. A* 117/2, 286, 2005.
- [13] MA Grettilat, et al, *Sens. & Act. A* 60, 219, 1997.
- [14] T Corman, P Enokson, G Stemme, *J. Micromech. Microeng.* 8, 84, 1998.
- [15] C Iliescu, et al, *Surface and Coatings Technology (in press 2005).*