Department of Electronics and Electrical Engineering IIT Guwahati

EE206 Analog Circuits MidSem Date: 01/03/2022

Maximum Marks: 20 **Answer Submission Deadline: 01/03/2022 10.30 AM**

General Instructions

We would place the question paper in Moodle at 8.58 hrs on 01/03/2022 (Tuesday) and if you have not received the question paper by 9 AM, email roypaily@iitg.ac.in to resend it again. During the entire examination period, you must be logged in to the MS Teams through the link (will be active by 8.50 AM), and your video and audio must be ON throughout. Adjust the camera in such a way that your face, hands and answer scripts are always visible. You are not supposed to leave your seat during the examination. Therefore, take the bio-break, breakfast, etc., before starting the exam and adequately prepare yourself with sufficient pens, pencils, calculator, white sheets, etc., so that you do not need to leave the seat. This is NOT an open book exam and therefore, you will be disqualified if you refer any materials from your phone, laptop, notebook, textbooks, etc. If there is a power/internet failure and your video is off during the exam, we would evaluate your performance through an additional online viva (the schedule will be announced later). I hope you know that the written examination will be easier to score than the viva.

You may work out the problems on a sheet of paper, scan the handwritten answers, and finally submit the answers as a .pdf file in the Moodle EE206[2022], keeping the file size less than 5 MB. Your file name should be your_roll_number_MidSem (for example, 100102001_ MidSem.pdf).

Additional Marks for early completion

The paper is set such that an above-average student would finish in 40 minutes, including the time for scanning and uploading. If you submit the answer scripts within 40 minutes, 20% extra marks will be added to your obtained marks. If you submit the answer scripts within 50 minutes, 15% extra marks will be added to your obtained marks. If you submit the answer scripts within 60 minutes, 10% extra marks will be added to your obtained marks. We would use the Moodle submission time stamp for additional marks calculation. In any case, you may write the main points as quickly as possible to submit before the deadline, that is 01/03/2022 10.30 AM. Late submission with penalty is allowed until 10.40 AM; however, the maximum marks awarded will be reduced proportionately to every minute of late submission. Give precise answers to redeem the time. Notations have their usual meaning.

Question Paper

Problem - Design of a Common Gate Amplifier (CG)

Assume 180 nm technology node and V_{DD} = 1.8 V. The V_{tn} = 0.5 V and V_{tp} = - 0.5 V. The $\mu_n C_{ox}$ = 300 $\mu A/V^2$ and $\mu_p C_{ox}$ = 120 $\mu A/V^2$. Assume an early voltage of V_A = 5 V for 1 µm channel length for both NMOS and PMOS. Wherever needed, you must give the appropriate units to get maximum marks.

- You are supposed to design a common gate amplifier for a maximum figure of merit. The figure of merit is defined as FoM = Gain Bandwidth Product / [Power x Area of all transistors]. For the area calculation, you may consider only the total sum of the WL products of transistors only.

- The students are supposed to design each of their circuits for different voltage gains. The specific voltage gain for you will be the last three digits of your roll number.
- The input transistor (the main transistor where you give your input signal) must be PMOS, not NMOS.
- The input signal is about one millivolt peak to peak magnitude of a relatively lower frequency. Assume a Thevenin resistance of 50 Ω for your input voltage source.
- For the frequency analysis, assume that all internal nodes have a typical capacitance of the order of 1 pF, irrespective of the transistor sizes.
- You may assume that a golden current source of 12 μA is available for biasing purposes.

Marking Scheme

1. Draw the complete circuit diagram. Avoid all resistors (except the Rsensor = 50 Ω as given) instead use only transistors. Even the current sources (except the golden current source, I_{REF} = 12 μA) are to be replaced by their actual transistor circuit. [2 points]
2. For what application is this amplifier employed relative to other types? Why? [1 point]
3. Calculate the DC (Direct Current) through all the transistors (neglect channel length modulation for this step) [1 point]
4. Calculate the W and L sizes of all the transistors (neglect channel length modulation for this step) [2 points]
5. Calculate the trans-conductance, gm of all the transistors (neglect channel length modulation for this step) [1 point]
6. Calculate the small-signal resistance r_{ds} of all the transistors (use channel length modulation for this step) [1 point]
7. What is the DC bias at the output/input terminals of the main transistor (use channel length modulation for this step) [2 points]
8. Calculate the DC bias voltages needed at the gate terminal of all the transistors [1 point]
9. Estimate the power dissipation of this circuit [1 point]
10. Estimate the poles of this amplifier and the bandwidth of the circuit [2 points]
11. Estimate the FoM of this amplifier (as defined on the previous page, for this calculation, you may keep the bandwidth in MHz, transistor sizes in μm and the power dissipation in μW) [2 points]
12. As a designer, mention the steps you may take to improve the FoM further [1 point]