Cache: Snooping & Directory Based

Tuesday, April 5, 2022 7:24 AM

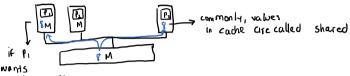
In many processor, we solve the redundance by applying Write-through and write-back, the same as with one processor.

The Update of cache memory is done using:

Shooping: used in shared memory with a bus

Directory - based: distributed memory

Example:



to change it.

School a msg through the bus to all p's that have the place. Then all p's change their state to invalid.

Pi then changed the value, with Modified state. If another processor wants it, it asks through the bus to update the value (everyone sees it). The modified state processor than updates RAM memory, and P2 also updates from RAM's new value.

 \rightarrow the problem is the bus: if $p \rightarrow \infty$, the bus is filled and the waiting time appears due to the bus

In the case of Distributed Mcm, the communication goes from device to device: RAM and cache communication is faster and thus no longur a bottleneck
Directory - based: every P has its own directory, used for the cache state.

Let's say p_2 has x_1 and p_1 wants it, it sends a message the x is them sent to p_1 s cache. Then, p_2 writes on its directory: x is shared with p_1 if another p_1 wants x, it travels to p_1 's cache p_2 's directory than updates the directory: x is shared to p_1 , p_2

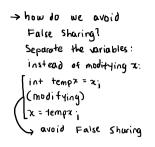


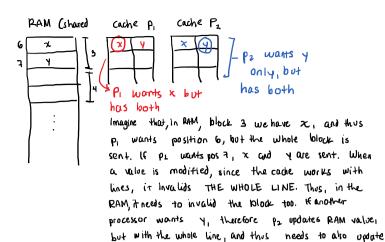
Imagine P, wants to modify x: sends a massage through the next to p_2 , so that p_2 invalidates all copies on its own RAM and (through a msg) invalidates all other p's in the directory. Once a p invalidates a value, it needs to send a msg that if can now proceed. In p_2 's directory; x is shared $p_1 p_0 \rightarrow \text{invalid}$. Thus, if another p wants it, p_2 sends a msg to p_1 (Correct value) so that p_1 sends the correct value, p_2 corrects if on its PAM and the directory; x in p_1 that in its directory; x in p_2 is p_3 in p_4 that p_4 is p_4 that p_4 is p_4 that p_4 in p_4 that p_4 is p_4 that p_4 that p_4 is p_4 that p_4 is p_4 that p_4 that p_4 is p_4 that p_4 that p_4 is p_4 that p_4 is p_4 that p_4 t

The other problem is : False Sharing

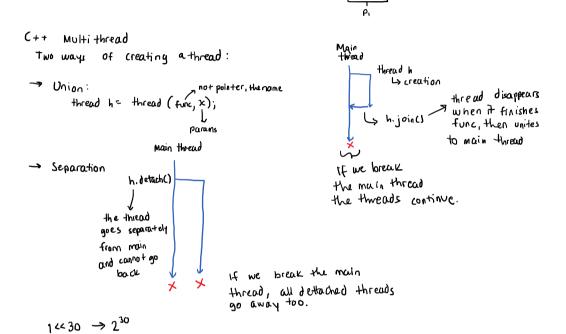
L> this does not happen in 1 processor It happens when we have a cache per processor

RAM (shared cache P, cache P2





x from another processor = performance becomes slow.



volatile S s; volatile since we do not want the compiler to optimize it (instead of the for loop, it just makes S = N), but we want it to execute the for