Lab 2 (27-09-2021)

Write the Verilog code and simulate using modelsim

1. Half adder (a) using gates (b) using dataflow model (using assign statement)
2. Full adder (a) using dataflow model (using assign statement) (b) using two half adders and an OR gate
3. Two to one multiplexer using behavioural model (using if statement)
4. 4 bit ripple carry adder using full adder modules
5. A four variable logic function that is equal to 1 if any three or all four of its variables are equal to 1 is called a majority function. Write a Verilog code that implements this majority function. Use the Boolean equation derived in Lab1 in assign statement

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Need to upload lab report in the following format in moodle at the end of the lab session as a PDF file

Question

Verilog code

Simulation waveform showing all the test inputs (as shown in the last figure of the intro _to_modelsim.pdf file)