Lab 6 (15-11-2021)

Design, Implement and simulate the following circuits in Logisim

1. Design a synchronous modulo-5 counter using D FF
2. Design a synchronous 4 bit up-down counter using JK FF
3. Design a circuit that generates the sequence 0-8-12-6-13-11-7-3-1-0 using DFF.
4. Design a Real time clock HRS:MIN:SEC using the counter available in the logisim library. Display the results using seven segment display. There should be provision to set the time (using load). *Optional* – Add provision for setting an alarm and displaying it

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Need to upload lab report in the following format in moodle at the end of the lab session as a PDF file

Question

Design and explanation required

Circuit diagram from logisim

Results obtained

U can upload a video for question 1 if you wish