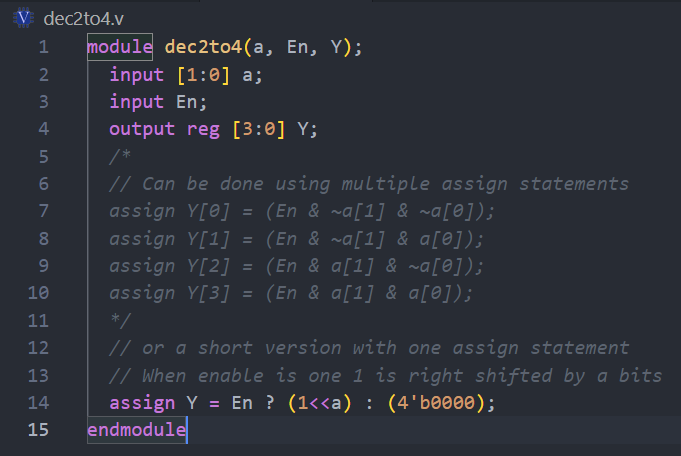


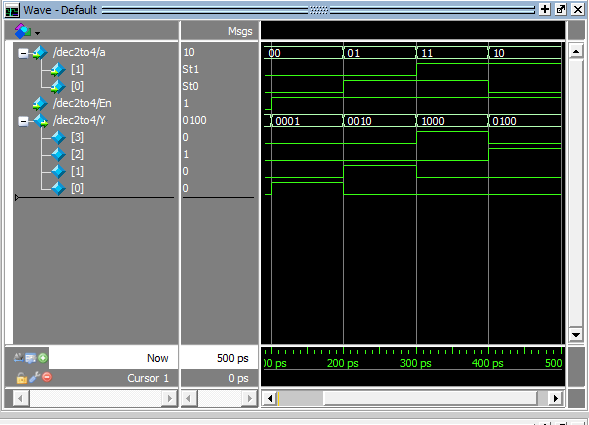
# 2 to 4 decoder using (a) concurrent signal assignment statements (b) case statement

## Solution:

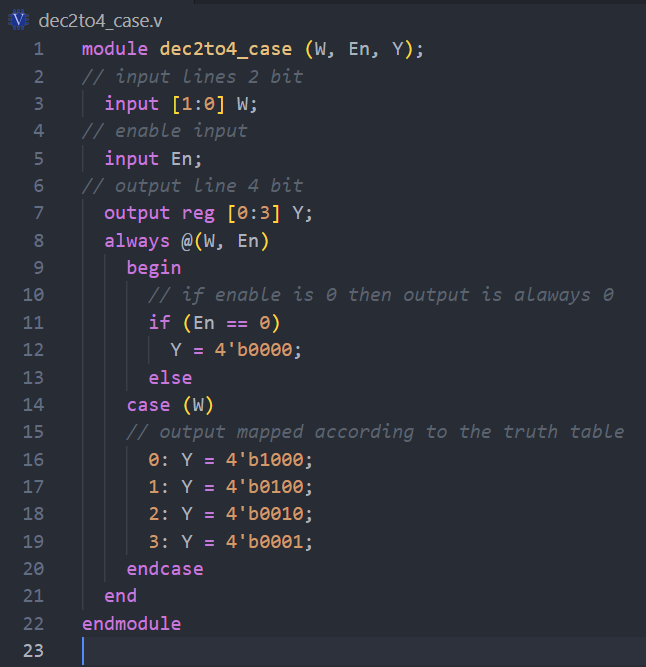
### Concurrent Signal assignments



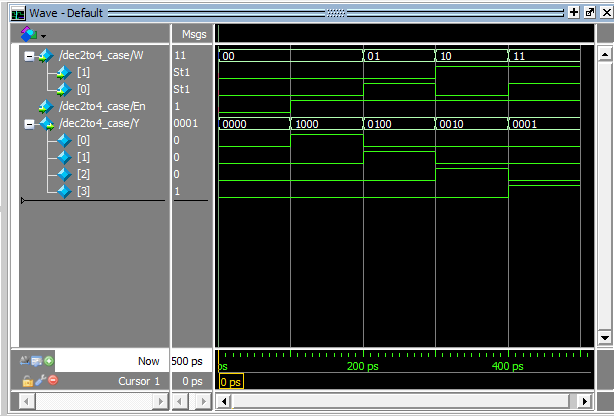
### Simulation waveform



### Case statements



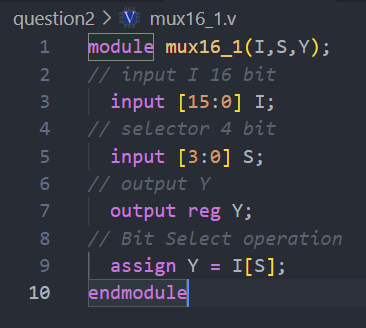
### Simulation waveform



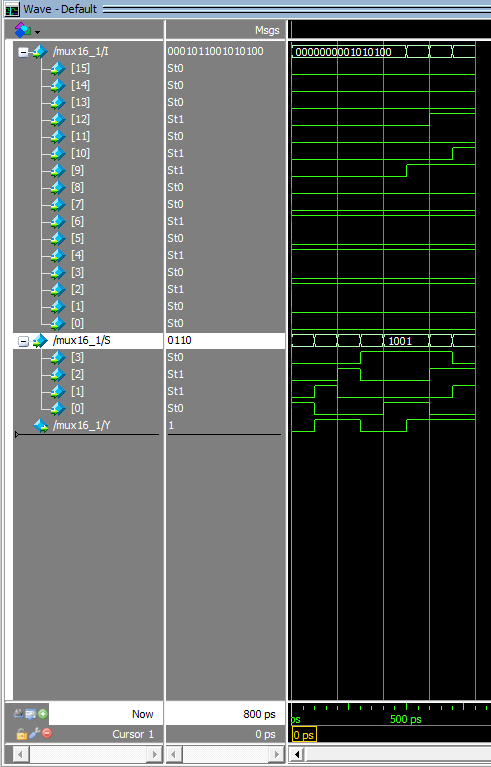
# 16:1 Mux

## Solution:

### Verilog code



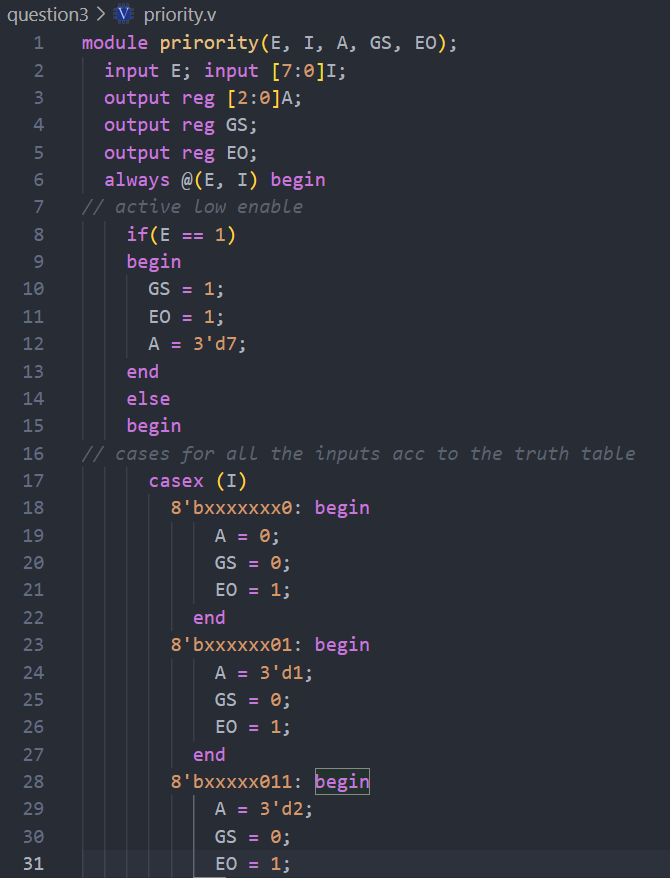
### Simulation



# Functionality of 74x148 priority encoder

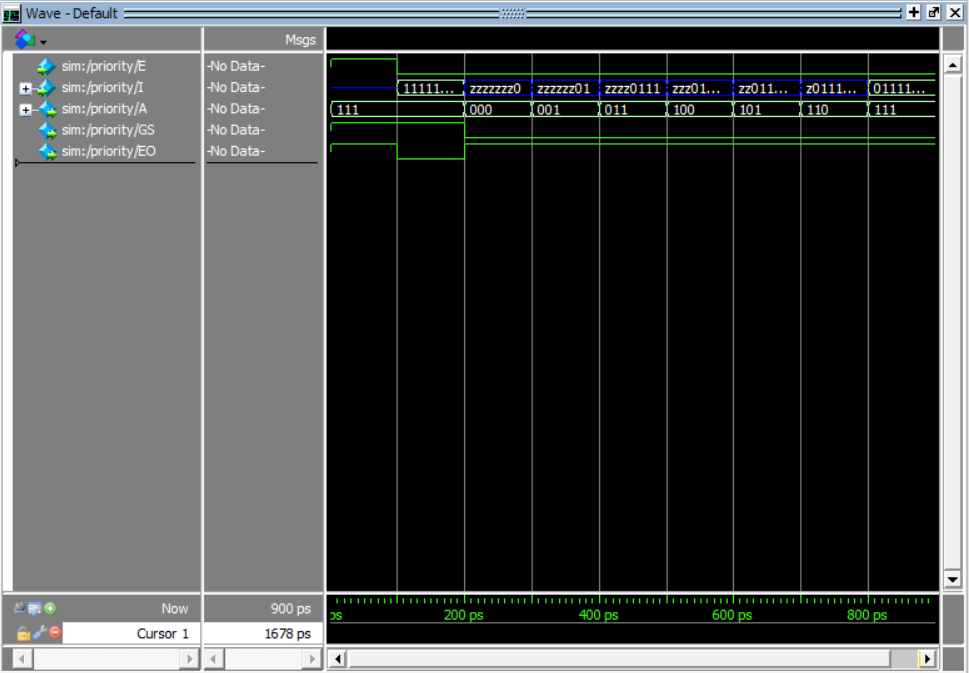
## Solution:

### Verilog code

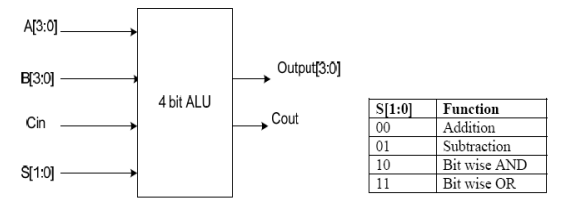


### 

### Simulation waveform

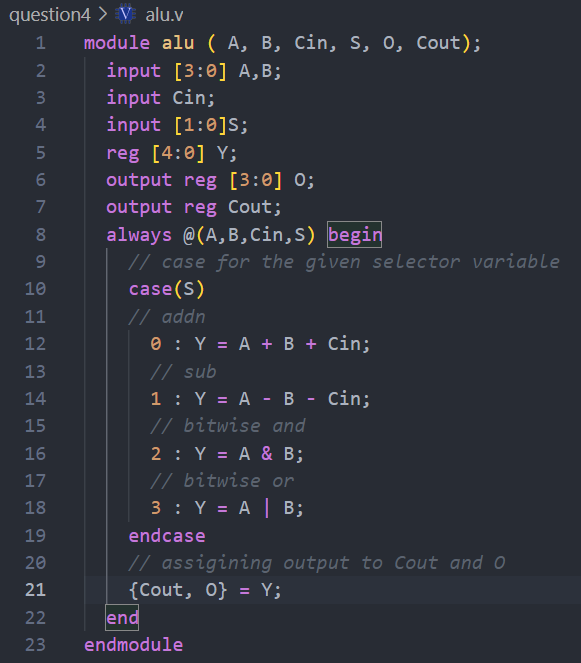


# ALU design

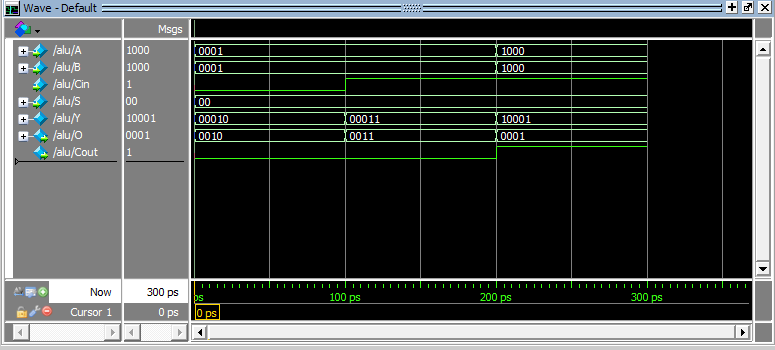


## Solution:

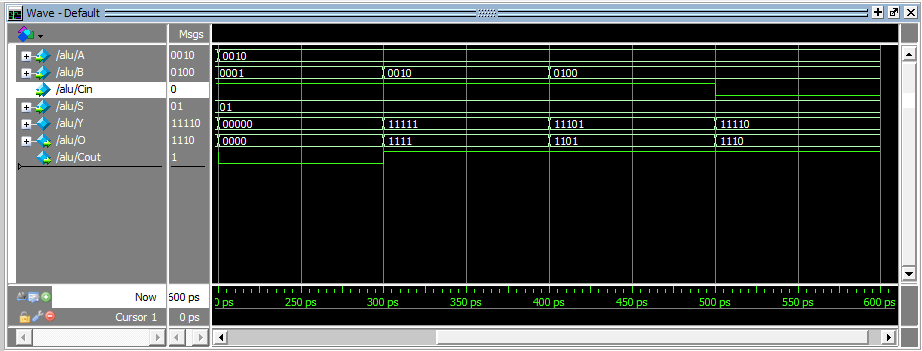
### Verilog code



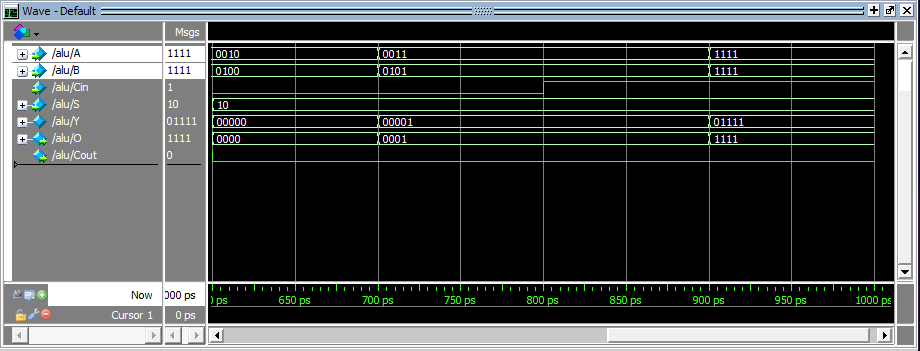
### Simulation waveform for S = 00



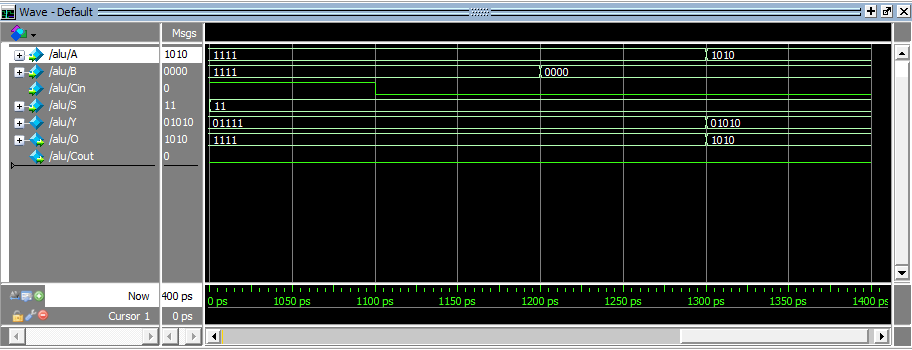
### Simulation waveform for S = 01



### Simulation waveform for S = 10



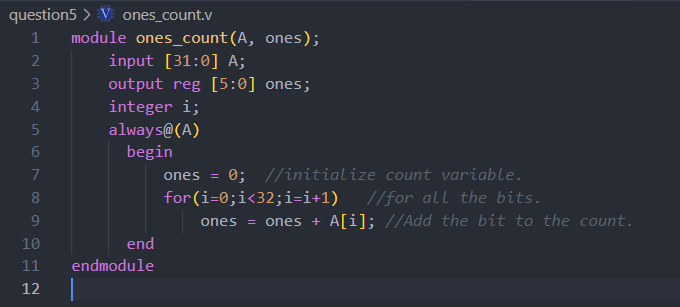
### Simulation waveform for S = 11



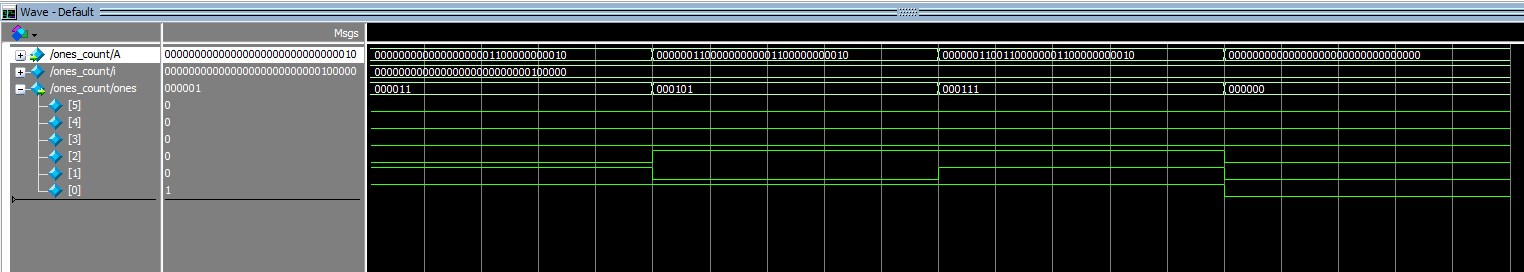
# Count number of 1s in a 32-bit number.

## Solution:

### Verilog code



### Simulation waveform

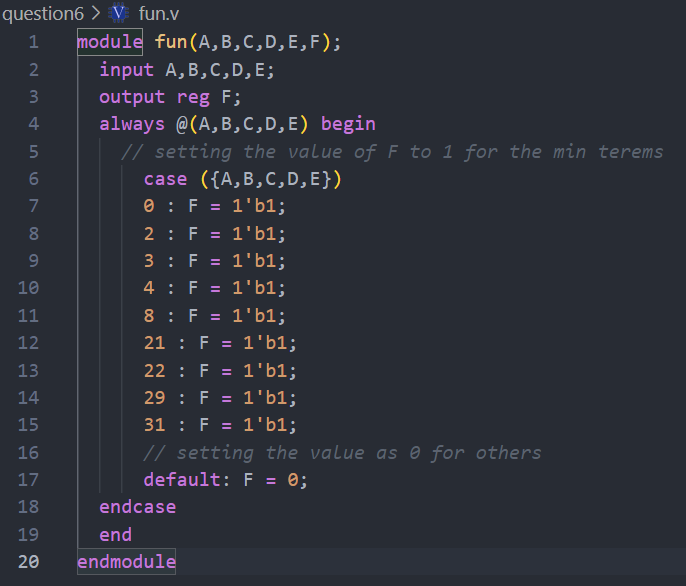


# Implement the following function

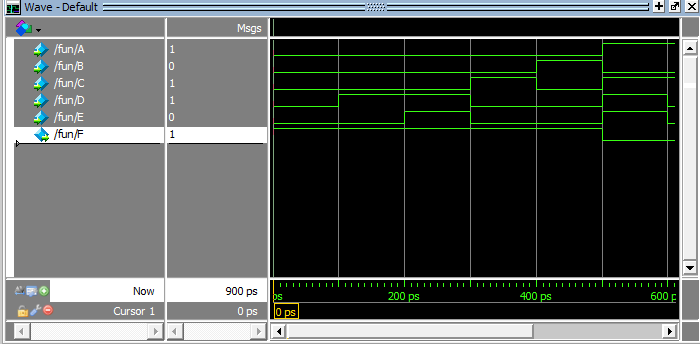


## Solution:

### Verilog code



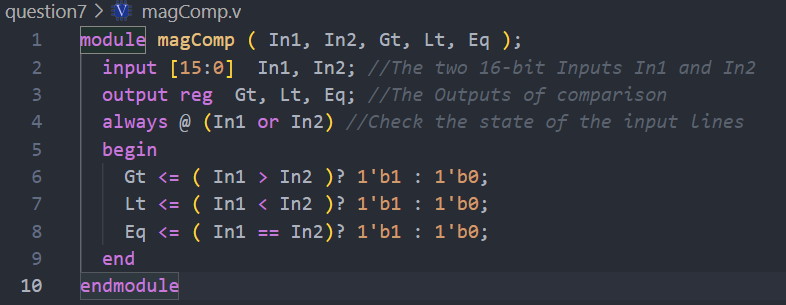
### Simulation waveform



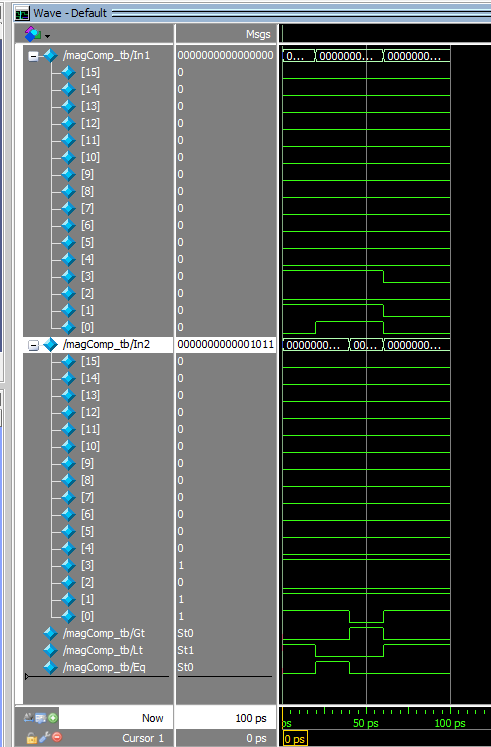
# 16-bit magnitude comparator.

## Solution:

### Verilog code



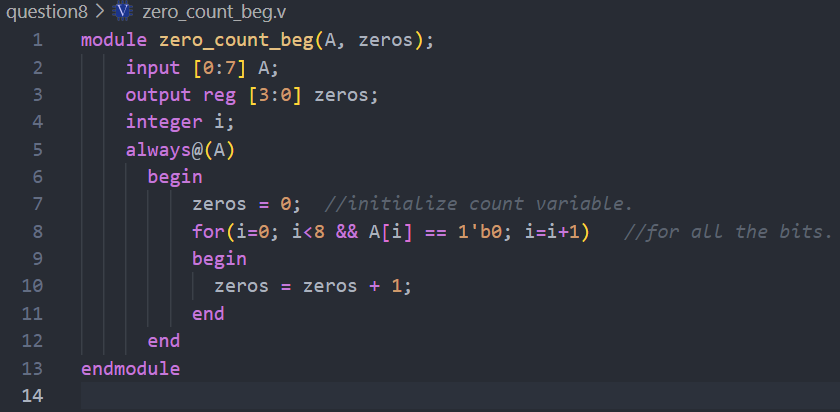
### Simulation waveform



# Count the number of leading 0’s in an 8-bit number.

## Solution:

### Verilog code



### Simulation waveform

