

# 1) Design a synchronous modulo-5 counter using D FF

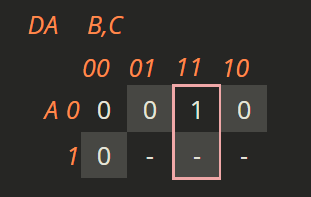
## Solution:

### Design and explanation

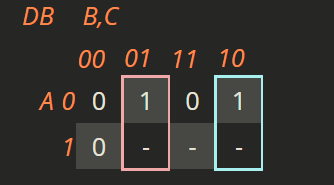
The counter design table for such counter shows the three flip-flop and their states also (0 to 5 states), as in table (a), the 6 inputs needed for the three flip-flops. The flip-flop inputs needed to step up the counter from the current to the next state have been worked out along with the assist of the excitation table illustrated in the table.

NOTE: A is the MSB and C is the LSB.

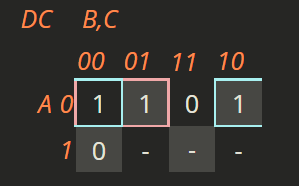




DA (A, B, C) = BC

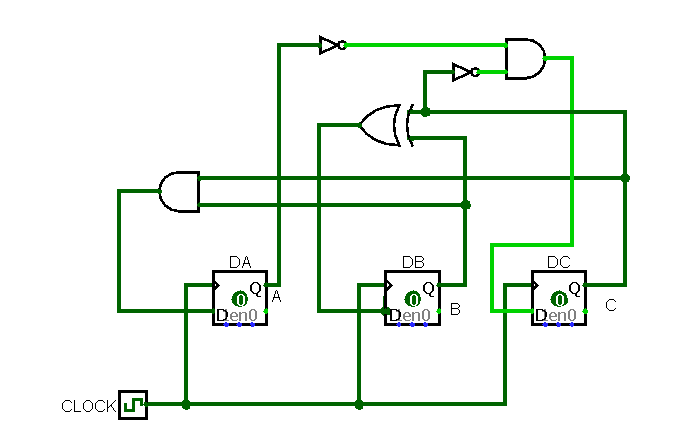


DB(A, B, C) = B'C + BC'



DC(A, B, C) = A'B' + A'C'

### CIRCUIT



### RESULT OBTAINED

VIDEO LINKED

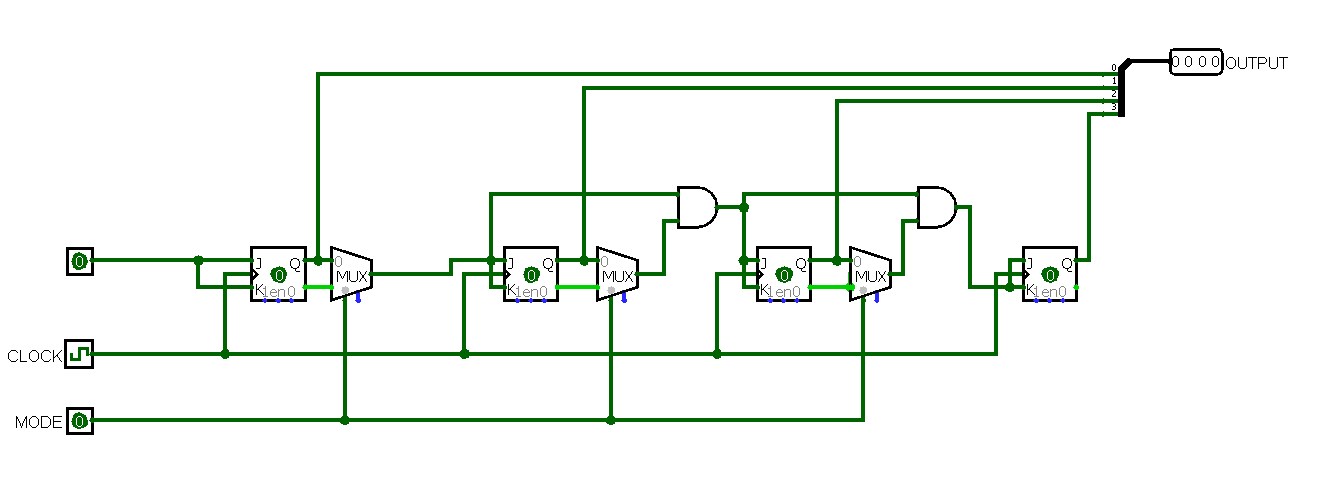
# 2) Design a synchronous 4 bit up-down counter using JK FF

## Solution:

### Design and explanation

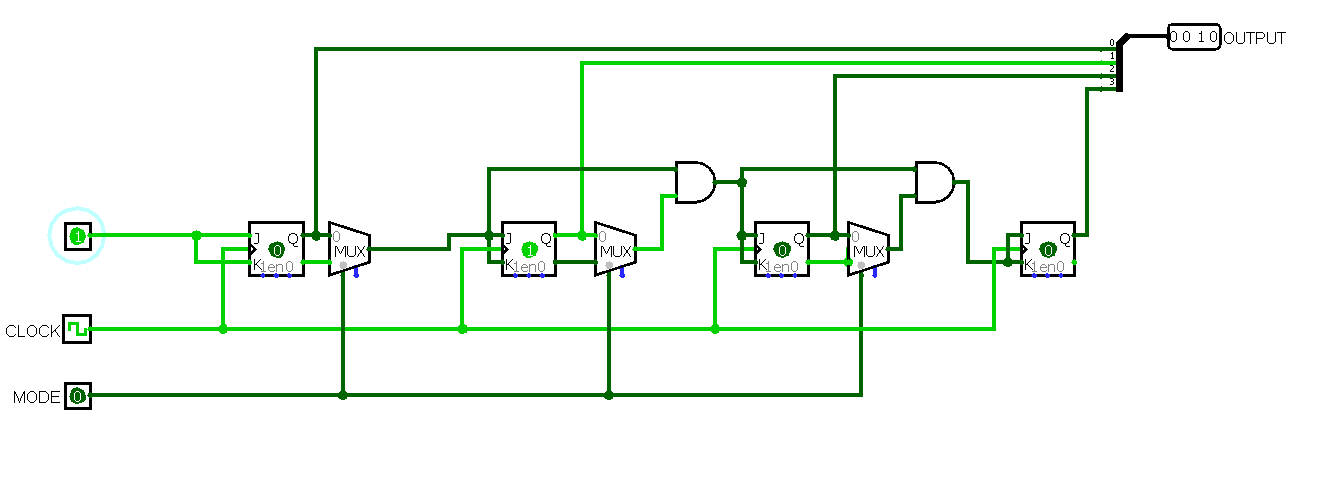
To design an up down counter we can use a Mode variable which when 0 does up counting and 1 does down counting. To perform down counting we just need to give the compliment of the clock to the next block, now the counter counts from backwards when Mode is equal to 1.

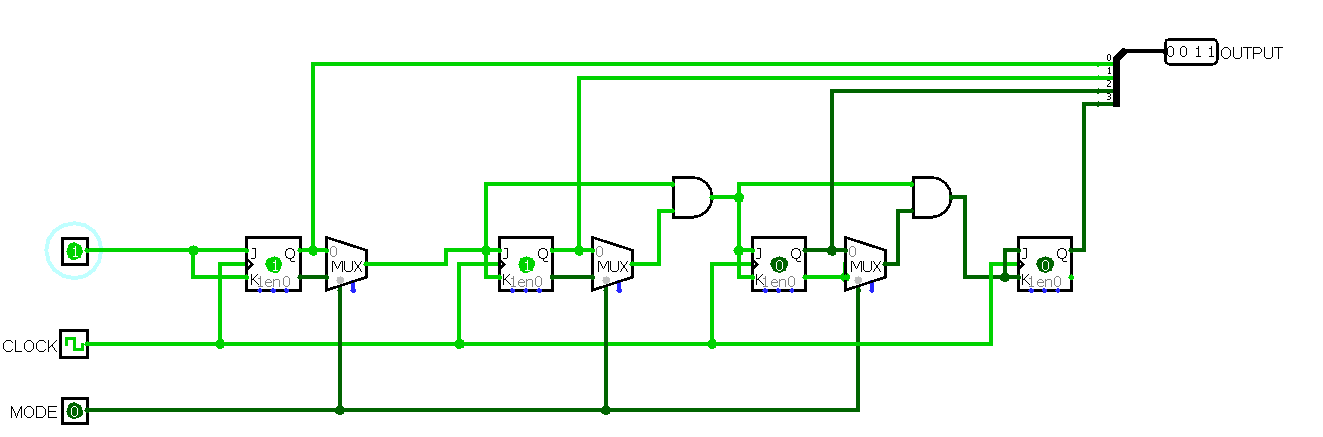
### CIRCUIT



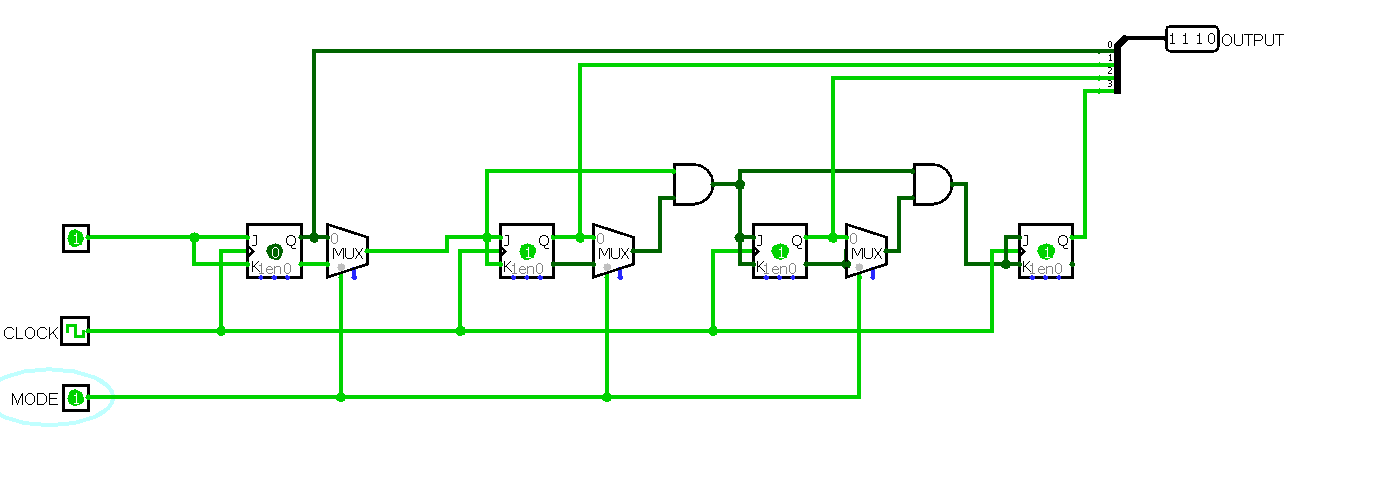
### RESULT OBTAINED

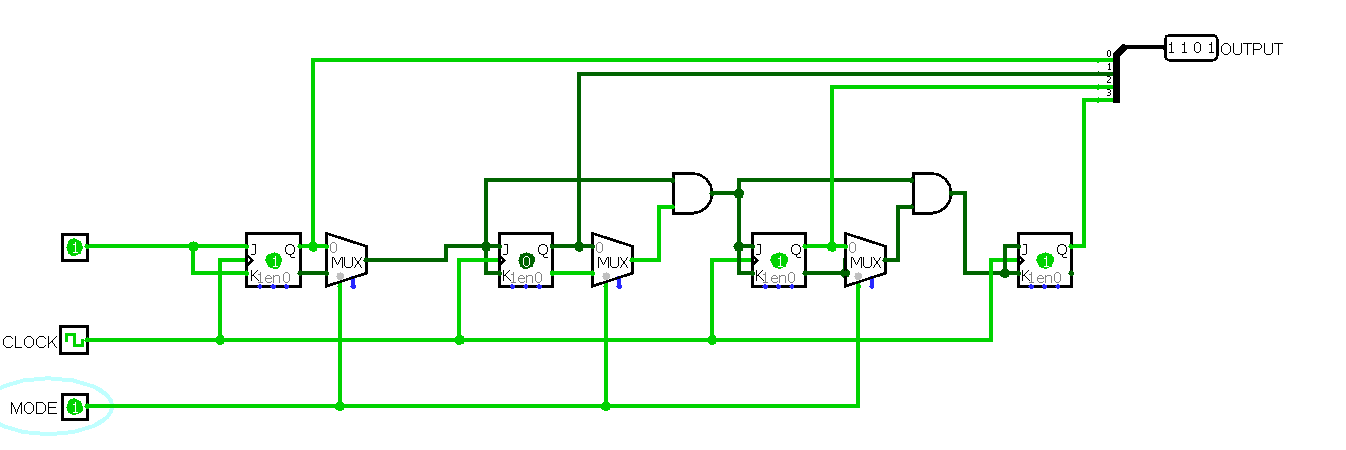
UP Count





Down Count





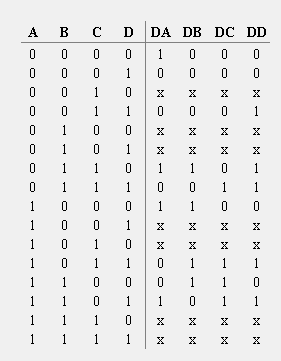
# 3) Design a circuit that generates the sequence 0-8-12-6-13-11-7-3-1-0 using DFF.

## Solution:

### Design and explanation

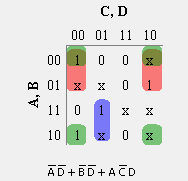
The sequence generator block diagram using a counter is illustrated below. Here, the combinational circuit is the next state decoder. The input of this state decoder can be obtained from the outputs of the FFs. Similarly, the outputs of this state decoder are given as inputs to the flip-flops. Based on the number of FFs, the required sequence like 0’s or 1’s can be generated.

**Characteristics table**

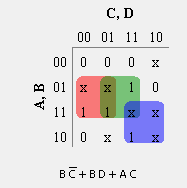
****

**Combinational logic expression**

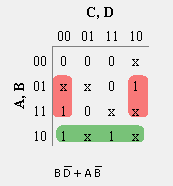
**DA**

****

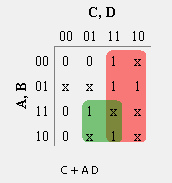
**DB**

****

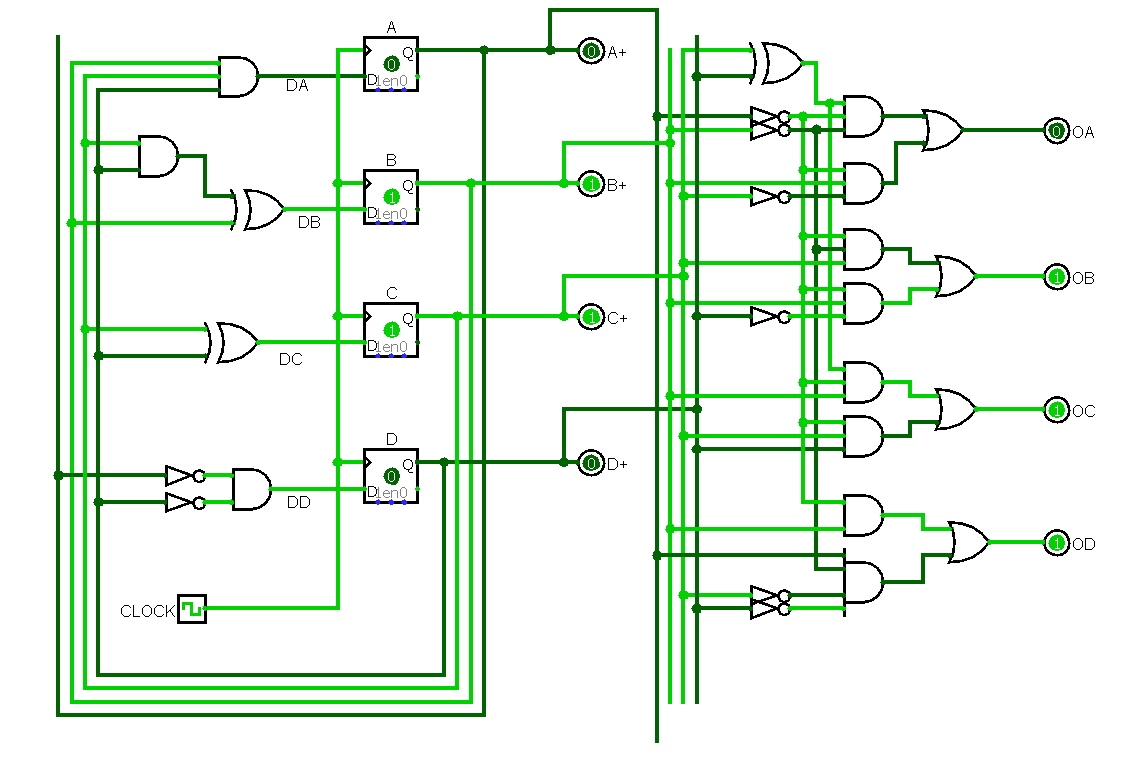
**DC**

****

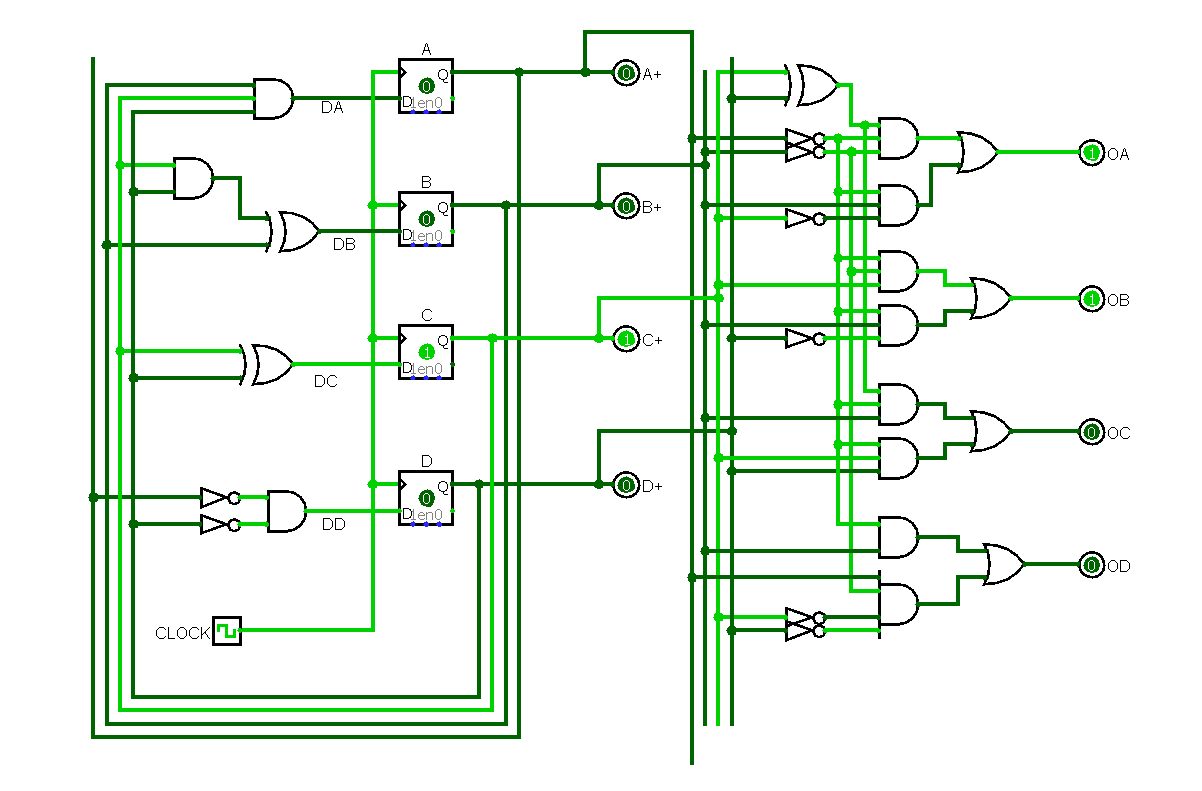
**DD**

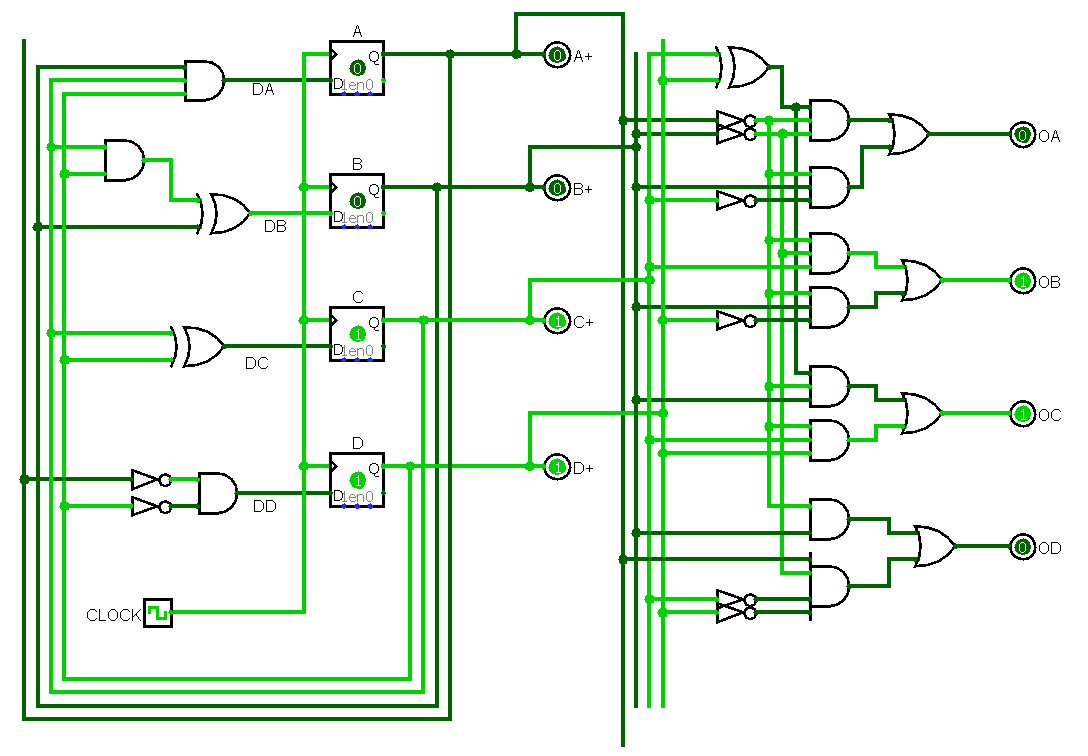
****

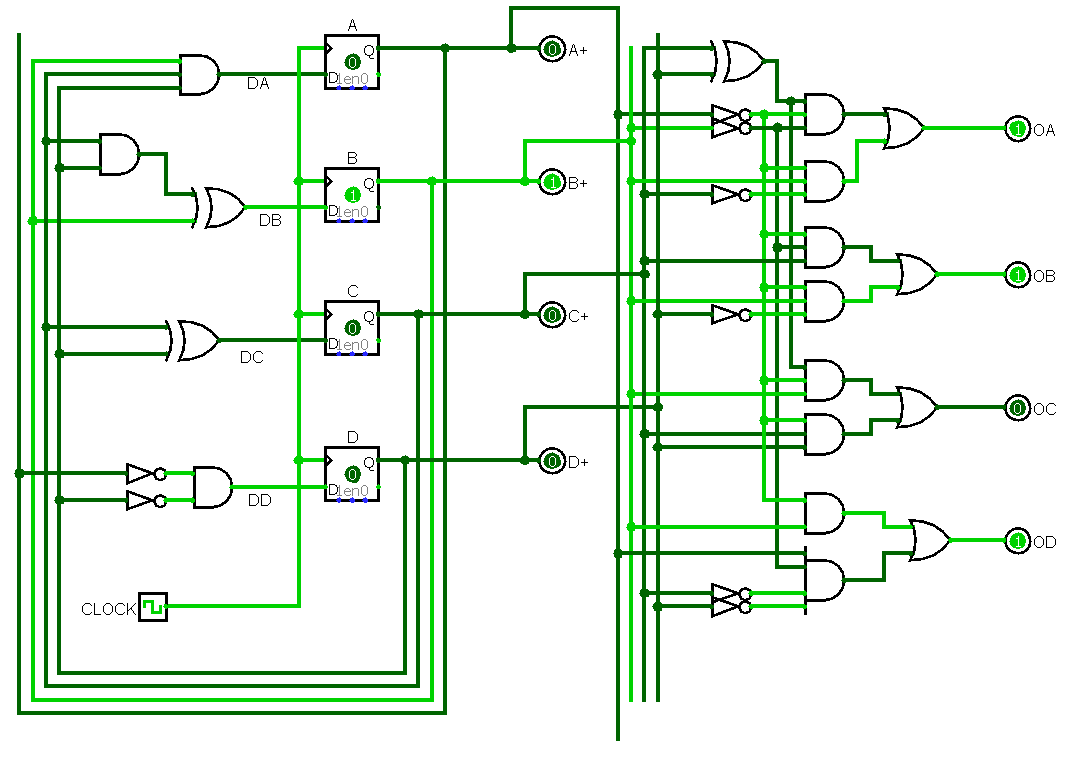
### CIRCUIT

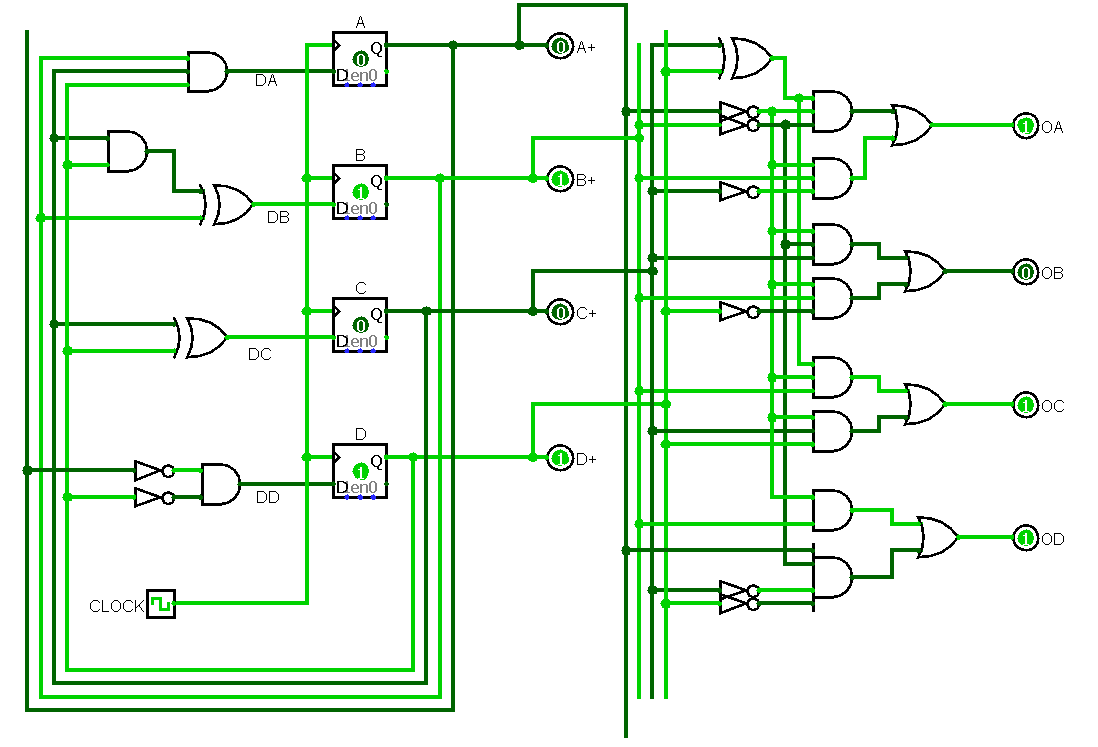


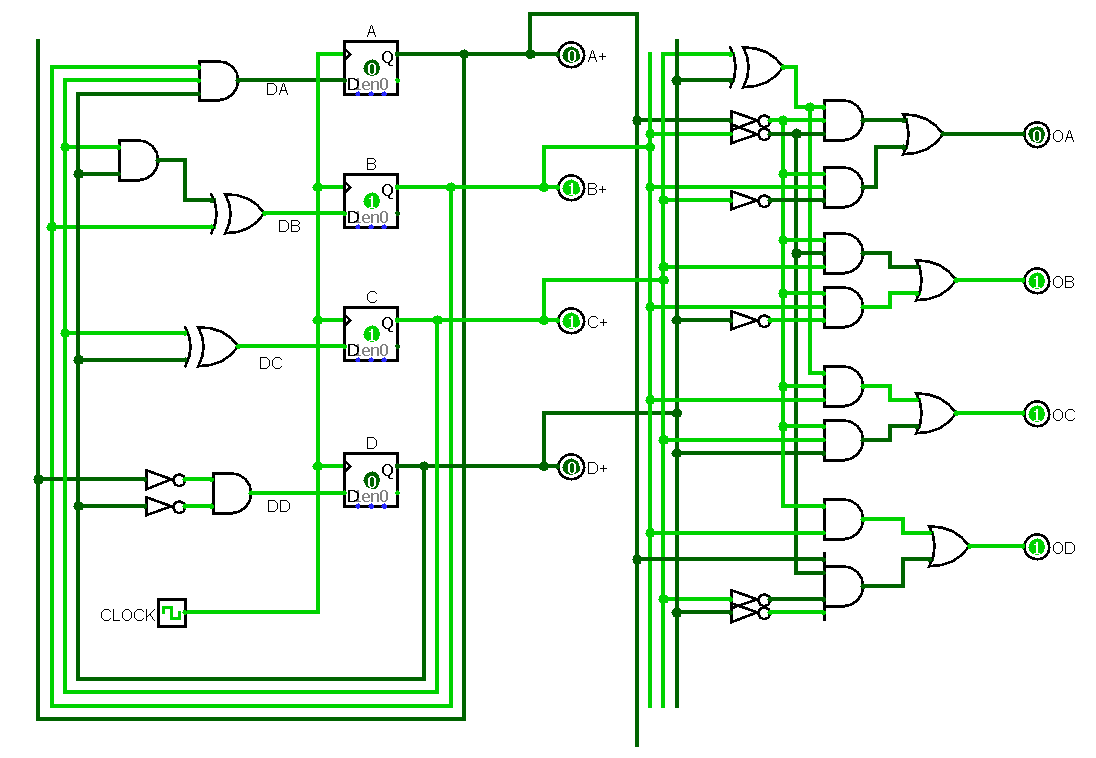
### RESULT OBTAINED











# 4) Design a Real time clock HRS: MIN:SEC using the counter available in the logisim library. Display the results using seven segment displays. There should be provision to set the time (using load). Optional – Add provision for setting an alarm and displaying it

## Solution:

### Design and explanation

### CIRCUIT

### RESULT OBTAINED