

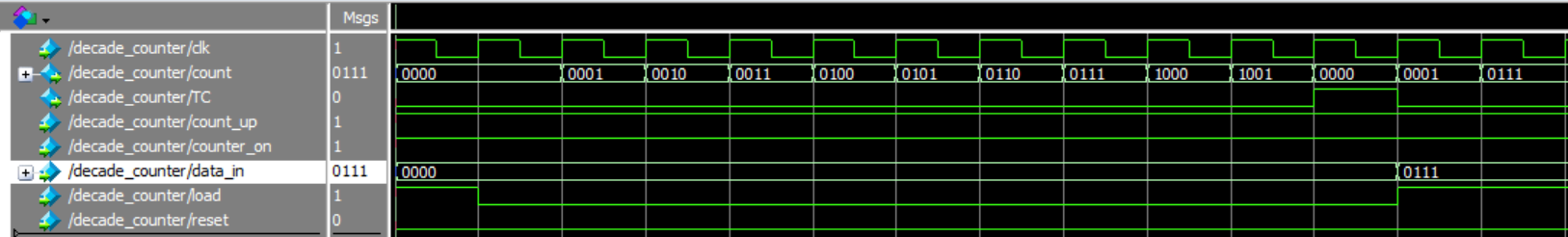
# Decade Counter

## Solution:

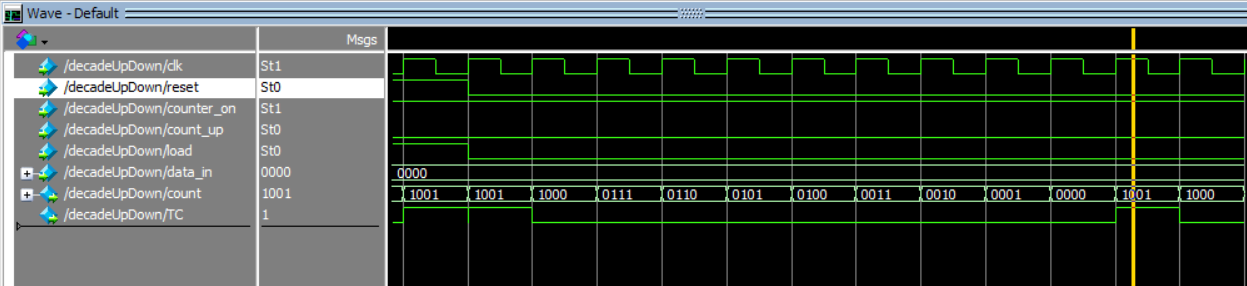
### Code



### Simulation waveform UP Count



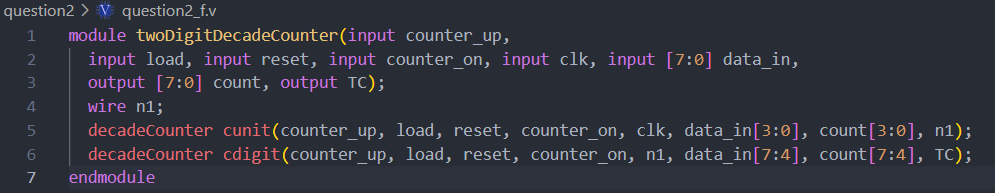
### Simulation waveform DOWN Count



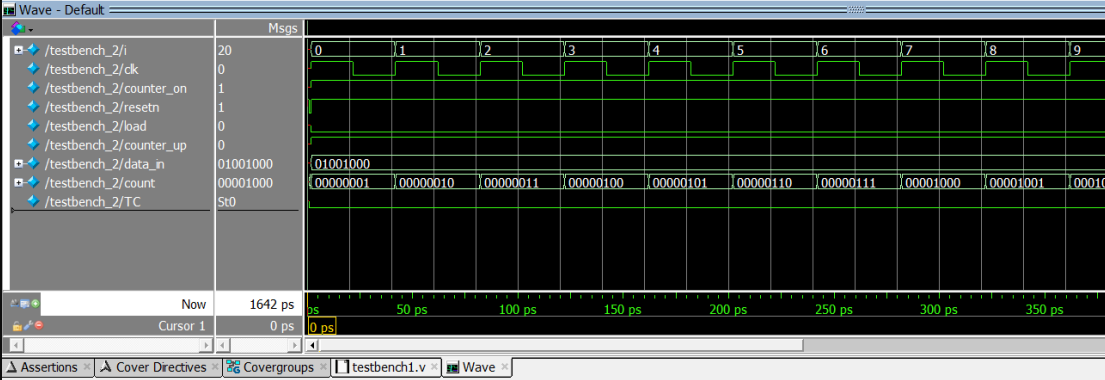
# Decimal up down counter

## Solution:

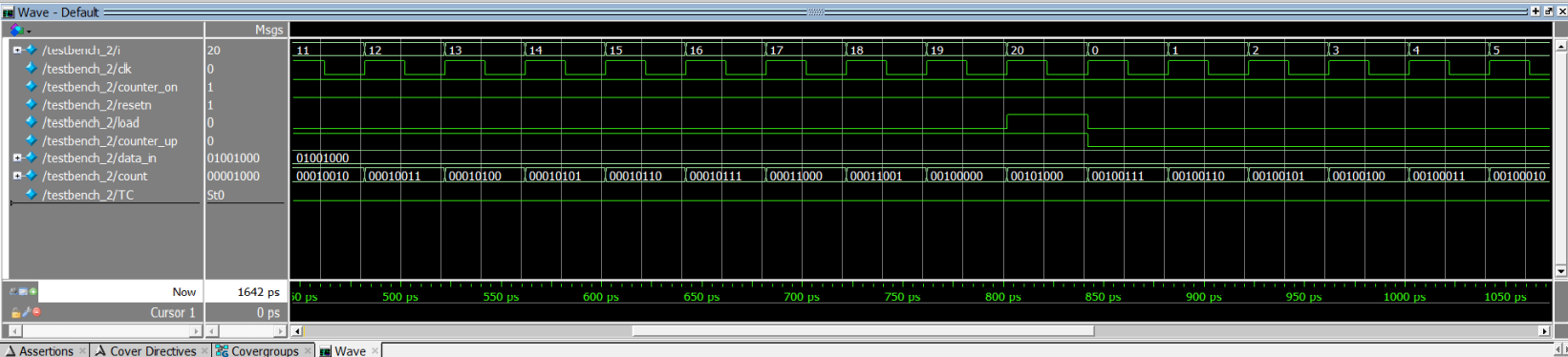
### Verilog code



### Simulation UP count



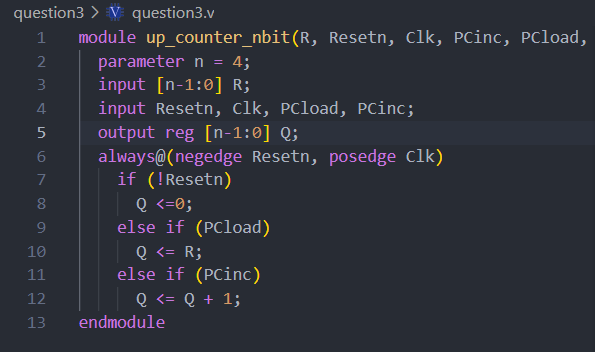
### Simulation DOWN count



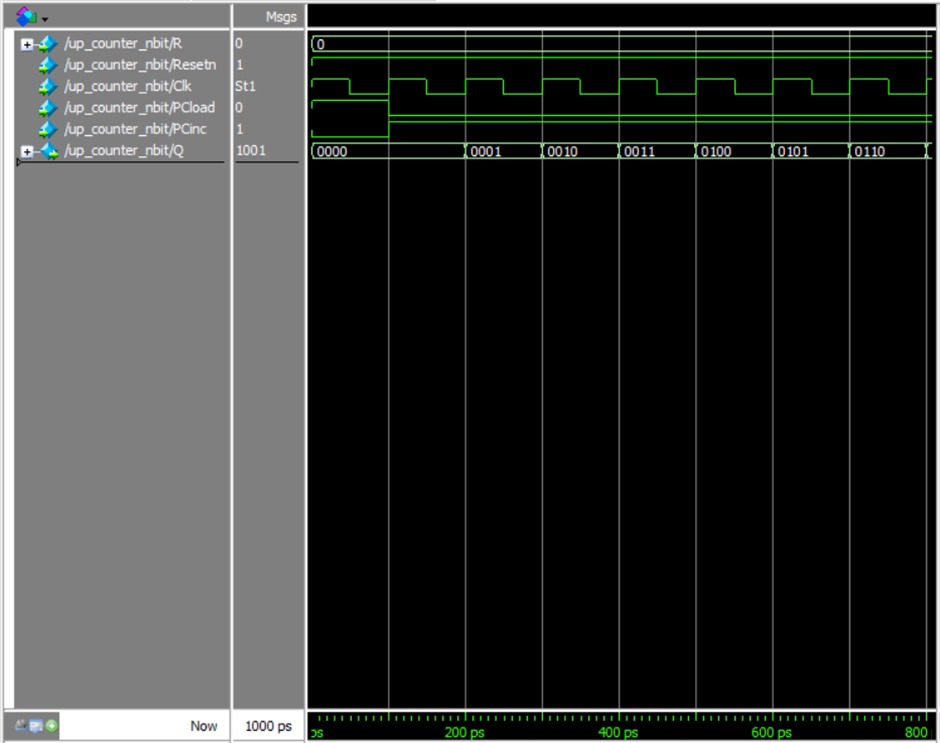
# N bit program counter

## Solution:

### Verilog code



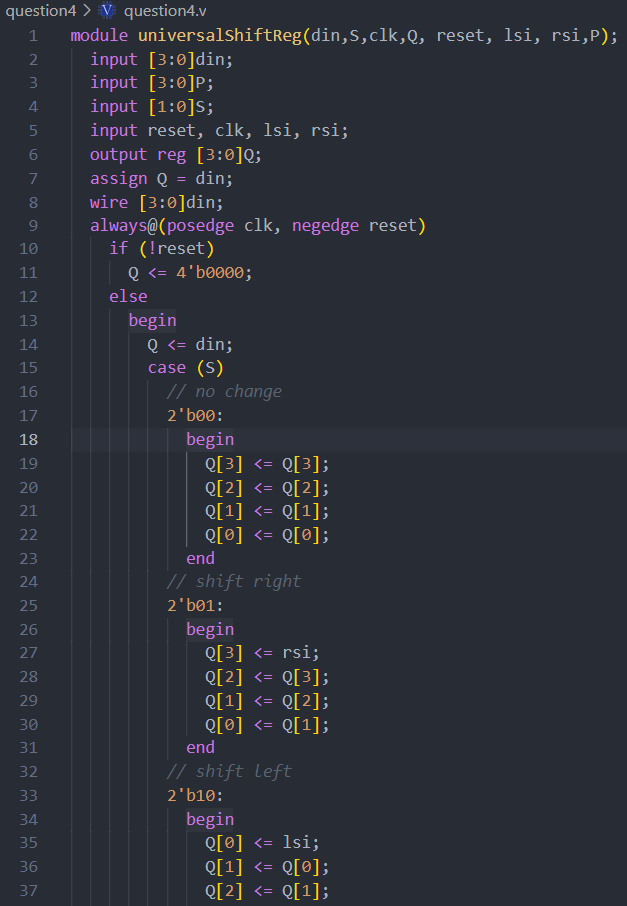
### Simulation waveform

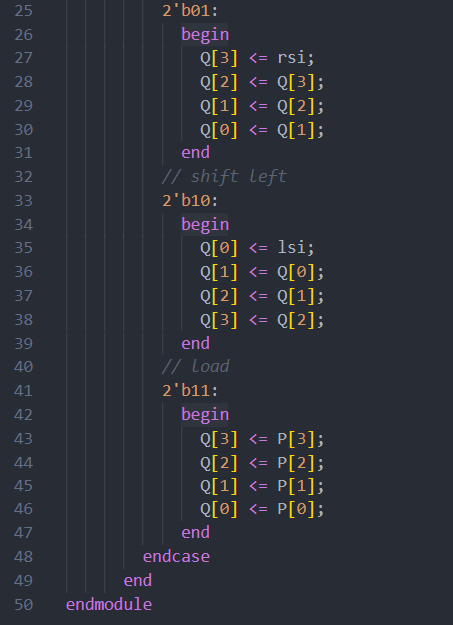


# Shift Register 74194

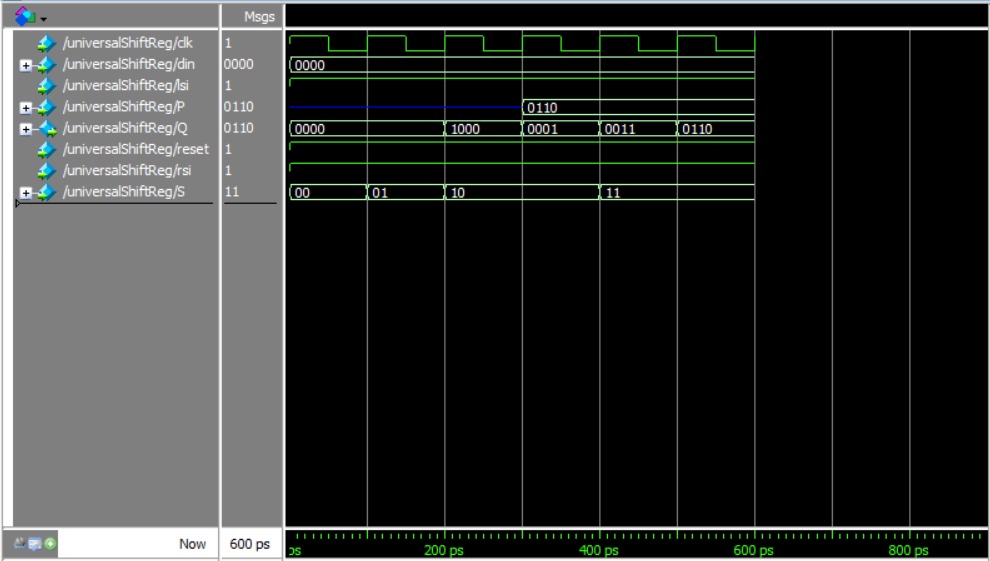
## Solution:

### Verilog code





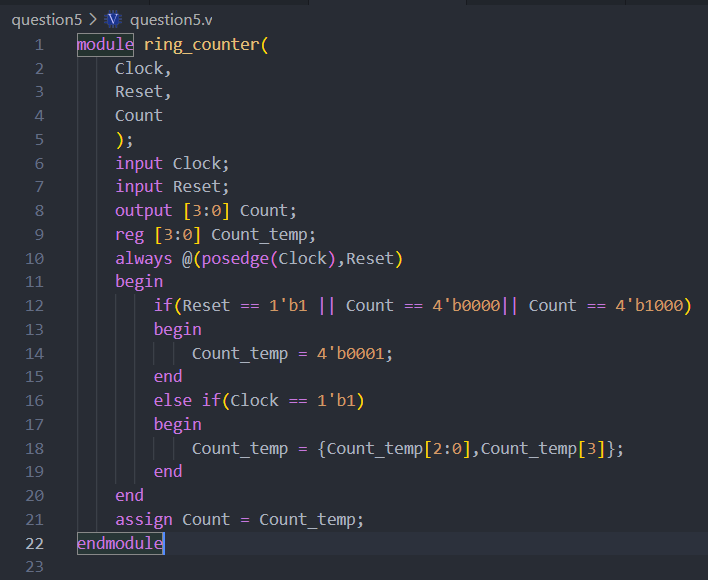
### Simulation waveform



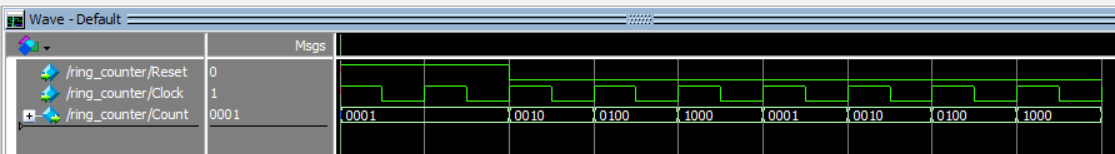
# Self-correction ring counter

## Solution:

### Verilog code



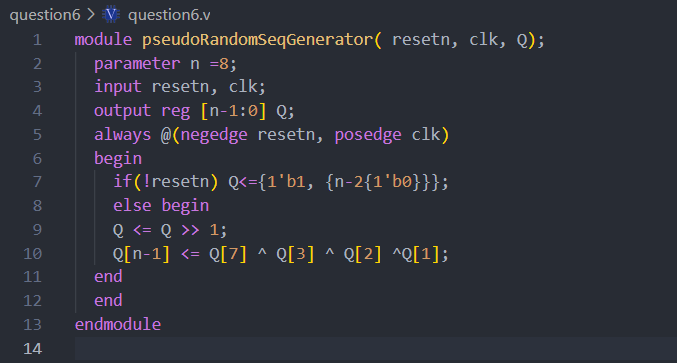
### Simulation waveform



# Pseudo random sequence generator

## Solution:

### Verilog code



### Simulation waveform

