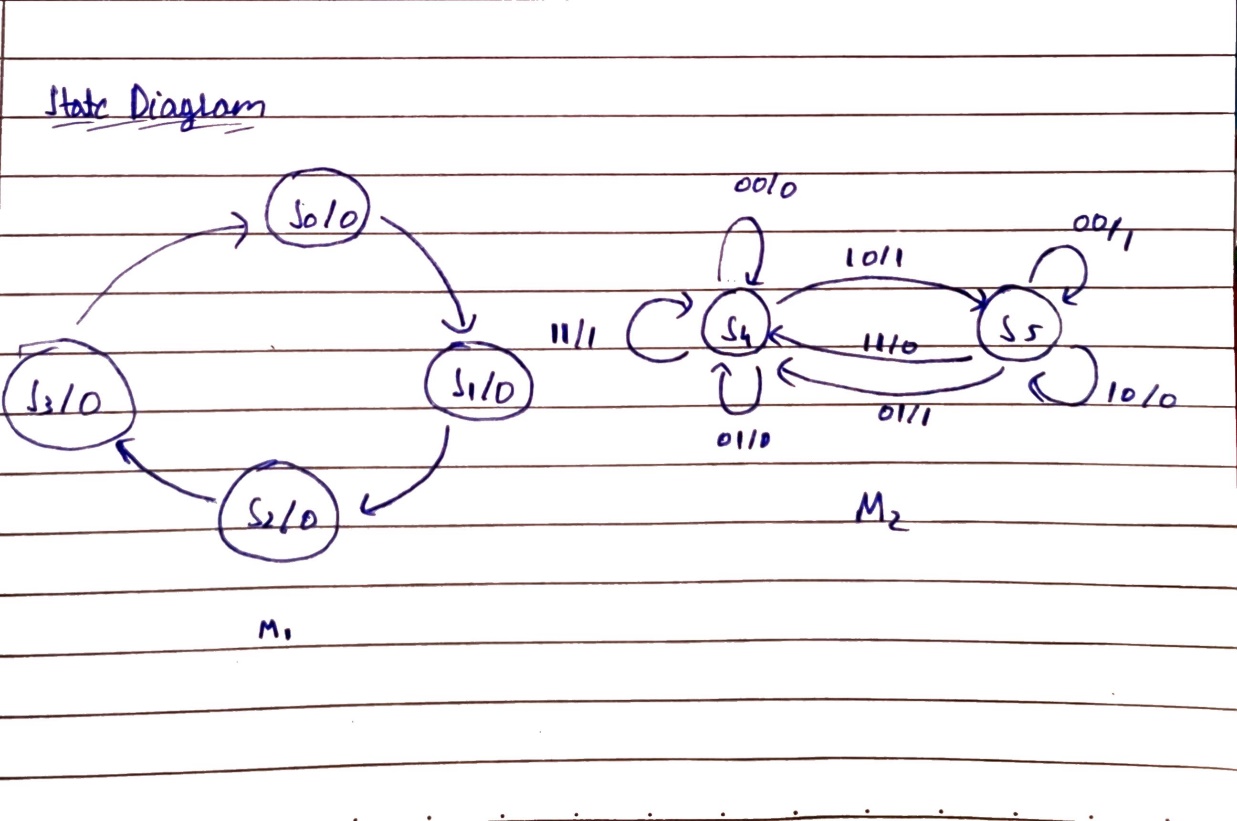


# A digital system has a single input X and a single output Y

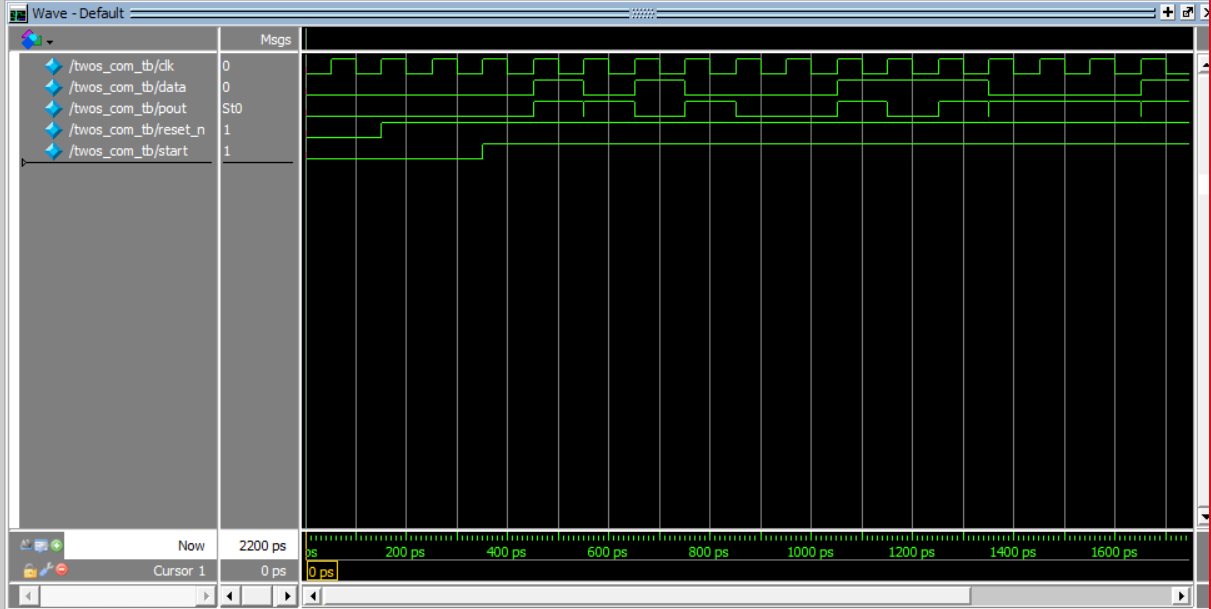
## Solution:

**State Diagram**

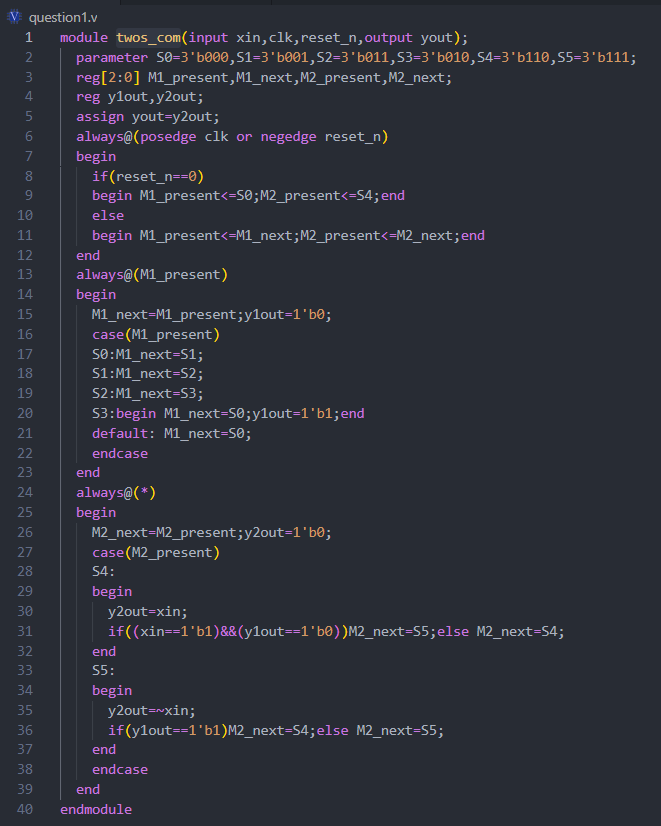
****

Combining two finite state machines. First one is used to count 4 bits and the second one is used to complement the input stream of bits. S0- S3 belong to M1 and S4-S5 belong to M2.

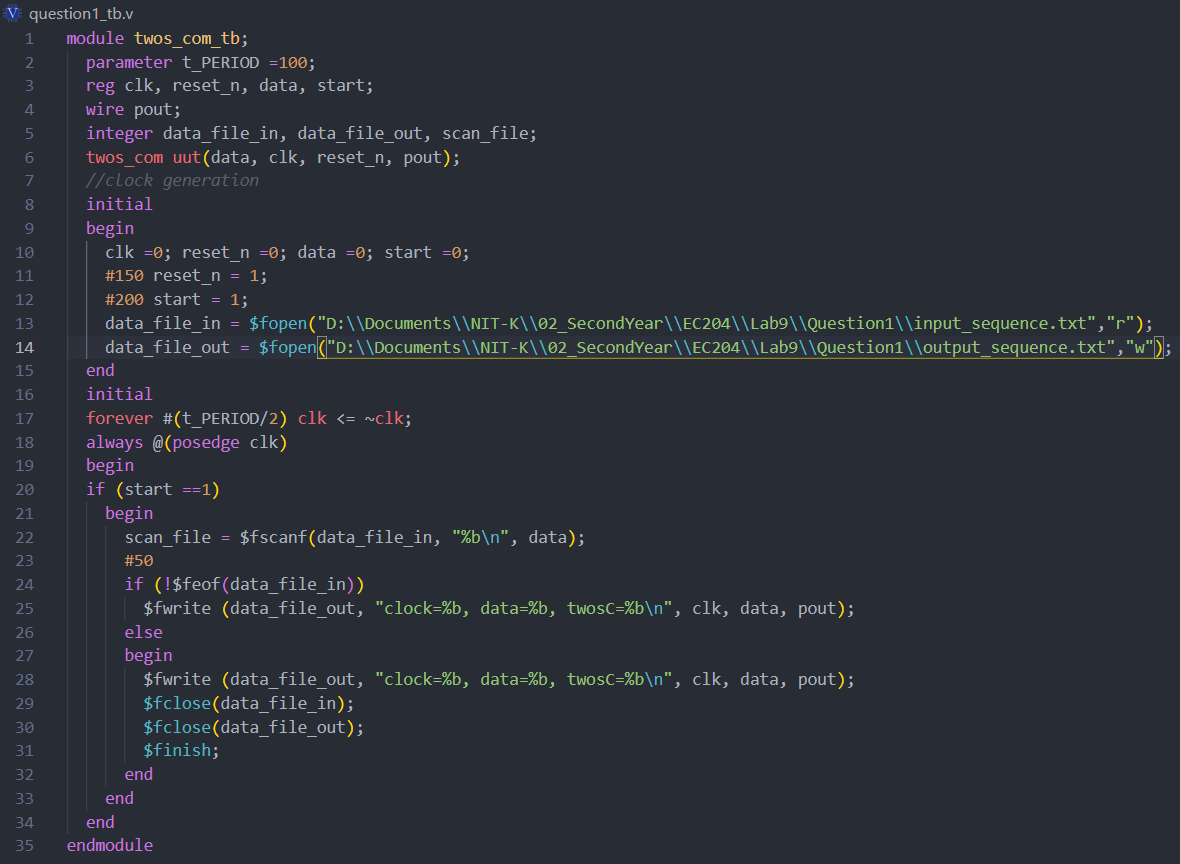
### Simulation



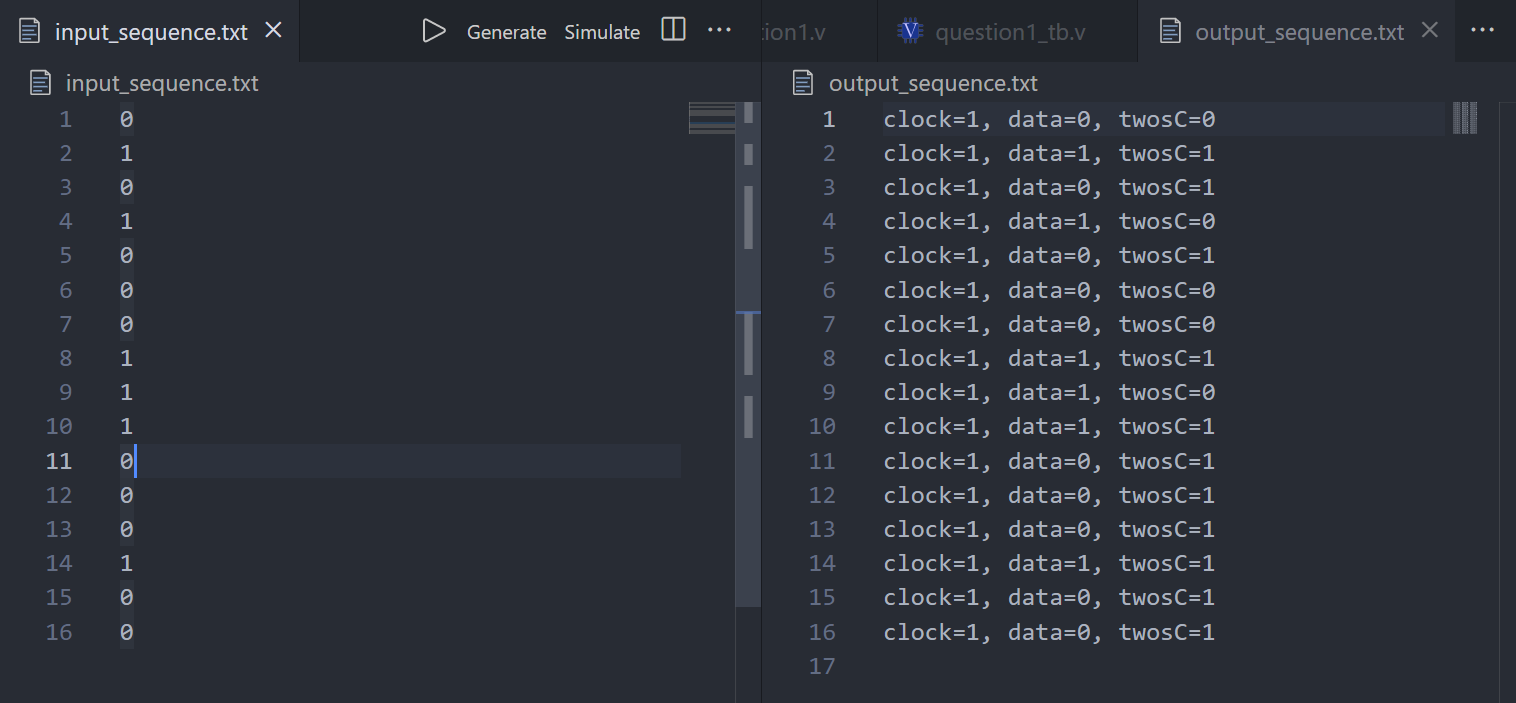
### Verilog code



### Verilog testbench



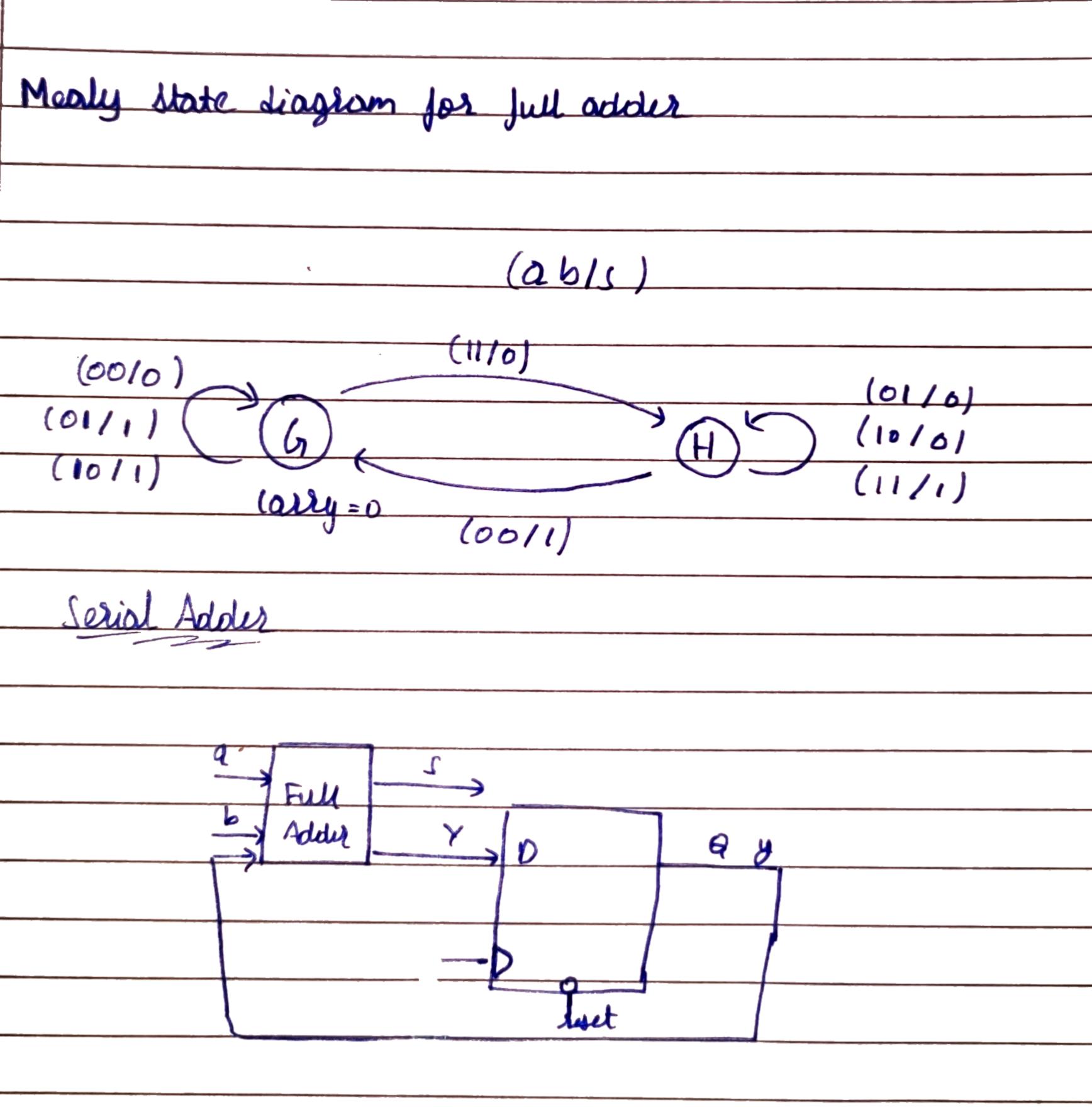
### Output



# Implement a serial adder in Verilog to add two 8 bit numbers using a single full adder and registers

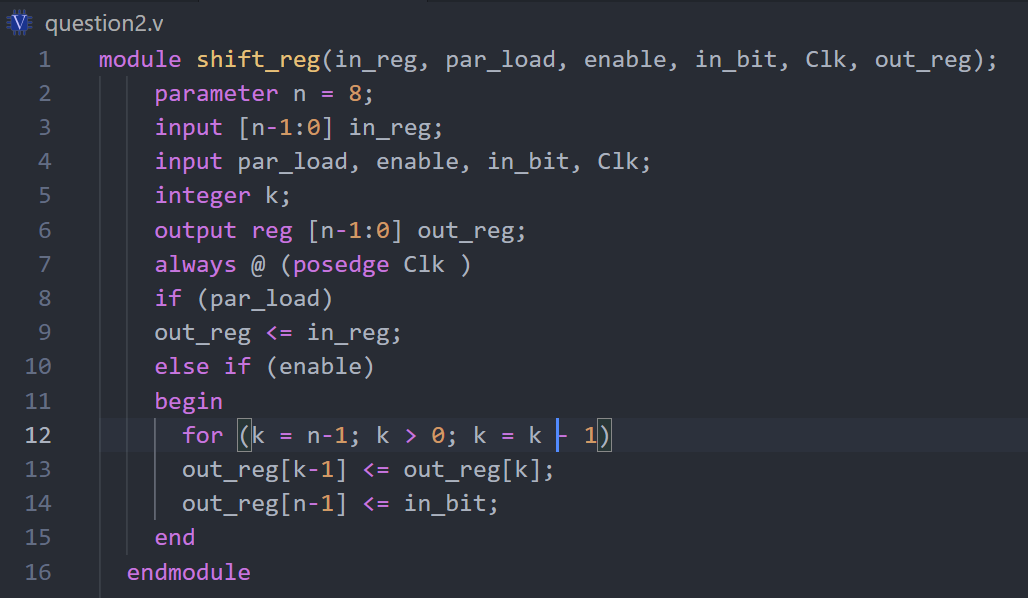
## Solution:

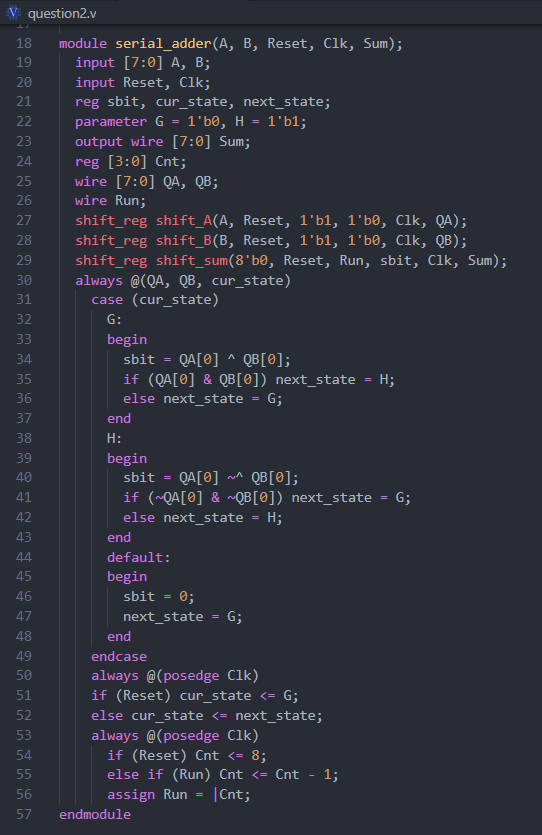
**State Diagram**



Inputs are two 8 bit numbers. Two shift registers are used to give out the digits which are then serially added. The output is similarly combined using another shift register. A mealy finite state machine is used to implement the full adder and a D flip flop to calculate the carry in for the full adder.

### Verilog code





### Simulation

