EC 354
VLSI Design Laboratory Manual

Tools to be used:

- NgSpice for Circuit Simulation.
- MAGIC for Layout and Extraction
- Netgen for LVS
- NgSPICE for Circuit Simulation
- IRSIM for Switch Level Simulation.

Resources:

User Manual for SPICE is available at

- http://172.16.15.11/packages/linux/eda_tools/manuals/spice_manual/
- http://172.16.15.11/packages/linux/eda_tools/tutorials_docs/spice_tutorial/

User manual for MAGIC and IRSIM are available at

- http://172.16.15.11/packages/linux/eda_tools/tutorials_docs/magic_irsim/

PART I

Experiment 1: Study the VI characteristics of NMOS Transistor

Objective:
Study the Input and Output characteristics of NMOS Transistor, effects of L, W, VTO, LAMBDA, VSB, and temperature on the behavior of the transistor.

Procedure:
a) Plot the input and output characteristics by sweeping VDS, VGS for a given L and W.
b) Vary W from a value equal to half the feature size to 10 times the feature size, repeat part (a), study the behavior with variation in W.
c) Vary L from a value equal to half the feature size to 10 times the feature size, repeat part (a), study the behavior with variation in L.
d) Vary VTO within a reasonable range, repeat part (a), study the behaviour with variation in VTO.
e) Vary LAMBDA within a reasonable range, repeat part (a), study the behaviour with variation in LAMBDA.
f) Vary VSB within a reasonable range, repeat part (a), study the change in VTO, and the behavior of transistor.
g) Vary temperature within a reasonable range, repeat part (a), study the change in VTO, and the behavior of transistor.

Experiment 2: Study of MOS inverter with passive resistive load.

Objective:
Study the transfer function, Noise margin, effect on risetime, falltime, propagation delay, power and energy consumed of a MOS Inverter for various L, W of the transistor, load capacitance and rise/fall time of input.

Procedure:
Plot the transfer function and transient response; for various combinations of values of Resistance R, L and W of NMOS transistor. Study the effect of variation of R, W/L ratio of pulldown transisor on risetime, falltime, propagation delay, and power consumed. Estimate the value theoretically and verify with simulated result and justify. Identify the region of operation of driver transistor during the transition of the output. Study the variation in IDS of driver transistor, current through load resistance RL; the charge and discharge current through the load capacitance CL with the transition of output.

Experiment 3 : Study of MOS inverter with active load – NMOS and PMOS (pseudo NMOS load)

Objective:

For a MOS Inverter with active load - NMOS and PMOS (pseudo NMOS load), study the transfer function, Noise margin, effect on risetime, falltime, propagation delay, power and energy consumed with variation in L and W of the pullup and pulldown transistors. Also power and energy consumed with non ideal step input.

Procedure:

a) Plot the transfer function and transient response; for various combinations of values of L and W of both driver and load transistors. Study the effect of W/L ratio of pullup and pulldown transisors on risetime, falltime, propagation delay, power consumed. Estimate the value theoretically and verify with simulated result and justify.

b) For an inverter with equal rise and fall time plot the transient response by varying the risetime and falltime of the input. Study the variations in power and energy consumed per transition. Estimate the value theoretically and verify with simulated result and justify.

c) Plot the transient response for an inverter with equal rise and fall time with various capacitive loads at the output (i.e. estimate the input capacitance of the inverter and try with different fanout loads.) Prepare a table of risetime, falltime, propagation delay, power consumed for various loads for ideal and non-ideal step inputs.

d) Compute the amount of continuous power and dynamic power dissipated.

Experiment 4 : Study of CMOS inverter

Objective:

Study the transfer function, Noise margin, effect on risetime, falltime, propagation delay, power and energy consumed of a CMOS Inverter with variation in L and W of the pullup and pulldown transistors. Also power and energy consumed with non ideal step input.

Procedure:

a) Plot the transfer function and transient response; for various combinations of values of L and W of both NMOS and PMOS transistors. Study the effect of W/L ratio of pullup and pulldown transisors on risetime, falltime, propagation delay, power consumed. Estimate the value theoretically and verify with simulated result and justify.

b) Plot the transient response for an ideal CMOS inverter with equal rise and fall time by varying the risetime and falltime of the input. Study the variations in power and energy consumed per transition. Estimate the value theoretically and verify with simulated result and justify.

c) Plot the transient response for an ideal CMOS inverter with equal rise and fall time with various capacitive loads at the output (i.e. estimate the input capacitance of the inverter and try with different fanout loads.) Prepare a table of risetime, falltime, propagation delay, power consumed for various loads for ideal and non-ideal step inputs.

Experiment 5 : Study of CMOS gates

Objective:
Study the behaviour transfer function, Noise margin, effect on risetime, falltime, propagation delay, power and energy consumed of a CMOS gates like Nand, Nor, functions like AOI (2 input AND gate , 2 input OR gate), and 2 input XOR gate with variation in L and W of the pullup and pulldown transistors. Also power and energy consumed with non ideal step input. Study the effect of VSB due to series connected transistors.

Procedure:
Similar to CMOS inverter experiment. Test with different input combinations and check the change in rise-time, falltime etc with test patterns.

To study the effect of VSB due to series connected transistors:

- connect the substrate of all NMOS to GND and all PMOS to VDD, simulate the circuit.
- connect the source of each transistor to substrate contact of respective transistor, and simulate.
- The first simulation gives you effect of Vsb on series connected transistors.
- Plot the switching waveforms at different nodes and compare.

PART II

Experiment 6: CMOS Inverter Layout and Characterization

Objective:

To learn layout, extract, LVS and characterization processes in the design flow with CMOS inverter as an example.

Procedure:

a) Design a CMOS Inverter for a specified value of risetime and falltime with a specified drivestrength. Write a spice netlist for that CMOS inverter.
b) Layout the CMOS inverter, save it in a .mag file. Provide sufficient width to the power rails.
c) Using the extresis and extract commands, extract the circuit parameters, parasitics into a .ext file.
d) Using the exttospice command convert the .ext file into a spice netlist.
e) Using the netgen command, compare the extracted spice netlist with the original netlist to verify that the laid out circuit indeed represents the original spice netlist.
f) Simulate the extracted spice netlist using NgSPICE. Compute the risetime and the falltime of this inverter with the design specifications. Justify the difference if any.
g) Compute the area occupied by the cell.
h) Try to minimize the area and improve the speed for the same load by using optimal layout techniques and create a standard cell for the inverter.
i) Find the power consumed per transition of output for various loads, continuous power dissipated.
j) Tabulate all your observations like area of the cell, input capacitance, output capacitance, rise and fall time power dissipated for various loads.

Experiment 7: Generation of a Standard Cell library

Objective:
To create a standard cell library of CMOS Gates – Two and Three input NAND, NOR, AND, OR gates, AOI for Two products of Two variables, D-Latch and a D-Flipflop.

Procedure:
Similar to experiment 6.

Reference for guidelines to design of standard cell library: http://www.vlsitechnology.org