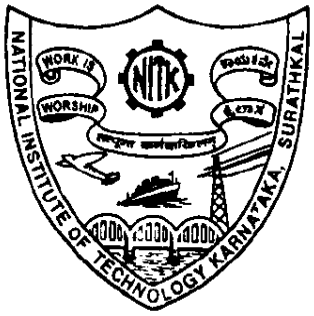
EC792 HPCA

LAB - 6



Report Submission

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Exercises

1. Implementing a simple CPU system

Comparing different CPUs

Parameter	AtomicSimpleCPU	TimingSimpleCPU	DerivO3CPU	InOrderCPU
Simulation Seconds	0.000008	0.000509	0.000142	0.000143
Total Instructions Simulated	6571	6571	6571	6583
IPC (Instructions per Cycle)	0.817256	0.012945	0.463023	0.045961
CPI (Cycles per Instruction)	1.223606	77.250646	2.159073	21.757557
Total CPU Cycles	8055	508541	141690	143230
Host Seconds	0.00	0.01	0.04	0.03
Host Memory Usage (Bytes)	404654224	404793488	404672800	404663440
Number of Integer Instructions	6505	6505	6505	Not Available
Number of Floating Point Instructions	12	12	12	Not Available
Number of Load Instructions	1212	1212	1212	Not Available

Number of Store Instructions	1082	1082	1082	Not Available
Average Memory Read Queue Length	0.00	1.00	1.45	1.45
Average Memory Write Queue Length	0.00	24.09	24.00	24.00
DRAM Bytes Read	39790	39790	160225	160225
DRAM Bytes Written	8246	8246	8246	8246
DRAM Read Bandwidth (Byte/Second)	4940402285	78243445.46457414	1118655310	1118655310
DRAM Write Bandwidth (Byte/Second)	1023839086	16285805.86422727	57571738	57571738

Brief Analysis:

- IPC and CPI: The TimingSimpleCPU shows drastically different performance characteristics compared to the other CPUs, with an extremely low IPC and very high CPI, indicating it simulates a very conservative execution model. This contrasts sharply with the AtomicSimpleCPU, which simulates an idealized scenario, and the DerivO3CPU and InOrderCPU, which offer more realistic, detailed simulations.
- Simulation Time: While the AtomicSimpleCPU and the DerivO3CPU offer quick simulations, the TimingSimpleCPU requires more simulated seconds, closely followed by the InOrderCPU.
- Memory Usage: Slight variations in host memory usage across models suggest different internal complexities and the data structures they use for simulation.
- DRAM Activities: The AtomicSimpleCPU and TimingSimpleCPU have similar DRAM read and write activities, whereas DerivO3CPU and InOrderCPU show increased DRAM activity, possibly due to more complex memory handling mechanisms.

The TimingSimpleCPU, with its unique performance profile, emphasizes the trade-offs between simulation speed and accuracy/detail.

The AtomicSimpleCPU is optimal for fast, broad-strokes simulation.
DerivO3CPU provides detailed, nuanced simulations with a focus on out-of-order execution; InOrderCPU focuses on in-order execution, offering a balance between detail and performance. The TimingSimpleCPU stands out for simulations where conservative execution and memory interaction are critical, offering a different perspective on system behavior.

2. Cache comparison

Comparing different cache configurations:

Metric	System 1	System 2	System 3	System 4
Total Committed Instructions	6607	6607	6607	6607
Committed Control Instructions	1521	1521	1521	1521
D-Cache Demand Hits	2120	2120	2120	2120
D-Cache Demand Misses	146	146	146	146
D-Cache Demand Miss Latency	15032000	15032000	15032000	15774000

Brief Analysis:

System 1: default configuration
System 2: Larger L1/L2 (512kB)
System 3: Higher Assoc. (4)
System 4: Longer latency (4)

Since the given program just prints in the console the variation in the performance except when the cache latency is increased.