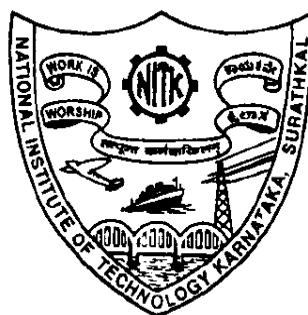


EC806 DSD using FPGA

LAB - 2



Report Submission

By

Inbasekaran Perumal

201EC226

Pranav Koundinya

201EC247

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING
NATIONAL INSTITUTE OF TECHNOLOGY KARNATAKA, SURATHKAL
SRINIVASNAGAR 575025 KARNATAKA INDIA

10 September 2023

1) In this exercise, we will use the switches as input and display the output using the 7-segment LED. Seven-segment LED decoder – Model a BCD to a segment decoder, download the code onto the board, and test its functionality. Read the section on 7-segment LEDs in the board user manual first. *Note that to turn ON a segment you need to put logic 0.*

Kmap

i) Truth table

A	B	C	D	a	b	c	d	e	f	g
0	0	0	0	1	1	1	1	1	1	0
0	0	0	1	0	1	1	0	0	0	0
0	0	1	0	1	1	0	1	1	0	1
0	0	1	1	1	1	1	1	0	0	1
0	1	0	0	0	1	1	0	0	1	1
0	1	0	1	1	0	1	1	0	1	1
0	1	1	0	1	0	1	1	1	1	1
0	1	1	1	1	1	1	0	0	0	0
1	0	0	0	1	1	1	1	1	1	1
1	0	0	1	1	1	1	1	0	1	1
1	0	1	0	x	x	x	x	x	x	x
1	0	1	1	x	x	x	x	x	x	x
1	1	0	0	x	x	x	x	x	x	x
1	1	0	1	x	x	x	x	x	x	1
1	1	1	0	x	x	x	x	x	y	
1	1	1	1	x	x	x	x	x	x	x

Note: x represents don't care

#102 a

AB	CD	00	01	11	10
00	1	0	1	1	
01	0	1	1	1	
11	X	X	X	X	
10	1	1	X	X	

$$a = A + BD + C + \bar{B}\bar{D}$$

ii) #102 b

AB	CD	00	01	11	10
00	1	1	1	1	1
01	1	C	1	0	
11	X	X	X	X	
10	1	1	X	X	

$$b = \bar{B} + \bar{C}\bar{D} + CD$$

iii) #102 c

1	1	1	0	
1	1	1	1	
X	X	X	X	
1	1	X	X	

$$c = \bar{C} + D + B$$

iv) #102 d

AB	CD	00	01	11	10
00	1	0	1	1	1
01	0	1	0	1	
11	X	X	X		
10	1	1	X	X	

$$d = \bar{B}\bar{D} + \bar{D}C + B\bar{C}D + C\bar{D} + A$$

v) #102 e

AB	CD	00	01	11	10
00	1	1	0	1	1
01	0	1	0	0	1
11	X	X	X		
10	1	1	X	X	

$$e = \bar{B}\bar{D} + C\bar{D}$$

vii) # for g

vi) # for f

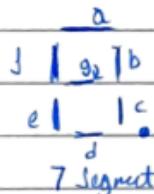
AB \ CD	00	01	11	10
00	1	0	0	0
01	1	1	0	1
11	X	X	X	X
10	1	1	X	X

AB \ CD	00	01	11	10
00	0	0	1	1
01	1	1	0	1
11	X	X	X	X
10	1	1	X	X

$$f = A + B\bar{D} + \bar{C}\bar{D} + B\bar{C}$$

$$g = \bar{B}C + BC + A + B\bar{D}$$

For the combination where all ABCD are zero (See the truth table)
a=1, b=1, c=1, d=1, e=1, f=1, g=0, so 7 segment LED shows 1-1(0).



Verilog Code:

```

module bcd_seven_segment_decoder(
  input [3:0]x,
  output a,
  output b,
  output c,
  output d,
  output e,
  output f,
  output g
);

```

```

assign a = ~(x[3] | x[2]&x[0] | x[1] | ~x[2] & ~x[0]);
assign b = ~(~x[2] | ~x[1] & ~x[0] | x[1] & x[0]);
assign c = ~(~x[1] | x[0] | x[2]);
assign d = ~(x[3] | ~x[2]&~x[0] | ~x[2] & x[1] | x[2] & ~x[1] & x[0] | x[1] & ~x[0]);
assign e = ~((~x[2] | x[1]) & ~x[0]);
assign f = ~(x[3] | x[2] & ~x[0] | ~x[1] & ~x[0] | x[2] & ~x[1]);
assign g = ~(~x[2] & x[1] | x[2] & ~x[1] | x[3] | x[2] & ~x[0]);

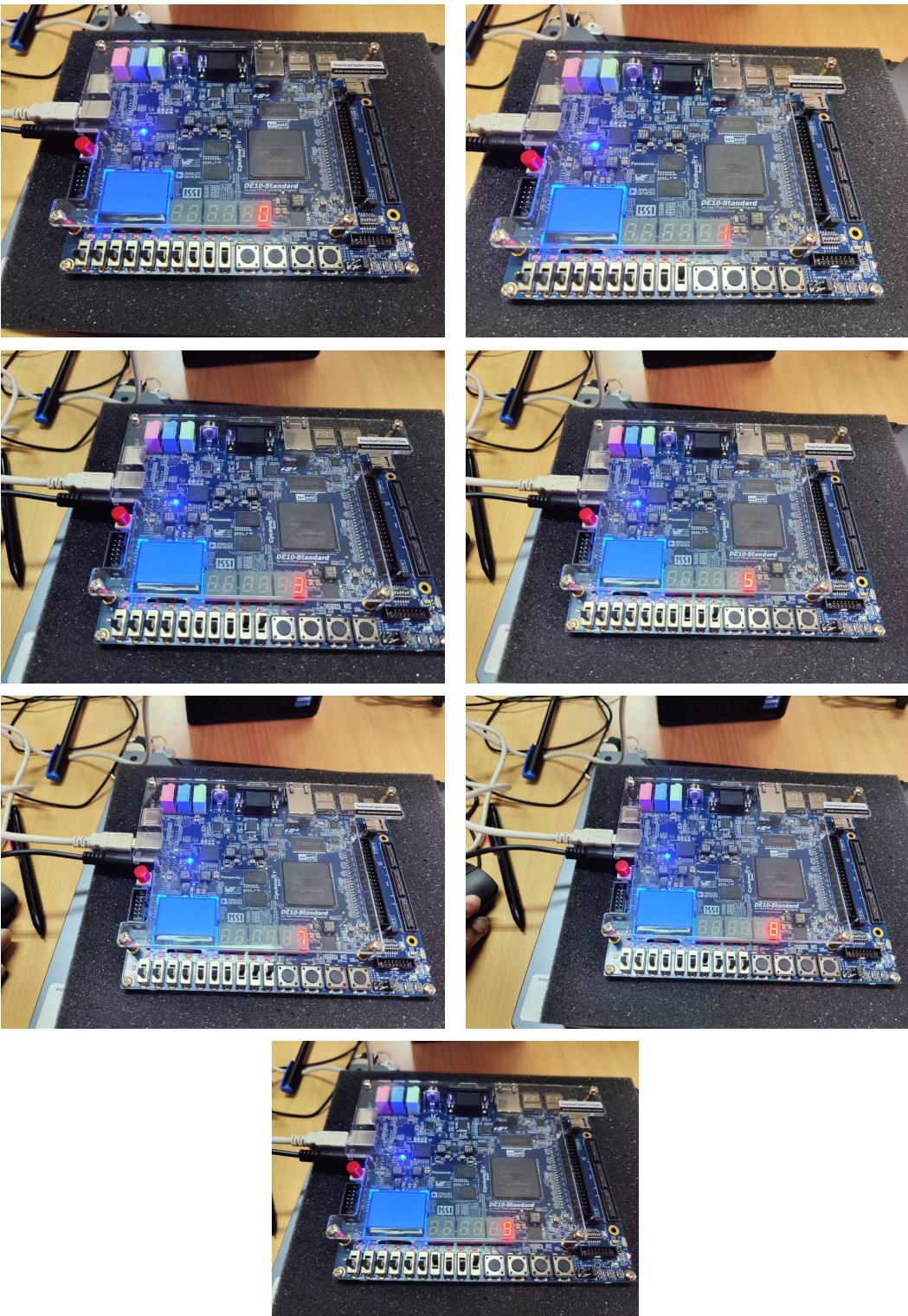
```

endmodule

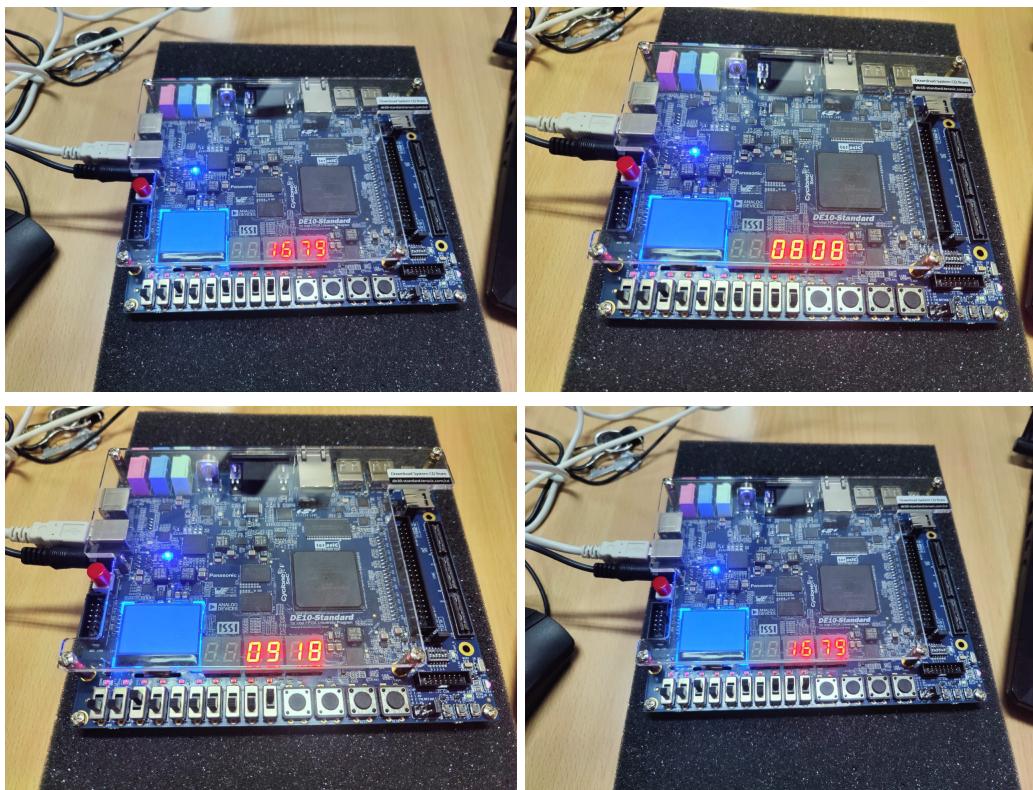
Resource Utilization:

Flow Summary	
<<Filter>>	
Flow Status	Successful - Wed Sep 20 14:54:27 2023
Quartus Prime Version	21.1.1 Build 850 06/23/2022 SJ Lite Edition
Revision Name	bcd_seven_segment_decoder
Top-level Entity Name	bcd_seven_segment_decoder
Family	Cyclone V
Device	5CSXFC6D6F31C6
Timing Models	Final
Logic utilization (in ALMs)	4 / 41,910 (< 1 %)
Total registers	0
Total pins	11 / 499 (2 %)
Total virtual pins	0
Total block memory bits	0 / 5,662,720 (0 %)
Total DSP Blocks	0 / 112 (0 %)
Total HSSI RX PCSs	0 / 9 (0 %)
Total HSSI PMA RX Deserializers	0 / 9 (0 %)
Total HSSI TX PCSs	0 / 9 (0 %)
Total HSSI PMA TX Serializers	0 / 9 (0 %)
Total PLLs	0 / 15 (0 %)
Total DLLs	0 / 4 (0 %)

Observations:



Q2 Using the adder4 module designed in the last class model a BCD adder that can add two BCD numbers. Provide inputs using the switches SW0-8. - Display the output using HEX1 and HEX2 and on LED0-4. - Display the inputs using HEX4 and HEX6.



Verilog Code:

Top-Level module:

```
module bcd_adder(
    input [3:0]A,
    input [3:0]B,
```

```

        output [3:0]a,
        output [3:0]b,
        output [3:0]c,
        output [3:0]d,
        output [3:0]e,
        output [3:0]f,
        output [3:0]g,
        output [4:0]L
    );
    wire [7:0]S;
    bcd_fourbit_adder mbcd(A, B, S, L);
    bcd_seven_segment_decoder aout(A, a[0], b[0], c[0], d[0], e[0], f[0], g[0]);
    bcd_seven_segment_decoder bout(B, a[1], b[1], c[1], d[1], e[1], f[1], g[1]);
    bcd_seven_segment_decoder lsn_out(S[3:0], a[2], b[2], c[2], d[2], e[2], f[2], g[2]);
    bcd_seven_segment_decoder msn_out(S[7:4], a[3], b[3], c[3], d[3], e[3], f[3], g[3]);
endmodule

```

BCD fourbit adder:

```

module bcd_fourbit_adder(
    input [3:0]A,
    input [3:0]B,
    output [7:0]S,
    output [4:0]L
);
    wire [4:0]T;
    wire gt_9, not_needed;

    fourbit_adder add1(A, B, 1'b0, T[3:0], T[4]);
    assign L = T;

    assign gt_9 = T[4] | T[3]&T[2] | T[1]&T[3];

    fourbit_adder add2({1'b0, gt_9, gt_9, 1'b0}, T[3:0], 1'b0, S[3:0], not_needed);

    assign S[7:4] = {3'b000, gt_9};

endmodule

```

BCD to seven segment display module:

```

module bcd_seven_segment_decoder(
    input [3:0]x,
    output a,
    output b,
    output c,
    output d,
    output e,

```

```

        output f,
        output g
    );

    assign a = ~(x[3] | x[2]&x[0] | x[1] | ~x[2] & ~x[0]);
    assign b = ~(~x[2] | ~x[1] & ~x[0] | x[1] & x[0]);
    assign c = ~(~x[1] | x[0] | x[2]);
    assign d = ~(~x[3] | ~x[2]&~x[0] | ~x[2] & x[1] | x[2] & ~x[1] & x[0] | x[1] & ~x[0]);
    assign e = ~((~x[2] | x[1]) & ~x[0]);
    assign f = ~(x[3] | x[2] & ~x[0] | ~x[1] & ~x[0] | x[2] & ~x[1]);
    assign g = ~(~x[2] & x[1] | x[2] & ~x[1] | x[3] | x[2] & ~x[0]);

endmodule

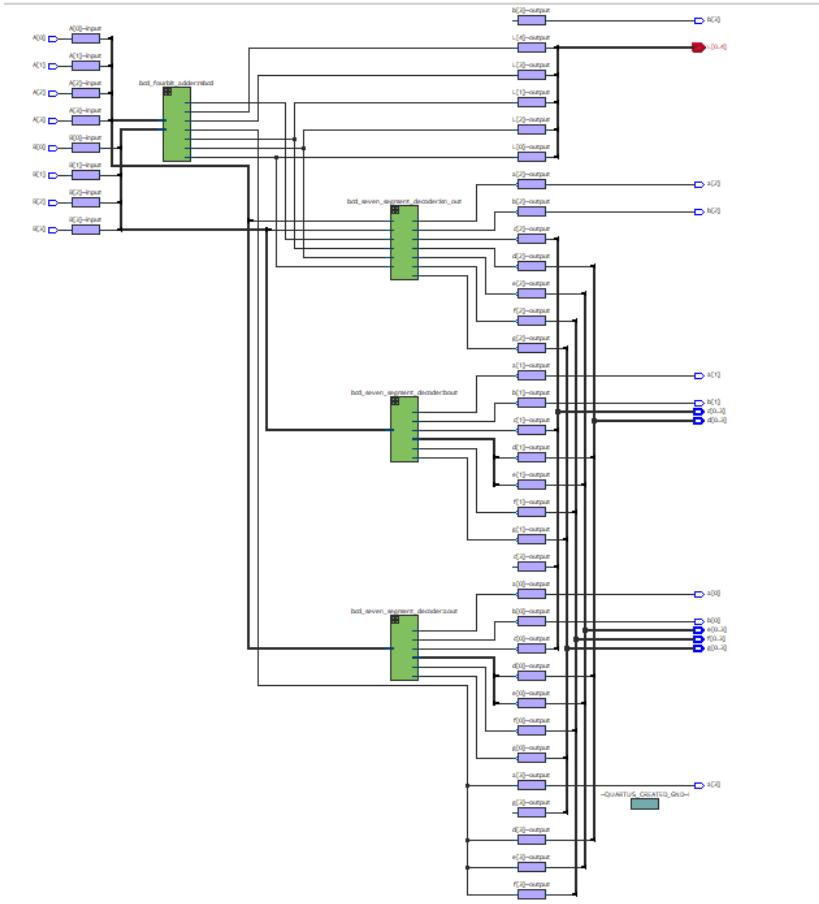
```

The code for four-bit adder has been taken from the lab session of previous week.

Resource Utilization:

Flow Summary	
<<Filter>>	
Flow Status	Successful - Wed Sep 20 17:08:24 2023
Quartus Prime Version	21.1.1 Build 850 06/23/2022 SJ Lite Edition
Revision Name	bcd_adder
Top-level Entity Name	bcd_adder
Family	Cyclone V
Device	5CSXFC6D6F31C6
Timing Models	Final
Logic utilization (in ALMs)	19 / 41,910 (< 1 %)
Total registers	0
Total pins	41 / 499 (8 %)
Total virtual pins	0
Total block memory bits	0 / 5,662,720 (0 %)
Total DSP Blocks	0 / 112 (0 %)
Total HSSI RX PCSs	0 / 9 (0 %)
Total HSSI PMA RX Deserializers	0 / 9 (0 %)
Total HSSI TX PCSs	0 / 9 (0 %)
Total HSSI PMA TX Serializers	0 / 9 (0 %)
Total PLLs	0 / 15 (0 %)
Total DLLs	0 / 4 (0 %)

Netlist:



Pin Planner:

Top View - Wire Bond
Cyclone V - 5CSXFC6D6F31C6

