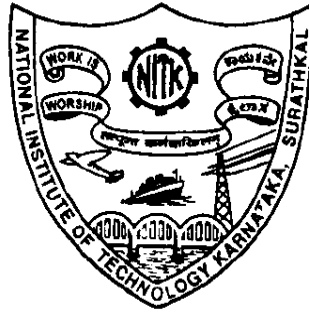


# **EC806 DSD using FPGA**

## **LAB - 3**



### **Report Submission**

By

Inbasekaran Perumal

201EC226

Pranav Koundinya

201EC247

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING  
NATIONAL INSTITUTE OF TECHNOLOGY KARNATAKA, SURATHKAL  
SRINIVASNAGAR 575025 KARNATAKA INDIA

27 September 2023

<b>1. Behavioral verilog code for (a) 2 to 4 decoder (b) M to N decoder.....</b>	<b>3</b>
Verilog code.....	3
a) 2 to 4 decoder.....	3
b) M to N decoder.....	4
Simulation results.....	5
a) 2 to 4 decoder.....	5
b) M to N decoder.....	5
Resource utilization.....	6
a) 2 to 4 decoder.....	6
b) M to N decoder.....	6
<b>2. Verilog code to Count the number of 1s in a 8 bit number.....</b>	<b>6</b>
Verilog code.....	6
Simulation results.....	8
Resource utilization.....	8
<b>3. Verilog code to Implement <math>F(v,w,x,y,z) = (0, 2, 3, 4, 8, 21, 22, 29, 31)</math>.....</b>	<b>8</b>
Verilog code.....	8
Simulation results.....	9
Resource utilization.....	10
<b>4. Verilog code to model a 16 bit magnitude comparator.....</b>	<b>10</b>
Verilog code.....	10
Simulation results.....	11
Resource utilization.....	11
<b>5. Verilog code to Count the number of leading 0s in an 8 bit number.....</b>	<b>12</b>
Verilog code.....	12
Simulation results.....	13
Resource utilization.....	13

## 1. Behavioral verilog code for (a) 2 to 4 decoder (b) M to N decoder

### Verilog code

#### a) 2 to 4 decoder

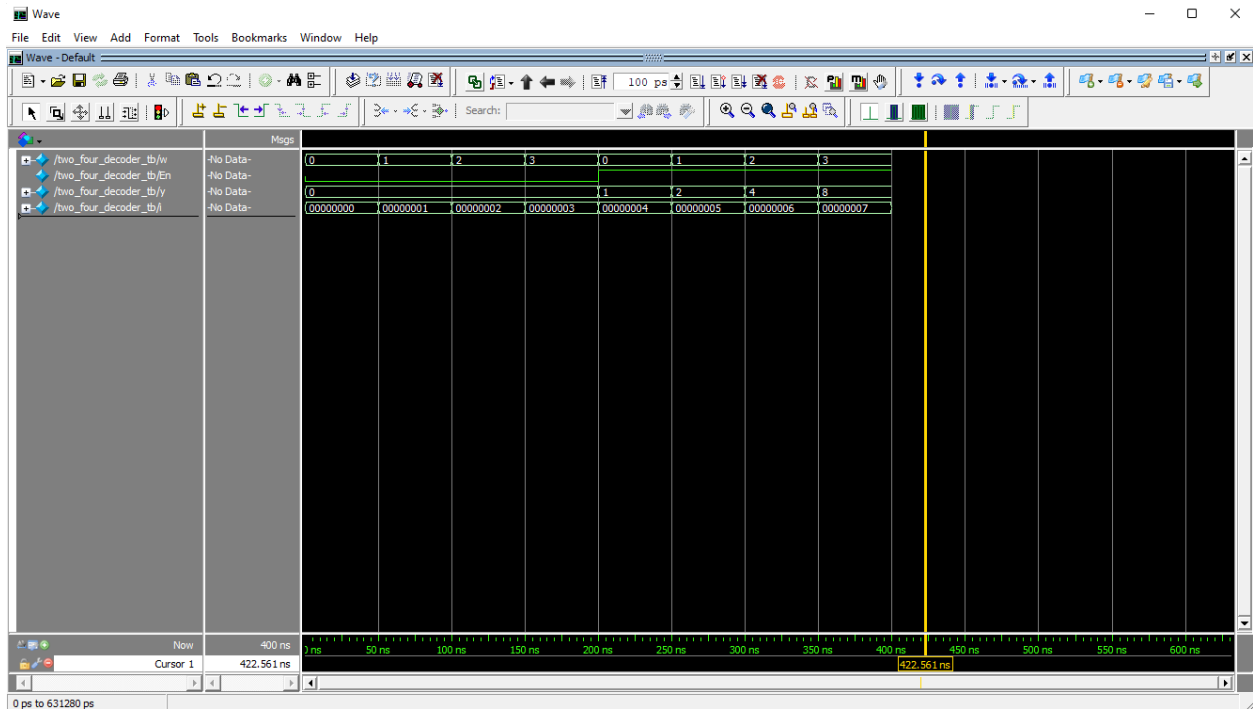
```
module two_four_decoder(  
    input [1:0]w,  
    input En,  
    output reg [3:0]y  
);  
  
    always @*  
    begin  
        if (~En)  
            y = 4'b0000;  
        else  
            y = 1 << w;  
        end  
    endmodule  
  
`timescale 1ns/1ps  
  
module two_four_decoder_tb();  
    reg [1:0]w;  
    reg En;  
    wire [3:0]y;  
    integer i;  
    two_four_decoder dut (w, En, y);  
    initial  
    begin  
        for(i = 0; i < 8; i = i + 1)  
        begin  
            {En, w} <= i;  
            #50;  
        end  
        $stop;  
    end  
endmodule
```

## b) M to N decoder

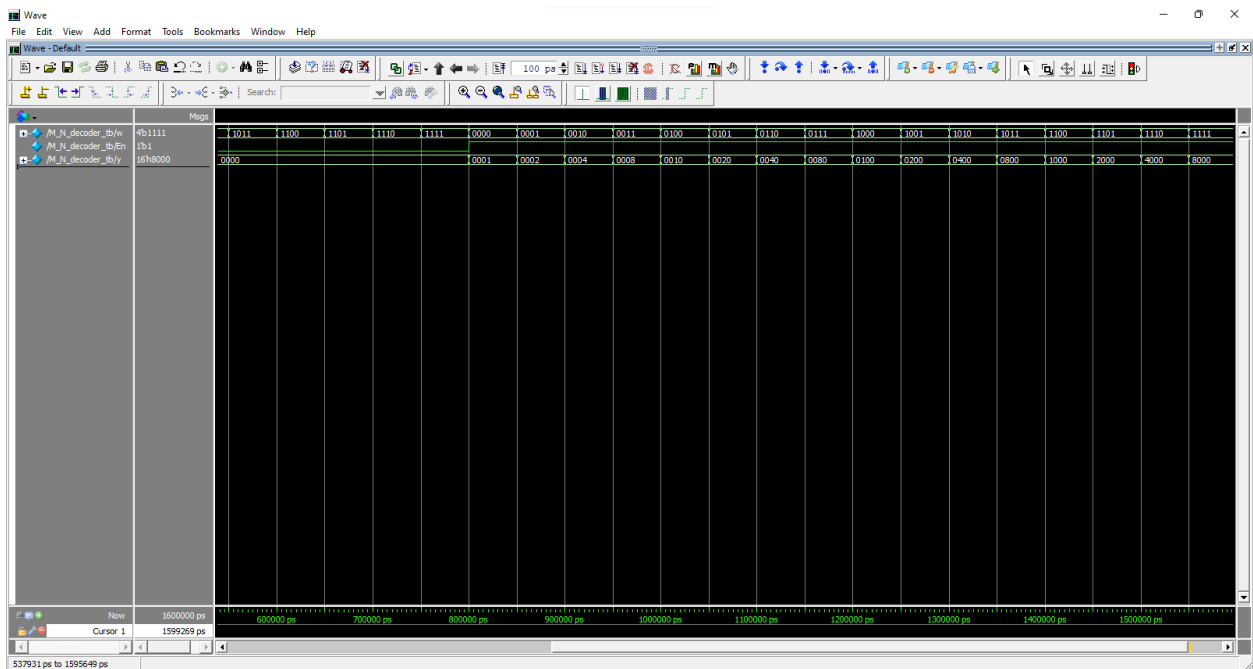
```
module M_N_decoder(  
    w, En, y  
);  
    parameter M = 4;  
    parameter N = 2**M;  
    input [M-1:0]w;  
    input En;  
    output reg [N-1:0]y;  
    always @*  
    begin  
        if(~En)  
            y = {N{1'b0}};  
        else  
            y = 1 << w;  
        end  
    endmodule  
  
`timescale 1ns/1ps  
  
module M_N_decoder_tb();  
    reg [3:0]w;  
    reg En;  
    wire [15:0]y;  
    integer i;  
    M_N_decoder dut (w, En, y);  
    initial  
    begin  
        for(i = 0; i < 32; i = i + 1)  
        begin  
            {En, w} <= i;  
            #50;  
        end  
        $stop;  
    end  
endmodule
```

## Simulation results

### a) 2 to 4 decoder



### b) M to N decoder



## Resource utilization

### a) 2 to 4 decoder

two_four_decoder.v	two_four_decoder_tb.v	Compilation Report - two_four_decoder
Table of Contents		
Flow Summary		
Flow Settings		
Flow Non-Default Global Settings		
Flow Elapsed Time		
Flow OS Summary		
Flow Log		
Analysis & Synthesis		
Fitter		
Assembler		
Timing Analyzer		
EDA Netlist Writer		
Flow Messages		
Flow Suppressed Messages		
Flow Summary		
Flow Status		
Quartus Prime Version		
Revision Name		
Top-level Entity Name		
Family		
Device		
Timing Models		
Logic utilization (in ALMs)		
Total registers		
Total pins		
Total virtual pins		
Total block memory bits		
Total DSP Blocks		
Total HSSI RX PCSs		
Total HSSI PMA RX Deserializers		
Total HSSI TX PCSs		
Total HSSI PMA TX Serializers		
Total PLLs		
Total DLLs		

### b) M to N decoder

Compilation Report - two_four_decoder
Table of Contents
Flow Summary
Flow Settings
Flow Non-Default Global Settings
Flow Elapsed Time
Flow OS Summary
Flow Log
Analysis & Synthesis
Fitter
Assembler
Timing Analyzer
EDA Netlist Writer
Flow Messages
Flow Suppressed Messages
Flow Summary
Flow Status
Quartus Prime Version
Revision Name
Top-level Entity Name
Family
Device
Timing Models
Logic utilization (in ALMs)
Total registers
Total pins
Total virtual pins
Total block memory bits
Total DSP Blocks
Total HSSI RX PCSs
Total HSSI PMA RX Deserializers
Total HSSI TX PCSs
Total HSSI PMA TX Serializers
Total PLLs
Total DLLs

## 2. Verilog code to Count the number of 1s in a 8 bit number

### Verilog code

```
module ones_count (
```

```

input  [7:0]x,
output reg [3:0]y
);
integer i;
always @(x)
begin
y = 'b0;
for(i = 0; i < 8;i = i + 1)
y = y + x[i];
end
endmodule

```

```

`timescale 1ns/1ps

```

```

module ones_count_tb();

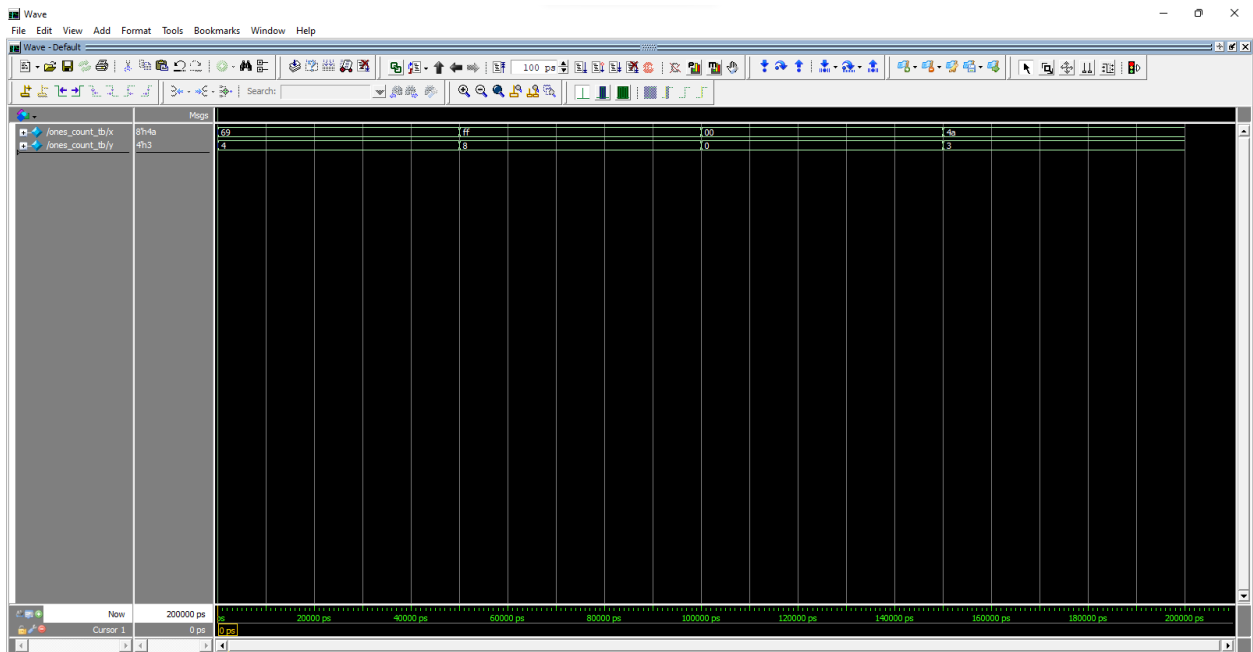
```

```

reg [7:0]x;
wire [3:0]y;
ones_count dut(x, y);
initial
begin
x <= 8'h69; #50
x <= 8'hff; #50
x <= 8'h00; #50
x <= 8'h4a; #50;
$stop;
end
endmodule

```

## Simulation results



## Resource utilization

Compilation Report - two_four_decoder	
Table of Contents	
Flow Summary	Flow Summary
Flow Settings	
Flow Non-Default Global Set	
Flow Elapsed Time	
Flow OS Summary	
Flow Log	
Analysis & Synthesis	
Fitter	
Assembler	
Timing Analyzer	
EDA Netlist Writer	
Flow Messages	
Flow Suppressed Messages	

Flow Status	Successful - Fri Sep 29 16:37:26 2023
Quartus Prime Version	22.1std.2 Build 922 07/20/2023 SC Lite Edition
Revision Name	two_four_decoder
Top-level Entity Name	ones_count
Family	Cyclone V
Device	5CSXFC6D6F31C6
Timing Models	Final
Logic utilization (in ALMs)	6 / 41,910 (< 1 %)
Total registers	0
Total pins	12 / 499 (2 %)
Total virtual pins	0
Total block memory bits	0 / 5,662,720 (0 %)
Total DSP Blocks	0 / 112 (0 %)
Total HSSI RX PCSs	0 / 9 (0 %)
Total HSSI PMA RX Deserializers	0 / 9 (0 %)
Total HSSI TX PCSs	0 / 9 (0 %)
Total HSSI PMA TX Serializers	0 / 9 (0 %)
Total PLLs	0 / 15 (0 %)
Total DLLs	0 / 4 (0 %)

## 3. Verilog code to Implement $F(v,w,x,y,z) = (0, 2, 3, 4, 8, 21, 22, 29, 31)$

### Verilog code

```
module sop(input [4:0]x, output reg f);  
always @(*) begin
```



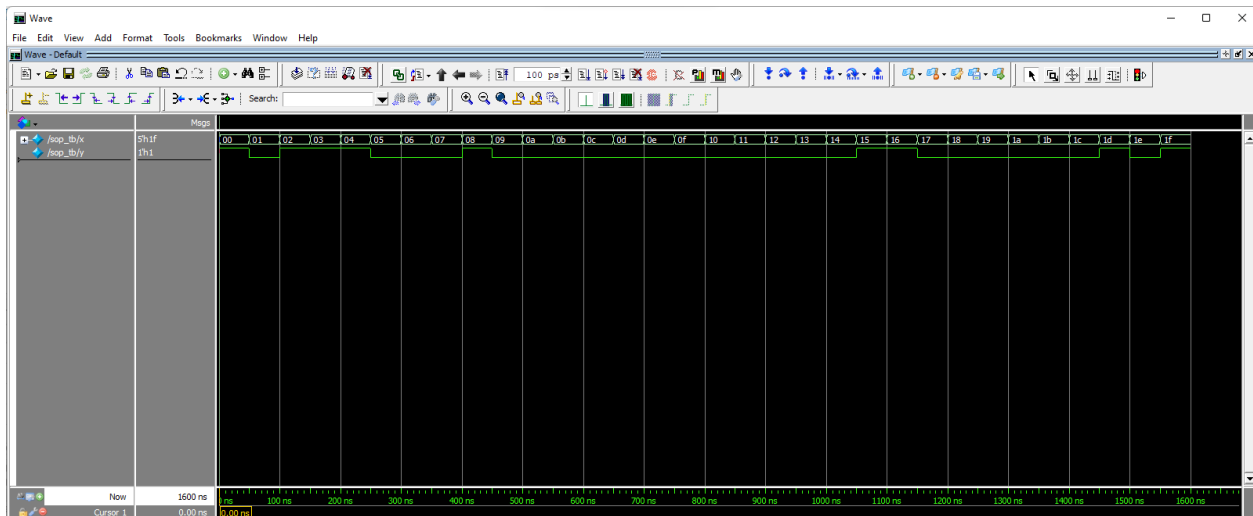
```

if(x == 0 || x == 2 || x == 3 || x == 4 || x == 8 || x == 21 || x == 22 ||
x == 29 || x == 31)
f = 1;
else
f = 0;
end
endmodule

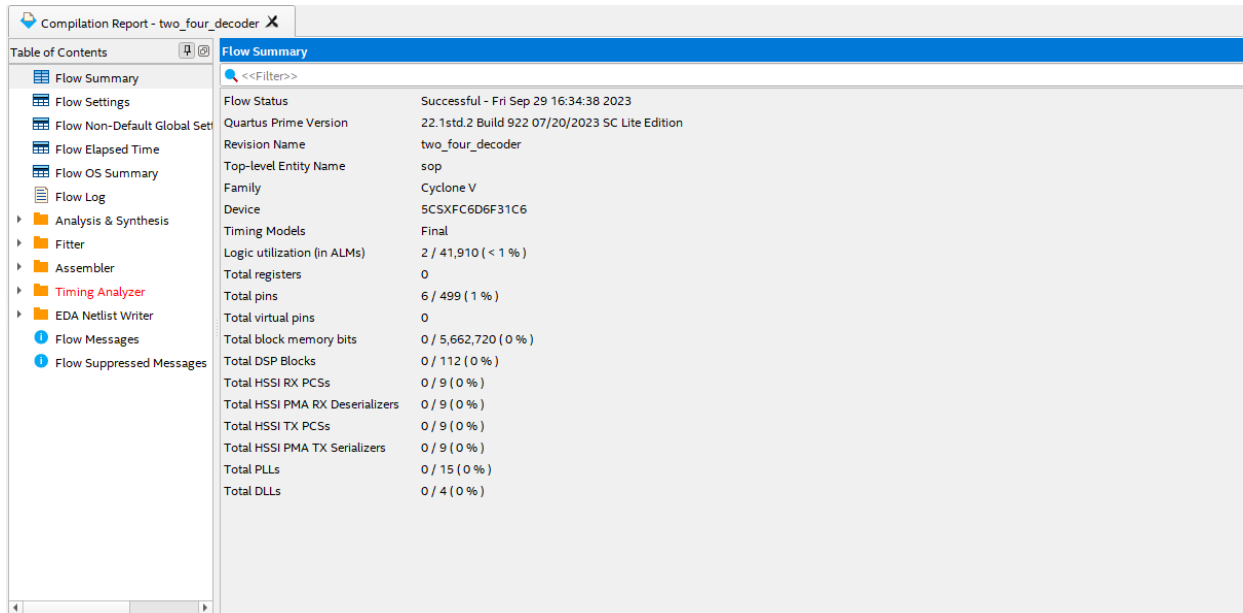
`timescale 1ns/1ps
module sop_tb();
reg [4:0]x;
wire y;
integer i = 0;
sop dut (x,y);
initial
begin
for(i = 0; i < 32; i = i + 1)
begin
x <= i;
#50;
end
//$stop;
end
Endmodule

```

## Simulation results



## Resource utilization



The screenshot shows the 'Flow Summary' window in Quartus Prime. The left sidebar contains a 'Table of Contents' with various project stages. The main area displays a table of resource utilization metrics.

<<Filter>>	
Flow Status	Successful - Fri Sep 29 16:34:38 2023
Quartus Prime Version	22.1std.2 Build 922 07/20/2023 SC Lite Edition
Revision Name	two_four_decoder
Top-level Entity Name	sop
Family	Cyclone V
Device	5C5XFC6D6F31C6
Timing Models	Final
Logic utilization (in ALMs)	2 / 41,910 (< 1 %)
Total registers	0
Total pins	6 / 499 (1 %)
Total virtual pins	0
Total block memory bits	0 / 5,662,720 (0 %)
Total DSP Blocks	0 / 112 (0 %)
Total HSSI RX PCSs	0 / 9 (0 %)
Total HSSI PMA RX Deserializers	0 / 9 (0 %)
Total HSSI TX PCSs	0 / 9 (0 %)
Total HSSI PMA TX Serializers	0 / 9 (0 %)
Total PLLs	0 / 15 (0 %)
Total DLLs	0 / 4 (0 %)

## 4. Verilog code to model a 16 bit magnitude comparator

### Verilog code

```
module comp_16(In1, In2, Gt,Eq,Lt);
input [15:0] In1, In2;
output Gt,Lt,Eq;
assign Gt = (In1 > In2) ? 1'b1 : 1'b0;
assign Lt = (In1 < In2) ? 1'b1 : 1'b0;
assign Eq = (In1 == In2) ? 1'b1 : 1'b0;
endmodule
```

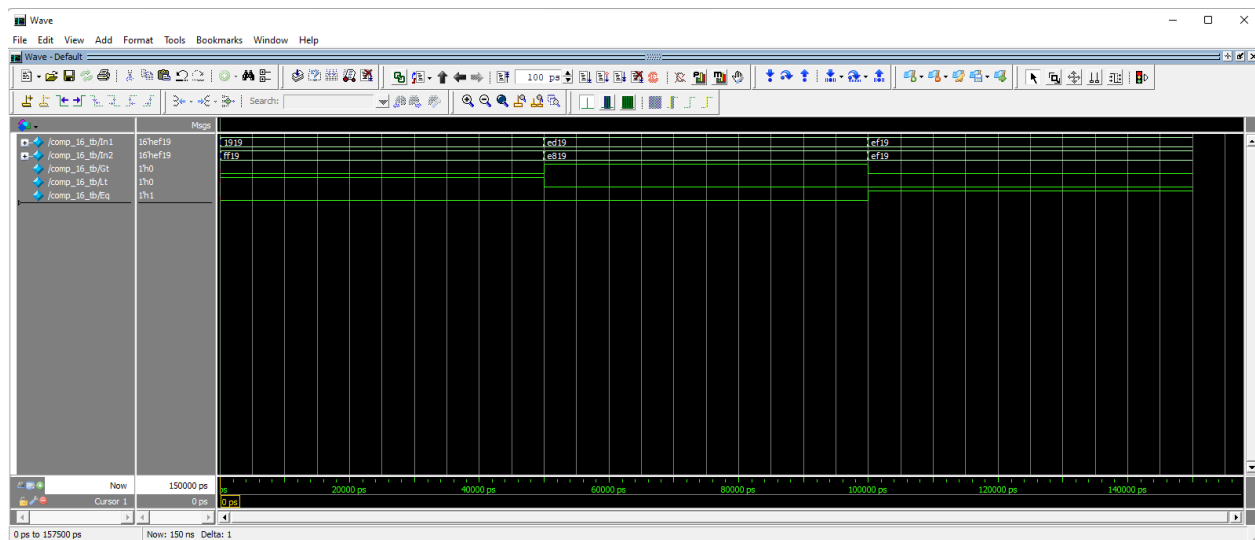
```
`timescale 1ns/1ps
module comp_16_tb();
reg [15:0] In1, In2;
wire Gt,Lt,Eq;
comp_16 dut(In1,In2,Gt,Eq,Lt);
initial
begin
In1 = 16'b0001_1001_0001_1001;
In2 = 16'b1111_1111_0001_1001;
#50
In2 = 16'b1110_1000_0001_1001;
```

```

In1 = 16'b1110_1101_0001_1001;
#50
In1 = 16'b1110_1111_0001_1001;
In2 = 16'b1110_1111_0001_1001;
#50;
end
endmodule

```

## Simulation results



## Resource utilization

Table of Contents	
Flow Summary	Flow Summary
Flow Settings	Flow Settings
Flow Non-Default Global Set	Flow Non-Default Global Set
Flow Elapsed Time	Flow Elapsed Time
Flow OS Summary	Flow OS Summary
Flow Log	Flow Log
Analysis & Synthesis	Analysis & Synthesis
Fitter	Fitter
Assembler	Assembler
Timing Analyzer	Timing Analyzer
EDA Netlist Writer	EDA Netlist Writer
Flow Messages	Flow Messages
Flow Suppressed Messages	Flow Suppressed Messages

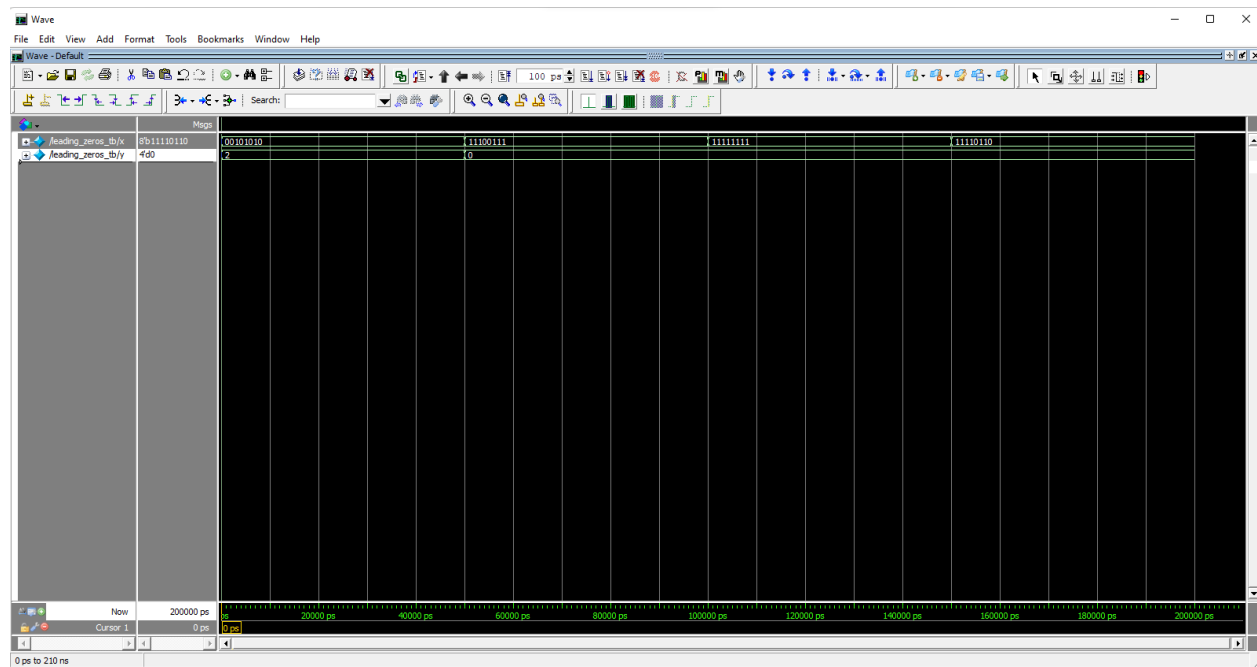
Flow Summary	
<<Filter>>	
Flow Status	Successful - Fri Sep 29 16:39:47 2023
Quartus Prime Version	22.1std.2 Build 922 07/20/2023 SC Lite Edition
Revision Name	two_four_decoder
Top-level Entity Name	comp_16
Family	Cyclone V
Device	5CSXFC6D6F31C6
Timing Models	Final
Logic utilization (in ALMs)	18 / 41,910 (< 1 %)
Total registers	0
Total pins	35 / 499 (7 %)
Total virtual pins	0
Total block memory bits	0 / 5,662,720 (0 %)
Total DSP Blocks	0 / 112 (0 %)
Total HSSI RX PCSs	0 / 9 (0 %)
Total HSSI PMA RX Deserializers	0 / 9 (0 %)
Total HSSI TX PCSs	0 / 9 (0 %)
Total HSSI PMA TX Serializers	0 / 9 (0 %)
Total PLLs	0 / 15 (0 %)
Total DLLs	0 / 4 (0 %)

## 5. Verilog code to Count the number of leading 0s in an 8 bit number

### Verilog code

```
module leading_zeros(  
    input  [7:0]x,  
    output reg [3:0]y  
);  
always @ (x)  
begin  
    casex(x)  
        8'b00000000 : y = 4'b1000;  
        8'b00000001 : y = 4'b0111;  
        8'b0000001x : y = 4'b0110;  
        8'b000001xx : y = 4'b0101;  
        8'b00001xxx : y = 4'b0100;  
        8'b0001xxxx : y = 4'b0011;  
        8'b001xxxxx : y = 4'b0010;  
        8'b01xxxxxx : y = 4'b0001;  
        8'b1xxxxxxx : y = 4'b0000;  
    endcase  
end  
endmodule  
  
`timescale 1ns/1ps  
  
module leading_zeros_tb();  
    reg [7:0]x;  
    wire [3:0]y;  
    leading_zeros dut (x, y);  
    initial  
    begin  
        x = 8'b0010_1010; #50  
        x = 8'b1110_0111; #50  
        x = 8'b1111_1111; #50  
        x = 8'b1111_0110; #50;  
    end  
endmodule
```

## Simulation results



## Resource utilization

Compilation Report - two\_four\_decoder X

Table of Contents		Flow Summary
	Flow Summary	<<Filter>>
	Flow Settings	
	Flow Non-Default Global Set	
	Flow Elapsed Time	
	Flow OS Summary	
	Flow Log	
	Analysis & Synthesis	
	Fitter	
	Assembler	
	Timing Analyzer	
	EDA Netlist Writer	
	Flow Messages	
	Flow Suppressed Messages	

Item	Status / Value	Date / Time
Flow Status	Successful	Fri Sep 29 16:41:54 2023
Quartus Prime Version	22.1std.2 Build 922 07/20/2023 SC Lite Edition	
Revision Name	two_four_decoder	
Top-level Entity Name	leading_zeros	
Family	Cyclone V	
Device	5CSXFC6D6F31C6	
Timing Models	Final	
Logic utilization (in ALMs)	4 / 41,910 (< 1 %)	
Total registers	0	
Total pins	12 / 499 (2 %)	
Total virtual pins	0	
Total block memory bits	0 / 5,662,720 (0 %)	
Total DSP Blocks	0 / 112 (0 %)	
Total HSSI RX PCs	0 / 9 (0 %)	
Total HSSI PMA RX Deserializers	0 / 9 (0 %)	
Total HSSI TX PCs	0 / 9 (0 %)	
Total HSSI PMA TX Serializers	0 / 9 (0 %)	
Total PLLs	0 / 15 (0 %)	
Total DLLs	0 / 4 (0 %)	