LAB IV

Sequential circuit design

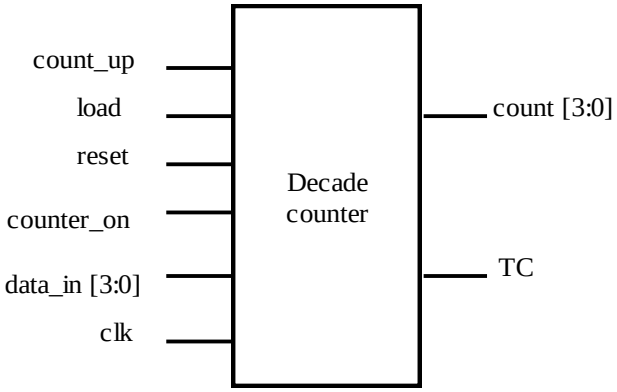
Objectives:

To design simple sequential logic circuits using Verilog and implement using using DE1 SOC/DE10

Exercise

In this lab we will design a decade counter and display the output using the 7 segment LED.

1. **Decade Counter** - Model a synchronous up/down decade counter with asynchronous reset. The counter is rising edge triggered.
   If the **load = 1**, the data **data_in** is loaded into the counter.
   If the **counter_on=counter_up=1,** the counter is incremented, the Terminal carry output **TC=1** when the counter is in state 9
   If the **counter_on=1 and counter_up=0,** the counter is decremented, the Terminal carry output **TC=1** when the counter is in state 0.



Provide the inputs data_in, counter_on, reset, load, count_up through **SW0-SW9.** Display the output using **LEDR0-3** and the rightmost seven segment LED **HEX0**.

Clock – The DE1 SOC/DE10 board has four 50MHz clock signals connected to the FPGA which can be used for user logic. Use CLOCK_50 connected to PIN_AF14 (*Refer Section 3.5 User manual).* This clock has to be reduced to a lower frequency using a clock divider and then used in the counter.
You can use the push button switches KEY0-3 for giving single pulses

Sample code for clock divider

```
reg [26:0] divcntr;
wire divclk;

always @(posedge clk)
   divcntr <= divcntr +1;
assign divclk = divcntr[26];
```

2. Use two decade counter modules to form a two-digit decimal up/down counter. Use the 4 push button keys if you need additional switches for providing input.