Lab III

Combinational Circuit Design

Objectives:

To model simple combinational logic circuits using Verilog and simulate them

Exercise:

1. Behavioral verilog code for (a) 2 to 4 decoder (b) M to N decoder
2. Verilog code to Count the number of 1s in a 8 bit number
3. Verilog code to Implement F(v,w,x,y,z) = Σ (0, 2, 3, 4, 8, 21, 22, 29, 31)
4. Verilog code to model a 16 bit magnitude comparator
5. Verilog code to Count the number of leading 0s in an 8 bit number