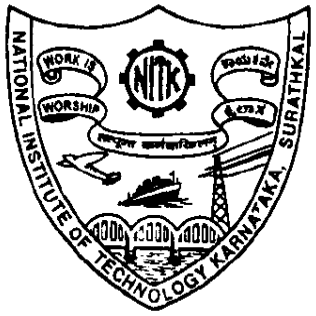
EC806 DSD using FPGA

LAB - 4



Report Submission

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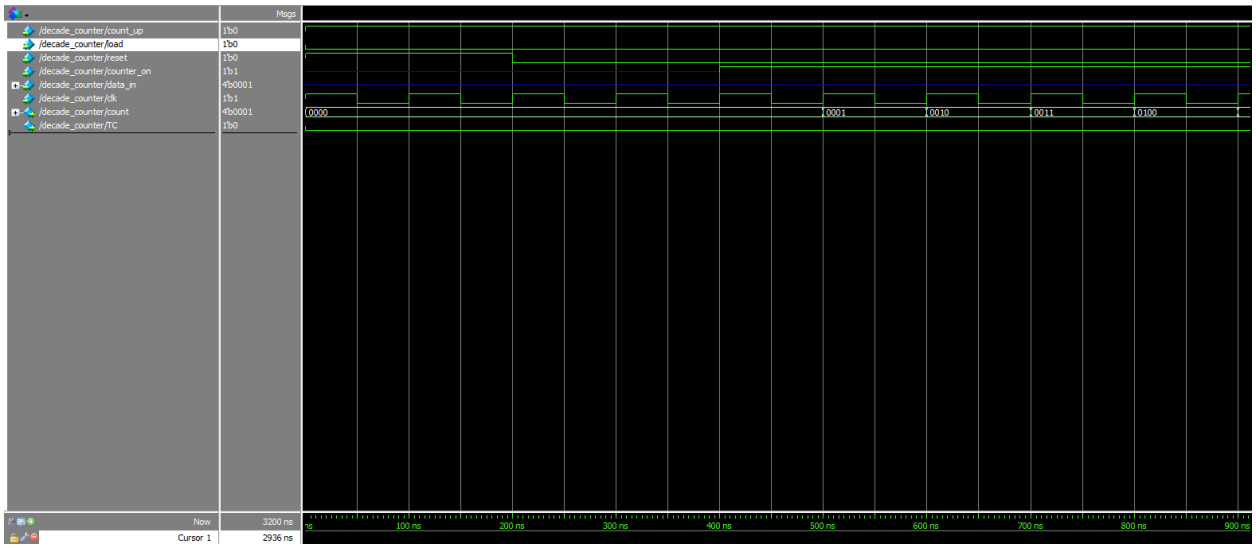
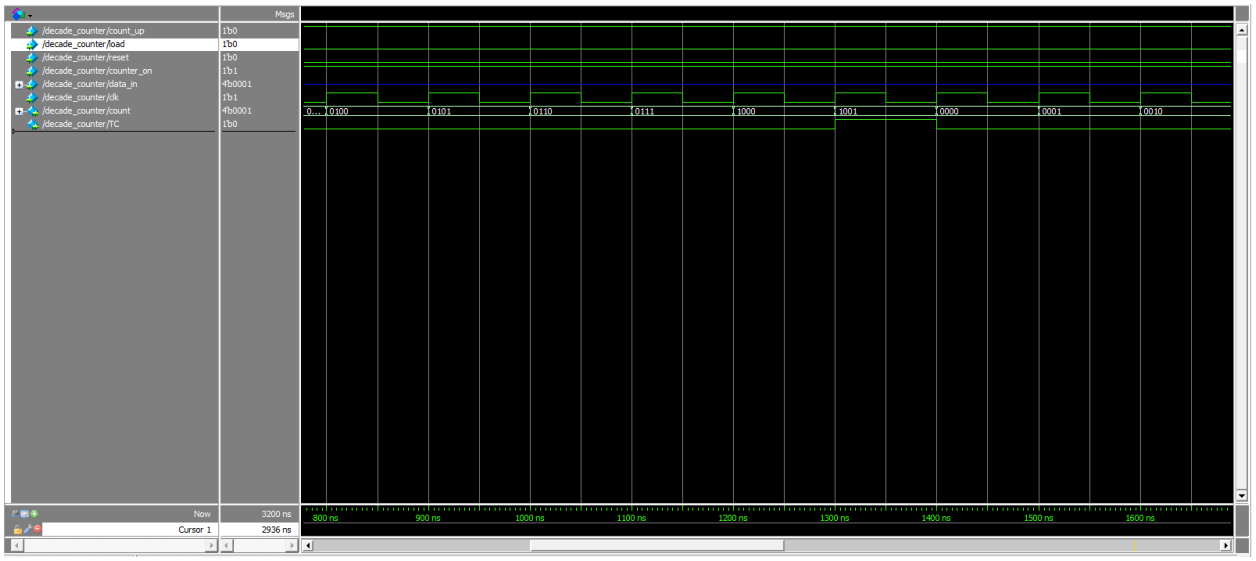
1. Behavioral verilog code for one-digit decade counter

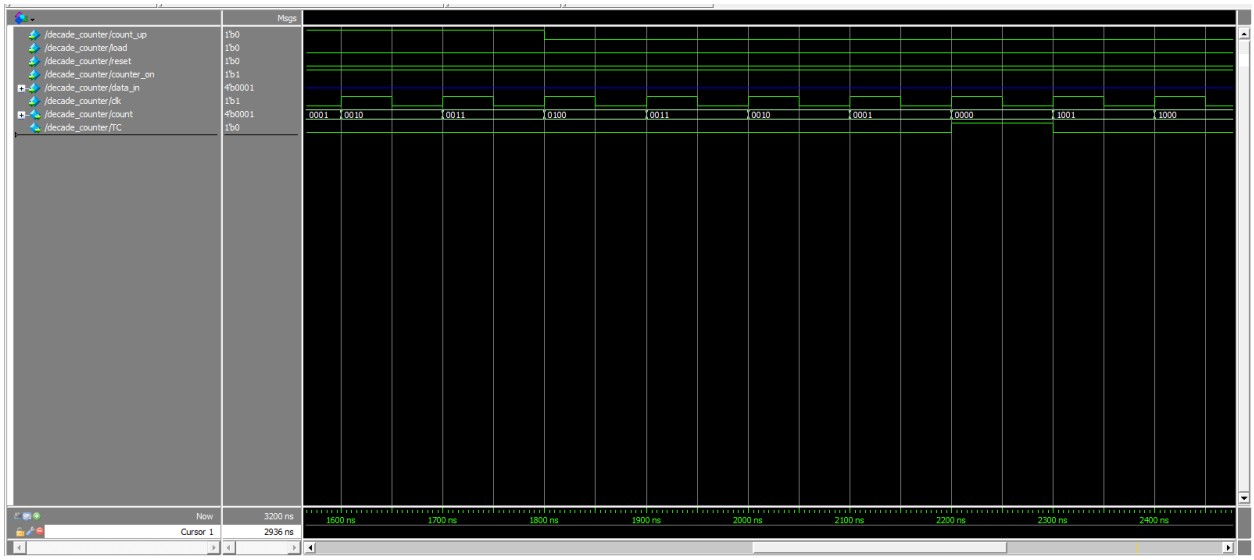
Verilog code:

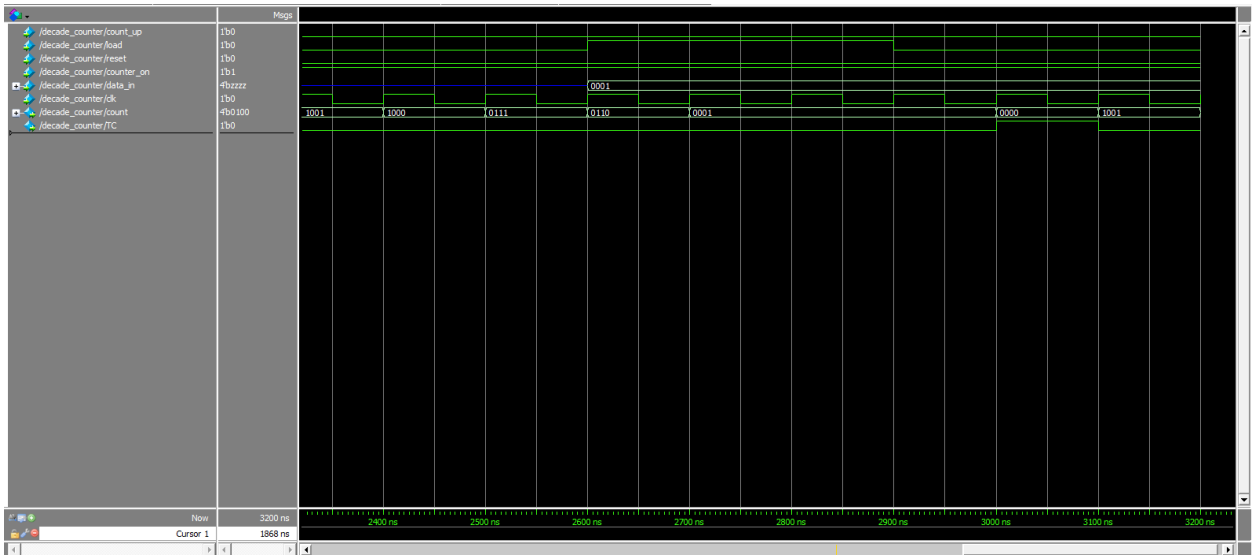
```
module decade_counter(
      input count_up,
      input load,
      input reset,
      input counter_on,
      input [3:0]data_in,
      input clk,
      output reg [3:0]count,
      output TC
);

      always @(posedge reset or posedge clk)
      begin
            if(reset)
                  count <= 4'b0000;
            else if(load)
                  count <= data_in;
            else if(counter_on)
            begin
                  if(count_up)
                        if(count == 9)
                              count <= 0;
                        else
                              count <= count + 1;
                  else
                        if(count == 0)
                              count <= 9;
                        else
                              count <= count - 1;
            end
            else
                  count <= count;
      end

      assign TC = (counter_on) && (~load) && ((~count_up && count == 4'b0000)
                  || (count_up && count == 4'b1001));

endmodule
```

Simulation Results:






Msgs
/decade_counter/count_up
/decade_counter/load
/decade_counter/reset
/decade_counter/counter_on
/decade_counter/data_in
/decade_counter/clk
/decade_counter/count
/decade_counter/TC
1'b0
1'b0
1'b0
1'b1
4'b0001
1'b1
4'b0001
1'b0
0001
0010
0011
0100
0011
0010
0001
0000
1001
1000
Now
3200 ns
Cursor 1
2936 ns
1600 ns
1700 ns
1800 ns
1900 ns
2000 ns
2100 ns
2200 ns
2300 ns
2400 ns

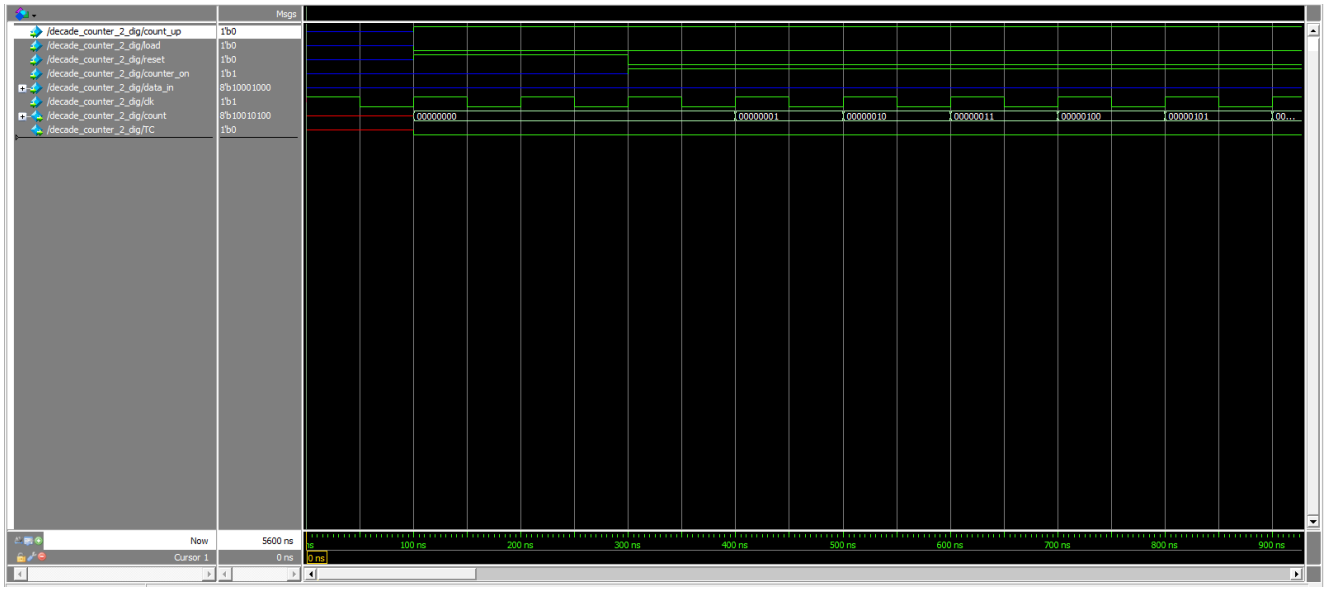

Msgs
/decade_counter/count_up
/decade_counter/load
/decade_counter/reset
/decade_counter/counter_on
/decade_counter/data_in
/decade_counter/clk
/decade_counter/count
/decade_counter/TC
1'b0
1'b0
1'b0
1'b1
4'bzzzz
1'b0
4'b0100
1'b0
0001
1001
1000
0111
0110
0001
0000
1001
Now
3200 ns
Cursor 1
1868 ns
2400 ns
2500 ns
2600 ns
2700 ns
2800 ns
2900 ns
3000 ns
3100 ns
3200 ns

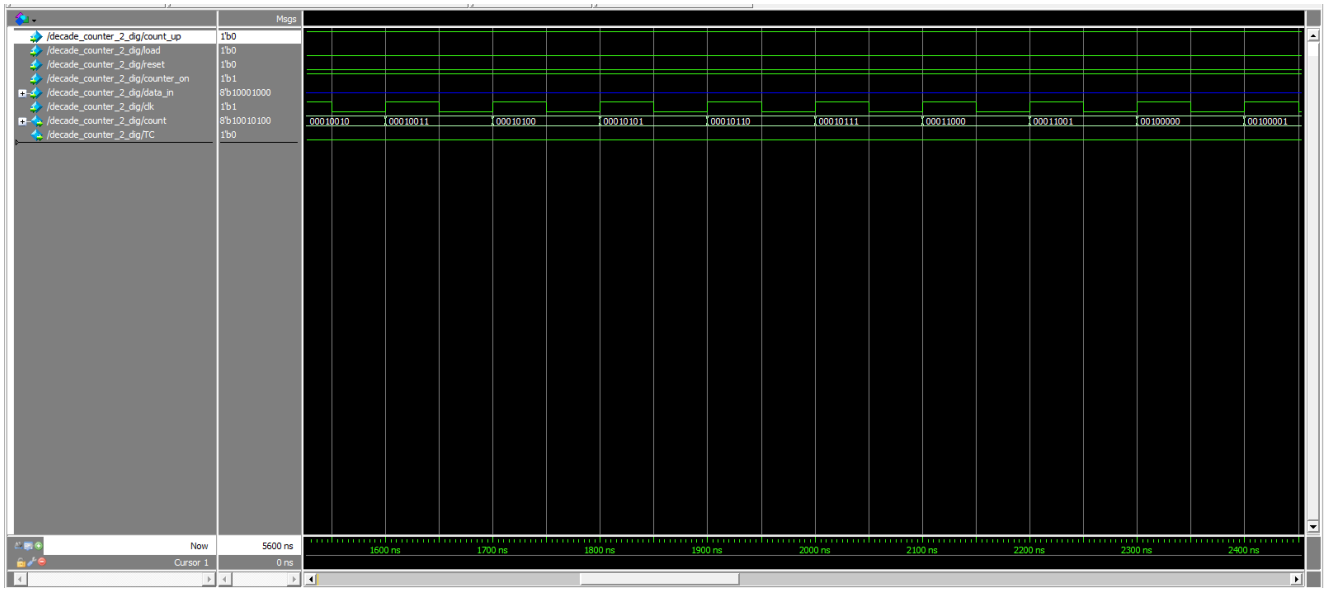
2. Verilog code for two-digit decade counter

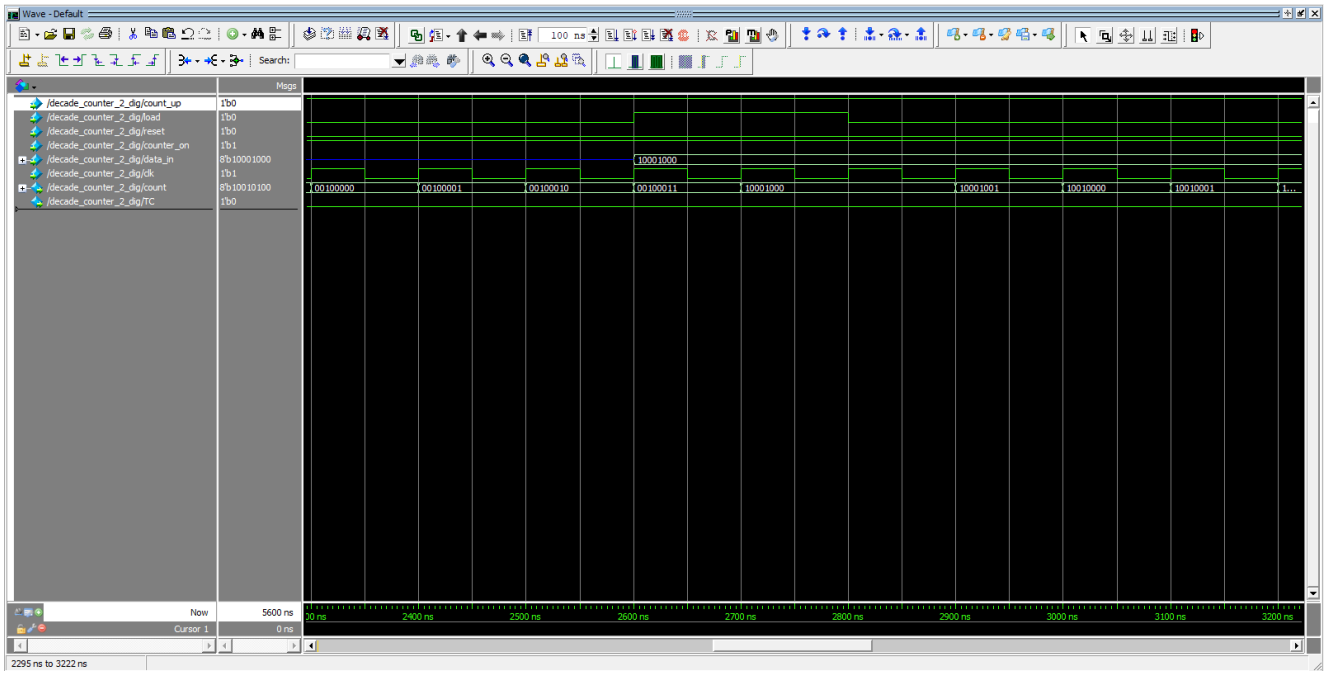
Verilog code

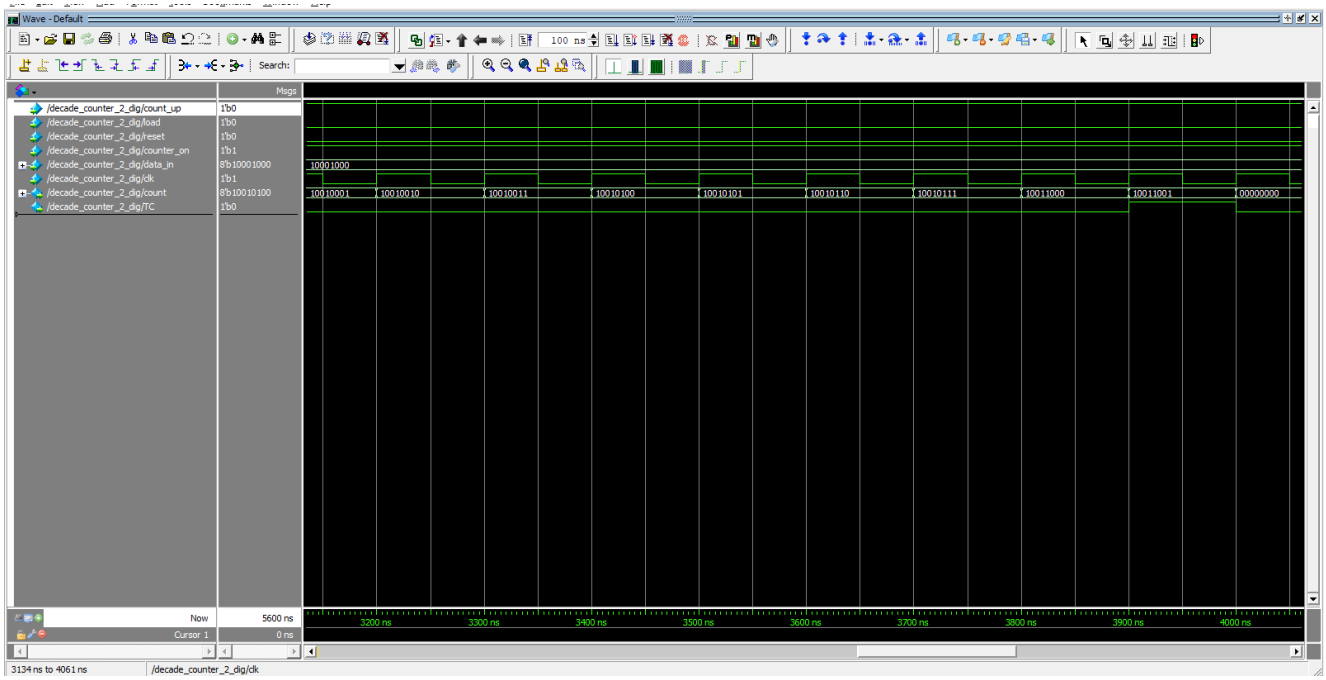
```
module decade_counter_2_dig(
    input count_up,
    input load,
    input reset,
    input counter_on,
    input [7:0]data_in,
    input clk,
    output reg [7:0]count,
    output TC
);

    wire tc_int;
    decade_counter
lsn(count_up,load,reset,counter_on,data_in[3:0],clk,count[3:0],tc_int);
    decade_counter
msn(count_up,load,reset,tc_int,data_in[7:4],clk,count[7:4],TC);
endmodule
```

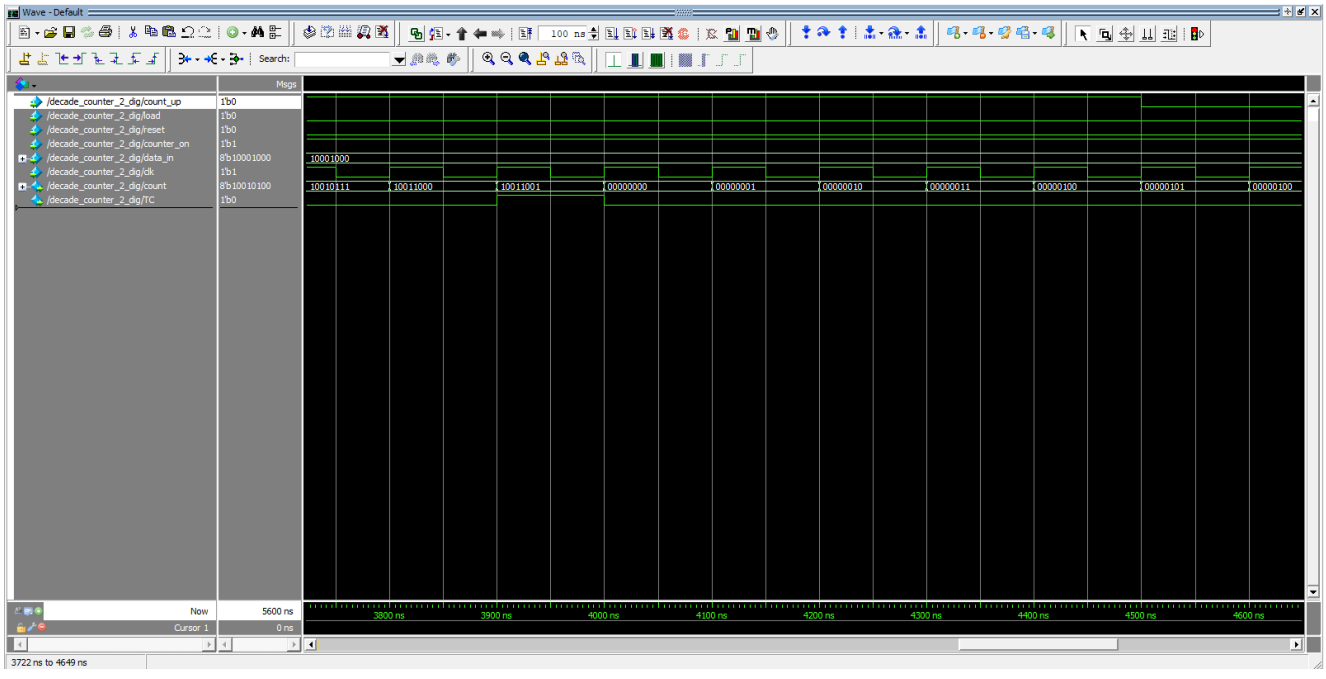
Simulation results

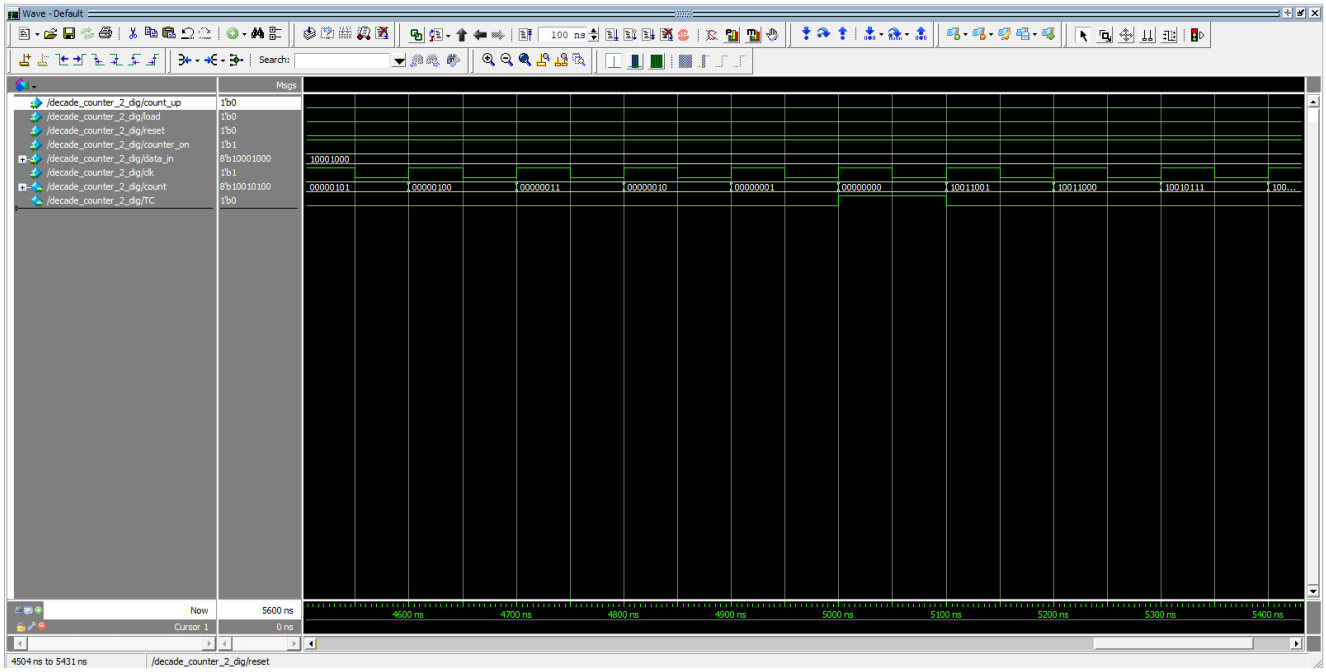



Msgs
/decade_counter_2_dig/count_up
/decade_counter_2_dig/load
/decade_counter_2_dig/reset
/decade_counter_2_dig/counter_on
/decade_counter_2_dig/data_in
/decade_counter_2_dig/clk
/decade_counter_2_dig/count
/decade_counter_2_dig/TC
1'b0
1'b0
1'b0
1'b1
8'b10001000
1'b1
8'b10010100
1'b0
00010010
00010011
00010100
00010101
00010110
00010111
00011000
00011001
00100000
00100001
Now
5600 ns
Cursor 1
0 ns
1600 ns
1700 ns
1800 ns
1900 ns
2000 ns
2100 ns
2200 ns
2300 ns
2400 ns


Wave - Default
Search:
Msgs
/decade_counter_2_dig/count_up
/decade_counter_2_dig/load
/decade_counter_2_dig/reset
/decade_counter_2_dig/counter_on
/decade_counter_2_dig/data_in
/decade_counter_2_dig/clk
/decade_counter_2_dig/count
/decade_counter_2_dig/TC
1'b0
1'b0
1'b0
1'b1
8'b10001000
1'b1
8'b10010100
1'b0
10001000
00100000
00100001
00100010
00100011
10001000
10001001
10010000
10010001
Now
5600 ns
Cursor 1
0 ns
2400 ns
2500 ns
2600 ns
2700 ns
2800 ns
2900 ns
3000 ns
3100 ns
3200 ns
2295 ns to 3222 ns


Wave - Default
Search:
Msgs
/decade_counter_2_dig/count_up
/decade_counter_2_dig/load
/decade_counter_2_dig/reset
/decade_counter_2_dig/counter_on
/decade_counter_2_dig/data_in
/decade_counter_2_dig/clk
/decade_counter_2_dig/count
/decade_counter_2_dig/TC
1'b0
1'b0
1'b0
1'b1
8'b10001000
1'b1
8'b10010100
1'b0
10001000
10010001
10010010
10010011
10010100
10010101
10010110
10010111
10011000
10011001
00000000
Now
5600 ns
Cursor 1
0 ns
3200 ns
3300 ns
3400 ns
3500 ns
3600 ns
3700 ns
3800 ns
3900 ns
4000 ns
3134 ns to 4061 ns
/decade_counter_2_dig/clk


Wave - Default
Search:
Msgs
/decade_counter_2_dig/count_up
/decade_counter_2_dig/load
/decade_counter_2_dig/reset
/decade_counter_2_dig/counter_on
/decade_counter_2_dig/data_in
/decade_counter_2_dig/clk
/decade_counter_2_dig/count
/decade_counter_2_dig/TC
1'b0
1'b0
1'b0
1'b1
8'b10001000
1'b1
8'b10010100
1'b0
10001000
10010111
10011000
10011001
00000000
00000001
00000010
00000011
00000100
00000101
00000100
Now
5600 ns
Cursor 1
0 ns
3800 ns
3900 ns
4000 ns
4100 ns
4200 ns
4300 ns
4400 ns
4500 ns
4600 ns
3722 ns to 4649 ns



FPGA implementation

For the FPGA implementation, we used active-low signals for load and reset, since we implemented using the push button switches, which yield active-low logic.

Top-level modular code

```
module two_digit_bcd_counter(
  input count_up,
  input loadn,
  input resetn,
  input counter_on,
  input [7:0]data_in,
  input clk,
  output TC,
  output [1:0]a,
  output [1:0]b,
  output [1:0]c,
  output [1:0]d,
  output [1:0]e,
  output [1:0]f,
  output [1:0]g
);
```

```
 wire divclk;
 wire [7:0]count;

 clock_divider divide(clk, divclk);
 decade_counter_2_dig dec(count_up, load, resetn, counter_on, data_in,
divclk, count, TC);
 bcd_seven_segment_decoder msn(count[7:4], a[1], b[1], c[1], d[1], e[1],
f[1], g[1]);
 bcd_seven_segment_decoder lsn(count[3:0], a[0], b[0], c[0], d[0], e[0],
f[0], g[0]);

endmodule
```

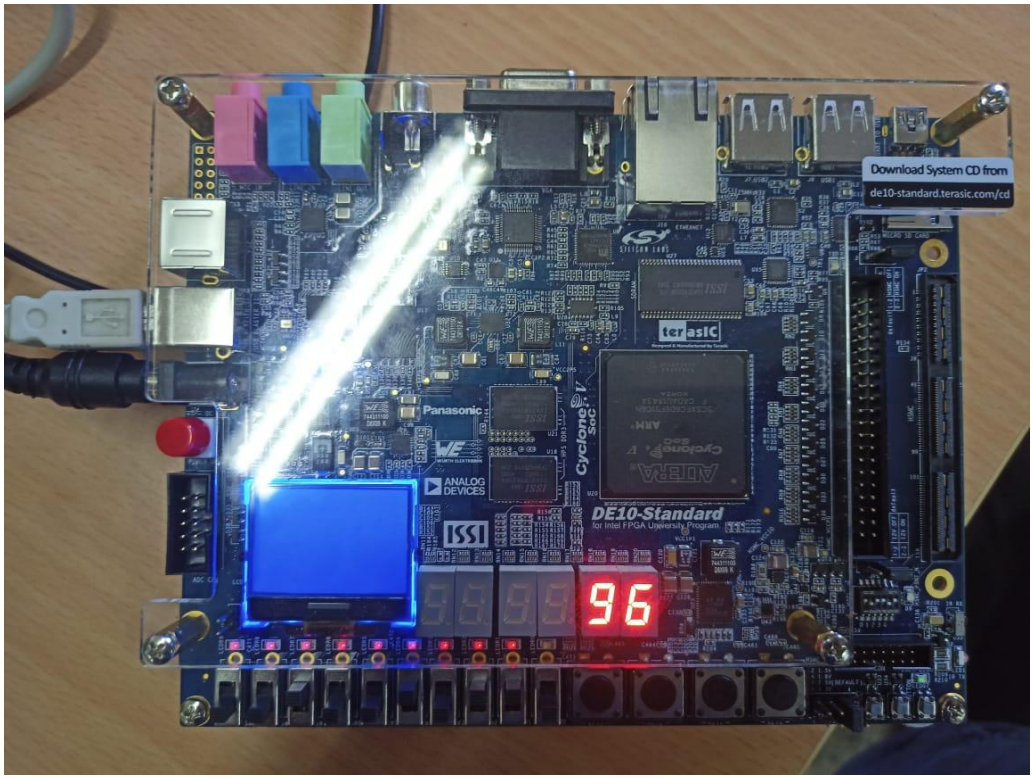
Resource utilization

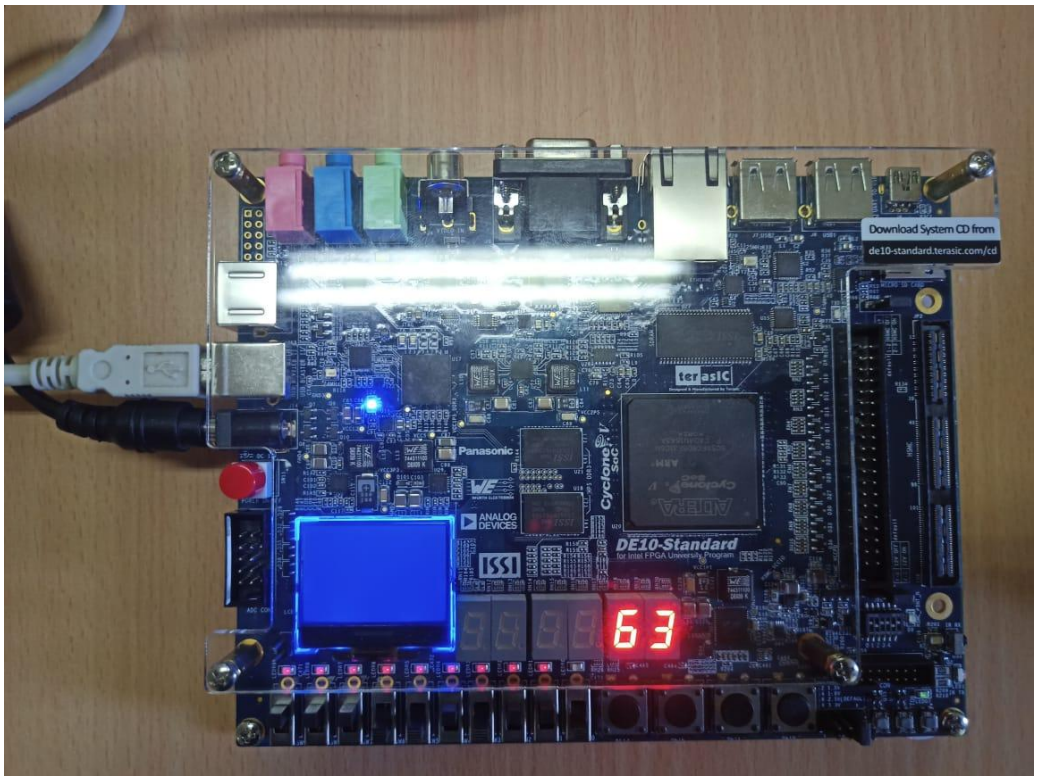
Flow Summary

<<Filter>>

Flow Status	Successful - Wed Oct 4 15:57:53 2023
Quartus Prime Version	21.1.1 Build 850 06/23/2022 SJ Lite Edition
Revision Name	decade_counter
Top-level Entity Name	two_digit_bcd_counter
Family	Cyclone V
Device	5CSXFC6D6F31C6
Timing Models	Final
Logic utilization (in ALMs)	31 / 41,910 (< 1 %)
Total registers	35
Total pins	28 / 499 (6 %)
Total virtual pins	0
Total block memory bits	0 / 5,662,720 (0 %)
Total DSP Blocks	0 / 112 (0 %)
Total HSSI RX PCSs	0 / 9 (0 %)
Total HSSI PMA RX Deserializers	0 / 9 (0 %)
Total HSSI TX PCSs	0 / 9 (0 %)
Total HSSI PMA TX Serializers	0 / 9 (0 %)
Total PLLs	0 / 15 (0 %)
Total DLLs	0 / 4 (0 %)

Implementation Snapshots:





Link to the Simulation Video