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Investigating the Correlation Between Space Charge Modulation and ON-State Breakdown in Multiple RESURF DeMOS Devices

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ABSTRACT In this work, the ON-state performance of the drain-extended metal-oxide-semiconductor (DeMOS) device with multiple RESURF junctions in the drift region is explored. Although the additional RESURF implant offers a significant improvement in the breakdown voltage (V_{BD}) and ON-resistance (R_{ON}) compared to the conventional DeMOS, it induces an early space charge modulation (SCM) initiated quasi-saturation (QS) effects and adversely impacts the ON-state breakdown of the device. Moreover, these devices are compared for a fixed breakdown voltage where a correlation between their analog/RF performance and QS effects is established. This work also presents and validates the design guideline for multiple RESURF devices that can alleviate the SCM/QS effects by 8% and improve the ON-state breakdown voltage by 35% compared to the standard device, thereby maximizing the ON-state performance of the device without compromising the OFF-state breakdown.

INDEX TERMS Drain extended MOS (DeMOS), double RESURF, triple RESURF, space charge modulation (SCM), quasi-saturation (QS), ON-state breakdown.

I. INTRODUCTION

Owing to the increase in the popularity of integrated circuit (IC) technology, there has been a constant thrust towards the integration of power transistors such as drain-extended metal-oxide-semiconductor (DeMOS) along with standard complementary MOS (CMOS) devices for compact design, low cost, and high voltage/high power performance. These devices are required in the voltage range of 20V-100V for smart power applications, for example, display drivers, dc-dc converters, automotive, and high-voltage telecommunication [1]–[5]. DeMOS transistors, as shown in Figure 1(a), use the reduced surface field (RESURF) concept, where the surface electric field is optimized by charge compensation between the lightly doped N-type drift region and the P-well and P-substrate regions [6]. This maximizes the device OFF-state breakdown voltage (V_{BD}) while minimizing the ON-resistance (R_{ON}) [7]. However, improving the tradeoff between V_{BD} and R_{ON} has always been a challenge for which several device designs and concepts such as split triple-gate, lateral trench, and integrated diodes in accumulation mode techniques have been reported [8]–[10]. A shallow trench isolation (STI) technique in the drift region greatly reduces the high electric fields near the gate to enhance the V_{BD}; however, the ON-resistance increases simultaneously [2]. A highly doped p-type implant in the N-well drift region, which forms multiple RESURF junctions, is reported to significantly improve the R_{ON} while maintaining high a V_{BD} [11], [12] For the same reason, these devices are being examined for switching applications [13]–[18].

DeMOS devices are often required to be biased at high drain voltages to sustain high current conditions where they conduct with increased carrier density across a lightly doped drift region, giving rise to space charge modulation (SCM) [19]–[22]. Under high current conditions, the carrier density in the drift region exceeds the background doping, and the peak electric field shifts from the gate edge to the drain edge of the device, leading to mobility degradation near the

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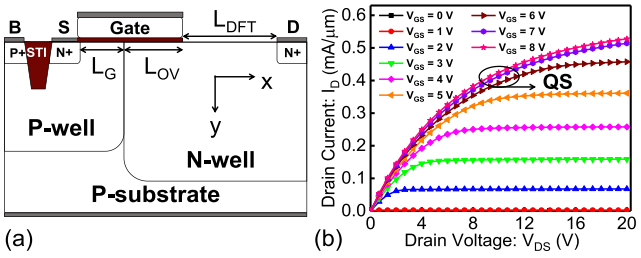

FIGURE 1. (a) Schematic of single RESURF (conventional) DeMOS device with design parameters as L_G: Channel Length, L_{OV}: Gate to N-well Overlap Length, and L_{DFT}: Drift Region Length. (b) Output (I_D-V_{DS}) characteristics of DeMOS depicting the quasi-saturation (QS) effects at high drain and gate voltages.

drain diffusion [23]. This effect is frequently ascribed to the onset of quasi-saturation (QS), where the drain current (I_D) becomes dependent on the drain voltage (V_{DS}) at a high gate voltage (V_{GS}), as depicted in the I_D-V_{DS} curve in Figure 1(b). This phenomenon adversely affects the transconductance (g_m) and limits further R_{ON} reduction with any change in gate voltage, which critically influences the device performance in analog/RF applications [24], [25].

In literature, various device designs to improve R_{ON} and g_m such as dual-gate, source-underlap, and adaptive RESURF and hybrid source techniques have been reported [26]–[28]. However, an in-depth understanding of the fundamental physics involved towards the onset of SCM as well as QS in the multiple RESURF (double, and triple) devices is rather limited. Also, the impact of multiple RESURF implant on the ON-state device performance while proposing design guidelines for mitigating SCM/QS effects is missing in the earlier works and requires proper investigation. This study attempts to fill the gap by developing a deep insight into the ON-state behavior of DeMOS device in the presence of multiple RESURF implants. Furthermore, it presents the correlation between the SCM and ON-state breakdown in the multiple RESURF based non-conventional DeMOS devices, which limits its capability in analog/RF applications and impacts its safe operating area.

II. DEVICE DESIGN AND SIMULATION SETUP

In this work, the single RESURF (conventional) DeMOS device (Figure 1(a)) is designed over a calibrated setup already reported by our group, which is optimized to offer highest breakdown voltage for the least ON-resistance [23]. As shown in Fig. 2, the multiple RESURF devices have the same layout footprint as the conventional DeMOS. These devices are designed by burying a highly doped P-type implant (P-Top) in the lightly doped N-type drift region. The key P-Top implant design parameters i.e., doping (N_{Ptop}), position in the drift region (D_{Ptop}), and distance from the gate edge (L_{PG}) and drain edge (L_{PD}), as summarized in Table 1, were optimized to achieve maximum V_{BD} for minimum R_{ON}. Figure 3 illustrates the trade-off between the R_{ON} and V_{BD}in different DeMOS devices. The data points

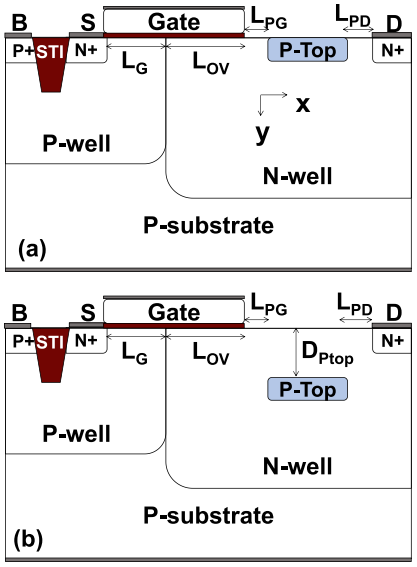

FIGURE 2. 2-D cross-section of multiple RESURF based DeMOS devices. (a) Double RESURF, and (b) Triple RESURF. RESURF implant (P-Top) design parameters include its doping (N_{Ptop}), position (D_{Ptop}), and its distance from the gate (L_{PG}) and drain (L_{PD}).

TABLE 1. Device design parameters.

Devices	T_{OX} (nm)	L_G (μm)	L_{OV} (μm)	L_{DFT} (μm)	N_{Ptop} (cm^{-3})	D_{Ptop} (μm)	L_{PG} (μm)	L_{PD} (μm)
Single RESURF	10	2.7	3.2	4	-	-	-	-
Double RESURF	10	2.7	3.2	4	6×10^{17}	0	0.1	1
Triple RESURF	10	2.7	3.2	4	6×10^{17}	0.3	0.05	0.8

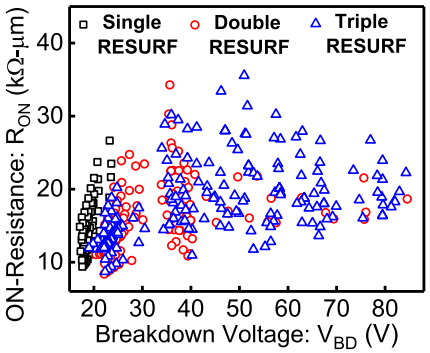

FIGURE 3. Trade-off between OFF-state breakdown voltage (V_{BD}) and ON-resistance (R_{ON}) in single (conventional), double and triple RESURF DeMOS devices for a range of P-Top implant design parameters i.e., doping, $N_{Ptop} = 4 \times 10^{17}$ to 8×10^{17} cm^{-3}; position, $D_{Ptop} = 0.1$ to 0.5 μm; and distance from the drain, $L_{PD} = 0.5$ to 1.5 μm at $V_{GS} = 5$ V and $V_{DS} = 10$ V.

for single RESURF DeMOS are generated for different drift region doping and drift region length (L_{DFT}), whereas the abovementioned P-Top implant design parameters are varied to obtain data points for multiple RESURF DeMOS devices. It should be noted that the chosen design parameter of these

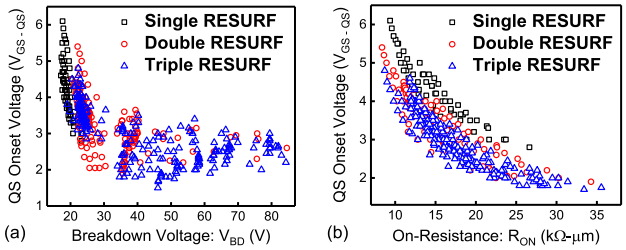

FIGURE 4. Trade-off between quasi-saturation (QS) onset voltage (V_{GS-QS}) and (a) OFF-state breakdown voltage (V_{BD}), and (b) ON-resistance (R_{ON}) for multiple DOE in single, double, and triple RESURF DeMOS devices. Data is extracted at $V_{GS} = 5$ V and $V_{DS} = 10$ V. The extraction of data points for comparison has been mentioned in the Section II.

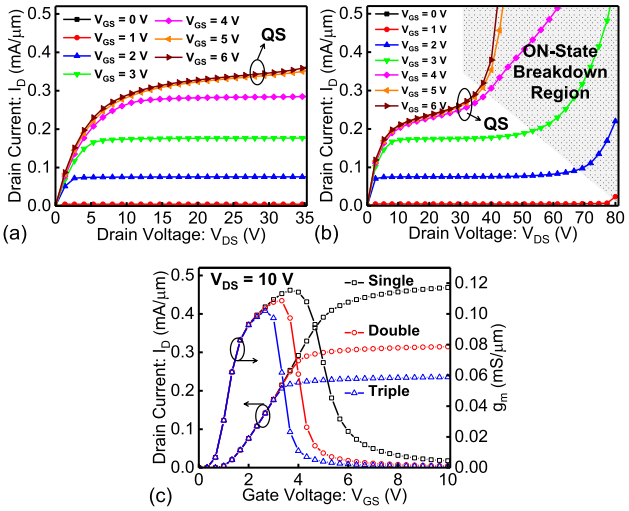

FIGURE 5. Output (I_D-V_{DS}) characteristics of (a) double, and (b) triple RESURF DeMOS, for multiple gate voltages (V_{GS}). (c) Comparison of I_D-V_{GS} and g_m-V_{GS} behaviors of single, double, and triple RESURF devices at $V_{DS} = 10$ V. The onset of ON-state breakdown (BV_{ON}) is indicated in (b).

devices is varied by keeping other parameters constant at values mentioned in Table 1. V_{BD} is obtained by current injection method at $V_{GS} = 0$V and R_{ON} is extracted at $V_{DS} = 0.1$V and $V_{GS} = 5$V. The dose of the P-Top implant was chosen to achieve enhanced depletion of N-well by the action of three regions: P-well, P-substrate, and P-Top implant. Thus, multiple RESURF DeMOS devices offer better OFF-state characteristics than conventional DeMOS devices. The device performance was examined using a well-calibrated Sentaurus TCAD framework [29]. TCAD models used to capture the physical behavior of the device include carrier-carrier scattering and doping-dependent mobility models, high field velocity saturation models, Shockley-Read-Hall (SRH) and Auger carrier recombination models, and avalanche (UniBo2) generation models.

III. RESULTS AND DISCUSSION

The trend of the QS-onset voltage (V_{GS-QS}) as a function of V_{BD} and R_{ON} is shown in Figures 4(a) and 4(b), respectively. V_{GS-QS} is the gate voltage at which the device encounters quasi-saturation effects. It can be noted from Figure 4(a) that the higher breakdown devices suffer the most from quasi-saturation with an early onset, whereas lower breakdown devices show high input voltage tolerance. Furthermore, the devices with lower R_{ON} in Figure 4(b) tend to have QS onset at higher gate voltages and higher R_{ON} devices show early onset of QS. In summary, V_{GS-QS} is shown to degrade for devices with higher V_{BD} and R_{ON}, and vice versa.

A. DC PERFORMANCE

The output characteristics of the double and triple RESURF DeMOS devices are shown in Figures 5(a) and 5(b), respectively. For the same layout footprint, the multiple RESURF devices offer high voltage blocking capability, allowing higher voltages at the drain terminal compared to the conventional DeMOS device. However, these devices are more prone to SCM/QS effects when operating in the ON-state. Under high-current conditions, like the conventional DeMOS device, when the free carriers injected by the channel into the drift region exceed the background doping of the lightly doped N-type drift region, the space charge density across the reverse bias P-N (P-well – N-drift) junction is disturbed. As a result, the peak electric field shifts from the gate edge and confines close to the drain edge. Furthermore, the presence of highly doped P-Top implant in the lightly doped drift region (depending on the position of the P-Top implant) strengthens the intensity of the localized electric field at the drain edge and triggers the onset of SCM/QS effects at lower gate voltages compared to the conventional DeMOS device. As evident from Figure 5(c), the triple RESURF device shows early onset of QS with maximum g_m-reduction, since the QS-onset occurs at the gate voltage where g_m significantly degrades [24]. The slope of the g_m roll-off suggests the severity of the QS effects in the triple RESURF DeMOS compared to the other variants. The ON-state performance of the multiple RESURF DeMOS devices is discussed in detail below.

1) DOUBLE RESURF DEMOS ($D_{PTOP} = 0$)

For V_{GS}up to 3V, the depletion region under the gate and the P-Top implant allows the sharing of the electric field while restricting the current conduction area in the drift region, as shown in Figures 6(a) and 6(b). It is worth noting that since the P-Top implant is at the surface, the charge carriers travel through the path below this implant in the double RESURF, which increases the R_{ON} by ∼20% than the single RESURF device. It can be seen in Figure 6(c) that as V_{GS} increases, the depletion region at the P-well to N-well junction becomes narrow and that under the gate to N-well overlap region shifts to the P-Top to drain junction, extending more towards the drain contact. As a result, the electric field tends to reallocate towards the drain. An increase in V_{GS} improves the channel conductivity, injecting the more carriers into the drift region, which increases the current conduction area (Figure 6(d)). With further increase in V_{GS}, the electric field strengthens

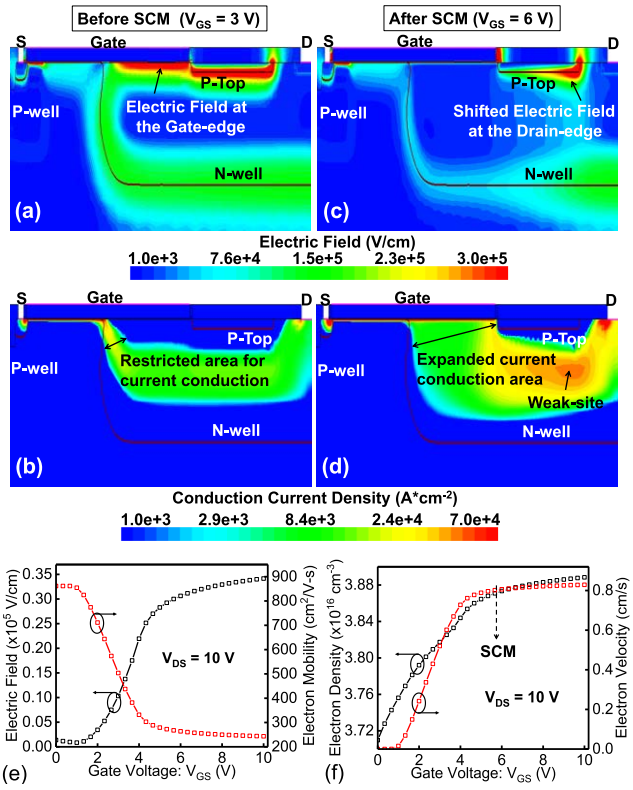

FIGURE 6. Electric field distribution and conduction current density (a), (b) before SCM captured at V_{GS} = 3 V, and (c), (d) after SCM captured at V_{GS} = 6 V, respectively in double RESURF DeMOS. (e) Electric field and electron mobility, and (f) electron density and velocity as a function of gate voltage (V_{GS}). Data is extracted by probing the weak site under the P-Top implant at V_{DS} = 10 V.

near the drain contact and the charge carriers drift with the maximum velocity. Consequently, a weak site (high-intensity electric field) is created under the P-Top implant towards the drain contact, embarking on the onset of SCM (Figure 6(d)). The weak site is probed to show that a higher electric field prevails near the drain at high V_{GS}, severely degrading the carrier mobility (Figure 6(e)). Even though the carriers have reached the maximum velocity, the electron density continues to rise, increasing the current density (Figure 6(f)).

2) TRIPLE RESURF DEMOS (D_{PTOP} = 0.3 μM)

The electric field distribution and conduction current density in the triple RESURF DeMOS before SCM (i.e., $V_{GS} \leq 3V$) are depicted in Figures 7(a) and 7(b), respectively, whereas those after SCM ($V_{GS} \geq 5V$) are shown in Figures 7(c) and 7(d), respectively. For a small V_{GS}, the device behaves like the double RESURF. The electric field is concentrated under the gate to N-well overlap region and across the P-Top implant (Figure 7(a)). The current conduction area is confined below the P-Top implant as it creates a wider depletion effect in the drift region, further increasing the R_{ON} of the device (Figure 7(b)). As V_{GS} increases, the peak electric field shifts from the gate edge to the drain edge, as shown in Figure 7(c). Since the depletion width decreases with increasing V_{GS} and the increased channel conductivity increases excess carrier injection in the drift region, the current conduction area increases in the drift region. Here, the P-Top implant position allows a dual-conduction path for carriers in the drift region [30]. Due to the retrograde doping of the N-well, the depletion region across the P-Top implant extends more towards the surface, leaving a narrow conduction path above the P-Top implant. The P-Top implant compels a considerable fraction of current to conduct through the surface in the drift region, which causes the carriers to localize at the P-Top implant to the drain junction (denoted by Site-A in Figure 7(d)). The surface conduction causes a significant current crowding near the drain, which is attributed to the early onset of SCM. The electric field profile, net doping, and electron density as an effect of SCM are shown in Figure 7(e). After SCM has occurred, a steep rise in the lateral electric field occurs at the drain contact. The high lateral electric field at drain triggers an excessive carrier generation owing to avalanche multiplication. This, in turn, increases the current density in the drift region, leading to high impact ionization near the drain edge (inset: Figure 7(d)), which severely degrades the ON-state breakdown of the device (BV_{ON}) (Figure 4(b)).

Figure 8(a) shows that on SCM triggering, intense carrier crowding causes a rapid increase in the peak electric field and charge carrier mobility degradation. Figure 8(b) shows a steady increase in the electron density for low V_{GS}, whereas at voltage near QS-onset, the electron density increases suddenly, depicting the intensity of QS in the triple RESURF DeMOS device. Moreover, the electron density continues to increase despite drift velocity saturation, contributing to a high current density.

B. DESIGN GUIDELINES

A careful strategy for optimizing the design parameters is an important requirement of RESURF technology. The triple RESURF DeMOS device suffers the most from early SCM/QS while offering the best OFF-state characteristics. For triple RESURF, the design of experiments (DOE) includes key parameters such as P-Top implant doping (N_{Ptop}), position in the drift region (D_{Ptop}), and its distance from the drain-edge (L_{PD}). The guidelines shown here can be used independently or in combination to mitigate SCM/QS effects. The P-Top implant design parameters are varied while keeping the same layout footprint as the conventional DeMOS device. Table 2 summarizes the behavior of the OFF-state breakdown (V_{BD}), ON-resistance (R_{ON}), QS-onset voltage (V_{GS-QS}), and ON-state breakdown (BV_{ON}) for different N_{Ptop}, D_{Ptop}, and L_{PD} values, where the standard triple RESURF parameters are highlighted in bold.

1) DOPING OF THE P-TOP IMPLANT: N_{PTOP}

The change in the electric field distribution for N_{Ptop} with lower value (4×10^{17}cm^{-3}) and higher value (8×10^{17}cm^{-3}) are shown in Figures 9(a) and 9(b), respectively. It should be noted that increasing the doping of the P-Top implant

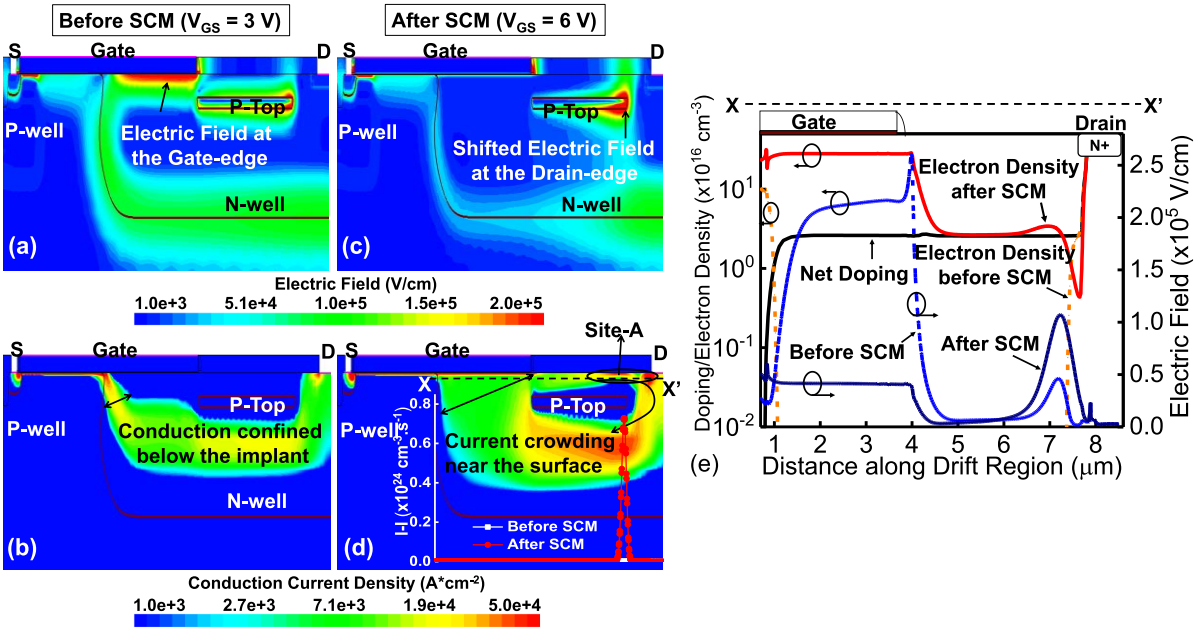

FIGURE 7. Electric field distribution and conduction current density (a), (b) before SCM captured at V_{GS} = 3 V, and (c), (d) after SCM captured at V_{GS} = 6 V, respectively in triple RESURF DeMOS. Inset: Impact ionization (I-I) along the cut X-X′ in (d). (e) Net doping concentration, electric field, and electron density along the cut X-X′ in the drift region, depicting onset of space charge modulation in the triple RESURF DeMOS.

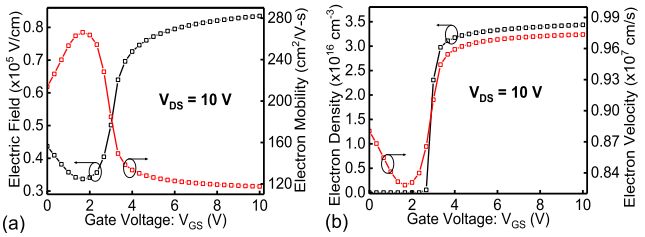

FIGURE 8. (a) Electric field and electron mobility, and (b) electron density and electron velocity as a function of gate voltage (V_{GS}) near the drain edge at Site-A, where SCM occurs in triple RESURF DeMOS.

TABLE 2. Performance of triple RESURF DeMOS device for different P-Top implant design parameters.

Parameters	Values	V_{BD} (V)	R_{ON} (KΩ-μm)	V_{GS-QS} (V)	BV_{ON} (V)
N_{Ptop}	4 x 10^{17} cm^{-3}	24.45	15.88	4.0	42
	5 x 10^{17} cm^{-3}	28.11	16.05	3.7	38
	6 x 10^{17} cm^{-3}	**79.47**	**16.39**	**3.6**	**34**
	7 x 10^{17} cm^{-3}	49.88	16.68	3.54	30
	8 x 10^{17} cm^{-3}	36.79	16.85	3.46	28
D_{Ptop}	0.1 μm	38.73	15.69	4.0	32
	0.2 μm	49.37	16.96	3.8	29
	0.3 μm	**79.47**	**16.39**	**3.6**	**34**
	0.4 μm	75.42	16.04	3.5	32
	0.5 μm	68.02	15.92	3.4	31
L_{PD}	0.5 μm	70.82	16.90	3.55	24
	0.8 μm	**79.47**	**16.39**	**3.6**	**34**
	1.0 μm	78.76	16.12	3.65	38
	1.2 μm	78.38	15.89	3.75	42
	1.5 μm	74.90	15.56	3.9	46

also increases its thickness as it is buried deep in the N-well region. Figure 9(a) shows that when the P-Top implant is lightly doped, the depletion region is confined to the P-Top implant boundary. As the implant doping increases, the peak electric field at the P-Top edge near the drain increases because the depletion region spreads towards the drain terminal, as shown in Figure 9(b). Thus, R_{ON} degrades by ∼6% when N_{Ptop} increases from $4 \times 10^{17}cm^{-3}$ to $8 \times 10^{17}cm^{-3}$ since the effective cross-sectional area of the N-well region shrinks. Also, V_{BD} increases until $N_{Ptop} = 6 \times 10^{17}cm^{-3}$, where the device achieves optimum dose balance, after which the device breakdown degrades, as shown in Table 2. Moreover, on increasing V_{DS} in higher N_{Ptop} devices, the electrons gain high energy to become ''hot electrons'' and cause avalanche multiplication, leading to impact ionization. Thus, increasing N_{Ptop} shifts the QS-onset to ∼14% lower gate voltage, and a significant current crowding near the drain degrades the BV_{ON} by ∼33%. Thus, N_{Ptop} can be optimized considering that lower implant doping improves the ON-state performance at the expense of OFF-state breakdown.

2) DEPTH/POSITION OF THE P-TOP IMPLANT: D_{PTOP}

The triple RESURF device performance is highly dependent on the depth/position of the P-Top implant (D_{Ptop}) in the drift region. The conduction current density for $D_{Ptop} = 0.1\mu m$ and $D_{Ptop} = 0.5\mu m$ is shown in Figures 10(a) and 10(b), respectively. For smaller D_{Ptop}, the current conduction takes place via the path underneath the P-Top implant, like double RESURF (Figure 10(a)). At this point, the R_{ON} and V_{BD} were low because the conduction path in the drift region was shorter and the P-Top implant was closer to the surface, which could not deplete the deep N-well, respectively.

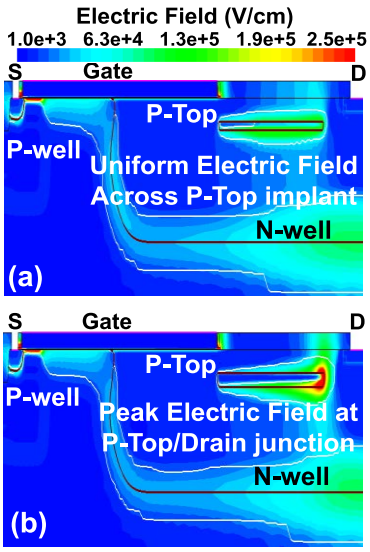

FIGURE 9. Electric field distribution versus P-Top implant doping (N_{Ptop}) in triple RESURF DeMOS, where (a) $N_{Ptop} = 4 \times 10^{17}$ cm^{-3}, and (b) $N_{Ptop} = 8 \times 10^{17}$ cm^{-3}, extracted at $V_{GS} = 5$ V and $V_{DS} = 10$ V.

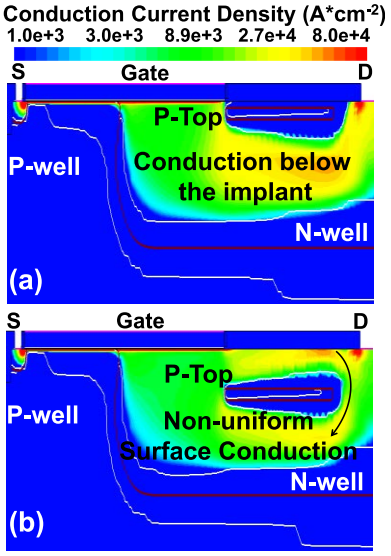

FIGURE 10. Conduction current density as a function of P-Top implant position in the drift region (D_{Ptop}) of triple RESURF DeMOS, where (a) $D_{Ptop} = 0.1$ μm, and (b) $D_{Ptop} = 0.5$ μm at $V_{GS} = 5$ V and $V_{DS} = 10$ V.

As shown in Table 2, on increasing D_{Ptop}, V_{BD} improves until $D_{Ptop} = 0.3\mu$m where the N-well is fully depleted; however, R_{ON} degrades as the P-Top implant occupies a broader area in the N-well region. Now, most of the current is conducted through the surface, resulting in a severe current crowding near the drain contact. Figure 10(b) shows that for larger D_{Ptop}, the surface conduction by the majority charge carriers defies the dual-path conduction phenomenon [30]. As most of the current is conducted through the shortest path i.e., above the P-Top implant, the R_{ON} of the device with a larger D_{Ptop} improves. However, the V_{BD} of the device degrades because the peak electric field at the gate to

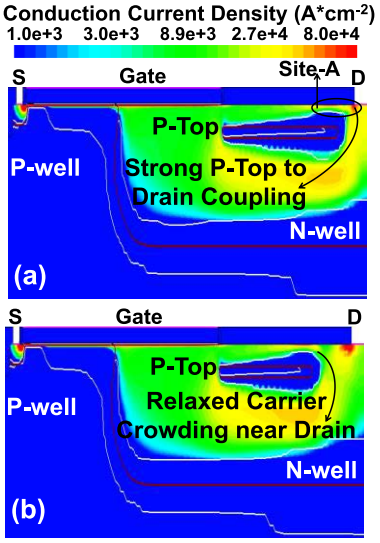

FIGURE 11. Conduction current density as a function of P-Top implant distance from the drain edge (L_{PD}) in the triple RESURF DeMOS, where (a) $L_{PD} = 0.5$ μm, and (b) $L_{PD} = 1.2$ μm at $V_{GS} = 5$ V and $V_{DS} = 10$ V.

N-well edge approaches the critical electric field. Moreover, Figure 10(b) shows that owing to non-uniform current conduction in the drift region, the QS-onset voltage degrades by ∼18%, further decreasing the BV_{ON} of the device with a larger D_{Ptop}.

3) DISTANCE OF THE P-TOP IMPLANT FROM DRAIN-EDGE: L_{PD}

Figures 11(a) and 11(b) show the conduction current density as a function of P-Top implant distance from the drain contact (L_{PD}) where L_{PD} is 0.5μm and 1.2μm, respectively. As shown in Figure 11(a), for a small L_{PD}, the P-Top implant and the drain establish a strong electric field confined to the Site-A (P-Top to drain junction), severely affecting the carrier mobility in this region. At this point, g_m degrades sharply due to the high impact ionization near the drain. As the L_{PD} increases (Figure 11(b)), the electric field shifts with the edge of the P-Top implant away from the drain, weakening the localized impact ionization. This results in a relaxed carrier crowding at the drain contact, substantially improving the R_{ON} by ∼8% when the L_{PD} is increased from 0.5μm to 1.2μm. It is worth mentioning that by optimizing the L_{PD}, approximately the same V_{BD} can be maintained while improving the R_{ON} of the device, as shown in Table 2. Moreover, the QS-onset is delayed by ∼10% and BV_{ON} shows a significant improvement of ∼75% with increasing L_{PD}. However, with a further increase in the L_{PD}, the OFF-state breakdown degrades due to inadequate space charge distribution in the drift region.

C. ANALOG/RF PERFORMANCE

This section explores the analog and RF performances of the multiple RESURF DeMOS devices while comparing with the conventional single RESURF DeMOS. For comparison,

TABLE 3. Set of devices with common breakdown voltage (V_{BD}). (Reference device is mentioned in Table 1).

Sets	N_{Drift}	L_{DFT}
Set-A (Double and Triple RESURF DeMOS)	(4 to 6) × 10^{12} cm^{-2} (increased)	4 μm (constant)
Set-B (Double and Triple RESURF DeMOS)	(4 to 6) × 10^{12} cm^{-2} (increased)	< 4 μm (decreased)

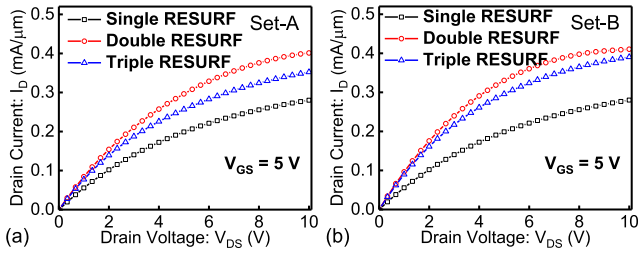

FIGURE 12. Output (I_D-V_{DS}) characteristics comparison of (a) Set-A, and (b) Set-B devices for V_{GS} = 5 V.

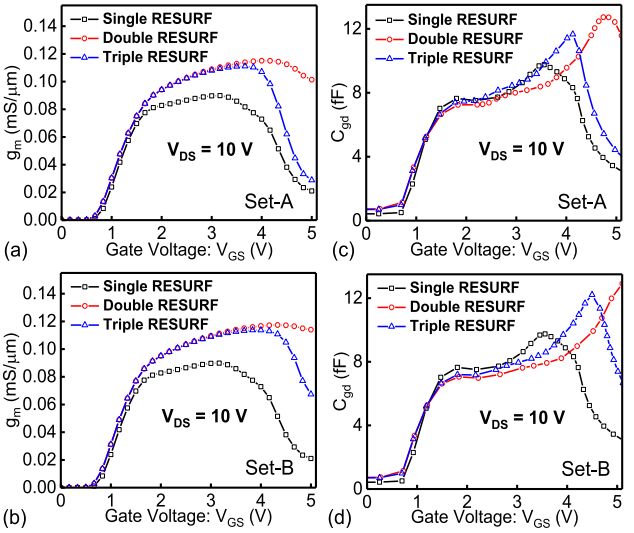

FIGURE 13. Comparison of transconductance (g_m) and Miller capacitance (C_{gd}) as a function of gate voltage (V_{GS}) for (a), (c) Set-A, and (b), (d) Set-B, respectively at V_{DS} = 10 V.

the multiple RESURF devices are optimized for a common breakdown voltage by defining two unique sets, Set-A and Set-B, as shown in Table 3. Set-A consists of devices in which a common V_{BD} is achieved by increasing the N-well doping (N_{Drift}) while keeping all other parameters constant; Set-B includes devices in which N_{Drift} is increased while simultaneously scaling L_{DFT} to achieve common V_{BD}.

Figures 12(a) and 12(b) show the I_D-V_{DS} characteristics of the Set-A and Set-B devices, respectively. For Set-A, double RESURF DeMOS shows a better electrical characteristics than the triple RESURF due to well-distributed current in the drift region. Moreover, the double RESURF device shows ∼43% increase in the ON-current (I_{ON}), whereas the triple RESURF device offers ∼26% higher I_{ON} compared to the conventional DeMOS. This is because, increasing N_{Drift} in the double RESURF device allows charge carriers to flow evenly in the drift region, whereas the depletion region across the P-Top implant in the triple RESURF DeMOS leaves a narrow path for surface conduction, resulting in carrier crowding near the drain. For Set-B, the double and triple RESURF DeMOS devices show ∼47% and ∼40% improvement in the I_{ON}, respectively, which is even higher than that of the Set-A devices.

The important intrinsic parameters that define the analog performance and frequency response of the DeMOS devices are the transconductance (g_m) and Miller capacitance (C_{gd}). All the devices exhibit QS behavior, which can be seen from the deterioration of g_m. When these devices enter QS, the slope of the g_m roll-off becomes directly dependent on the intensity of QS. The transconductance (g_m) versus gate voltage characteristics for Set-A and Set-B is compared in Figures 13(a) and 13(b), respectively. Both, double and triple RESURF devices offer ∼30% higher g_m than the conventional DeMOS in Set-A and Set-B, attributed to increased N-well doping. Moreover, Set-B devices offer extended gate voltage swing, since L_{DFT} directly influences the QS effects in DeMOS devices. Because of its inverse relationship with the electric field, a lower L_{DFT} can accommodate a higher electric field for the same V_{DS}. As a result, a higher carrier density is required to screen a higher electric field, for which the gate potential must be increased. Thus, the onset of QS shifts to higher gate voltage, allowing the maximum gate voltage swing required for power RF applications. The double RESURF DeMOS in both sets, Set-A and Set-B, shows the maximum improvement in the allowable gate voltage swing, leading to much-delayed QS. This shows that the triple RESURF DeMOS, due to maximum current crowding near drain, is more susceptible to QS than the double RESURF device.

Figures 13(c) and 13(d) display the Miller capacitance (C_{gd}) as a function of the gate voltage for the Set-A and Set-B devices, respectively. As soon as QS is triggered, excess charge carriers accumulate in the drift region, contributing to the nonlinear behavior of the parasitic capacitance in the device. This nonlinearity results in a sharp peak of the Miller capacitance upon encountering QS. The double RESURF device in both sets shows a larger gate voltage swing compared to the triple RESURF, attributed to the well-distributed current in the drift region. The triple RESURF device exhibits a sharp capacitance peak in both sets as compared to the other variants because of the non-linear electric field distribution near the gate edge under high current conditions. It can also be noted that the larger the gate voltage swing, the higher the parasitic capacitance overshoot in the device.

Figure 14, in principle, shows the manifestation of all the trends discussed thus far. It should be noted that the capacitance C_{gd} has a direct impact on the cut-off frequency (f_T) and maximum oscillation frequency (f_{MAX}) of the device. Figures 14(a) and 14(b) show f_T as a function of the gate voltage for the Set-A and Set-B devices, respectively. As shown,

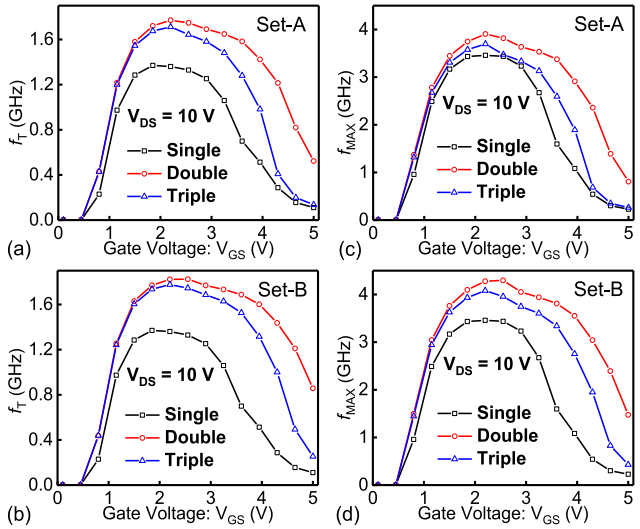

FIGURE 14. Comparison of RF figure-of-merit (FOM) parameters. Transistor cut-off frequency (f_T) and maximum oscillation frequency (f_{MAX}) as a function of gate voltage (V_{GS}) for (a), (c) Set-A, and (b), (d) Set-B, respectively at V_{DS} = 10 V.

the double RESURF DeMOS offers the highest f_T with ∼35% improvement in both device sets. It is worth highlighting that the device that suffers the least from QS shows higher f_T and shifts the fall of f_T to a higher gate voltage, whereas the device that suffers severely from QS shows a lower f_T, which rolls off at a comparatively lower gate voltage. Figures 14(c) and 14(d) show f_{MAX} as a function of gate voltage for the Set-A and Set-B, respectively. As shown, the f_{MAX} response largely depends on the g_m-reduction, Miller capacitance, and f_T of the device, rather than on the QS directly. The multiple RESURF devices show better f_{MAX} response than the conventional DeMOS, and the double RESURF DeMOS in both sets shows the highest f_{MAX} compared to the other variants.

IV. CONCLUSION

The impact of RESURF implant, forming multiple RESURF junctions, on the ON-state device performance is systematically investigated while focusing on the space charge modulation and quasi-saturation effects. The triple RESURF DeMOS device offers a higher OFF-state breakdown voltage; however, it suffers severely from early SCM/QS at high gate voltages. It also experiences an early ON-state breakdown due to high impact ionization at the drain edge, severely impacting the analog and RF performance of the device. However, for a fixed breakdown voltage achieved by optimizing the device design parameters (i.e., N_{Drift}, L_{DFT}), multiple RESURF devices offered up to 47% improvement in I_{ON}, 30% in g_m, 35% in f_T, and 25% in the onset of SCM/QS, compared to the conventional device. A complete device design guideline is also proposed showing that careful placement of the P-Top implant could be a key to minimize the SCM/QS effects while satisfying the OFF-state breakdown requirements.

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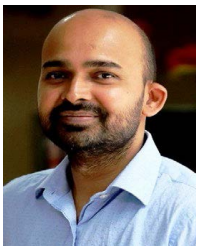

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