EEE 5400 FINAL PROJECT COVER PAGE

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Members worked on the following sections for analysis of the 16nm FinFET Fabrication Process Flow.

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    a. *Introduction*
    b. *Fin Formation*
    c. *Fin Cut*
    d. *Shallow Trench Isolation*

2. **Sushant Rassay**
    a. *Well Formation*
    b. *Dummy Gate Formation*
    c. *Source and Drain Formation*
    d. *NiSi Salicide Formation*

3. **Sujit Desai**
    a. *Replacement Metal Gate (RMG) Deposition*
    b. *Metallization*
    c. *Conclusion*

Analysis of 16nm FinFET Fabrication Process Flow

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***Abstract*—In this paper we report conventional 16nm FinFET fabrication process flow. Different fabrication technologies available and challenges for various steps like lithography, deposition, ion implantation, gate source formation etc. are explained in detail. 16nm node technology is simulated using coventor software.**

Keywords— 16nm node, FinFET, Fabrication technologies, coventor software.

I. Introduction

FinFETs are sub 20nm technology tri gate transistors which are more attractive compared to planar transistors mainly due to reduced area, minimized short channel and electrostatic effects [1]. In CMOS, only one gate controls the source- drain channel and does not have good control of the channel causing leaking currents when the gate is off. Whereas in case of FinFET the channel is thin vertical fin and is fully wrapped on three sides by the gate having completely depleted channel and low leakage. Due to less leakage current FinFETs due to low leakage current, total power required is less and can operate at low voltages with high consistency. Current smallest technology node is 7nm and commercially available from Samsung. In this paper we present 16nm FinFET fabrication process flow where different fabrication steps are explained in detail.

II. Manufactruing Process Flow

A. Fin Formation

1) Lithography:

For high resolution and finite pitch size in 16nm FinFET technology, lithography plays an crucial role. Conventional 193nm lithography has a maximum resolution of 80nm. Extreme UV light lithography at 13.5nm is ideal candidate for next generation IC fabrication compared to 193nm immersion technique but mass production of this system still needs to be achieved [2]. Main challenges with EUV are power source, photo resists and mask [3-4] But further reduction in feature size can using 193nm can be achieved by mainly using two methods i.e. pattern split techniques such as Litho-Litho-Etch (LLE) and Litho-Etch-Litho-Etch (LELE) technique and self-aligned techniques like Self Aligned Double Patterning (SADP) and Self Aligned Quadruple Patterning (SAQP). For 16nm FinFET we currently use Spaced Based Self Aligned Double Patterning technique which is described below:

On a silicon wafer, thermal oxide is grown on which a nitride layer is used as protection layer and is deposited by Low Pressure Chemical Vapor Deposition technique followed by amorphous silicon growth and is used as mandrel layer. Silicon Anti Reflection Coating (SiARC) is deposited on silicon followed by coating of photo resist. Using 193nm immersion

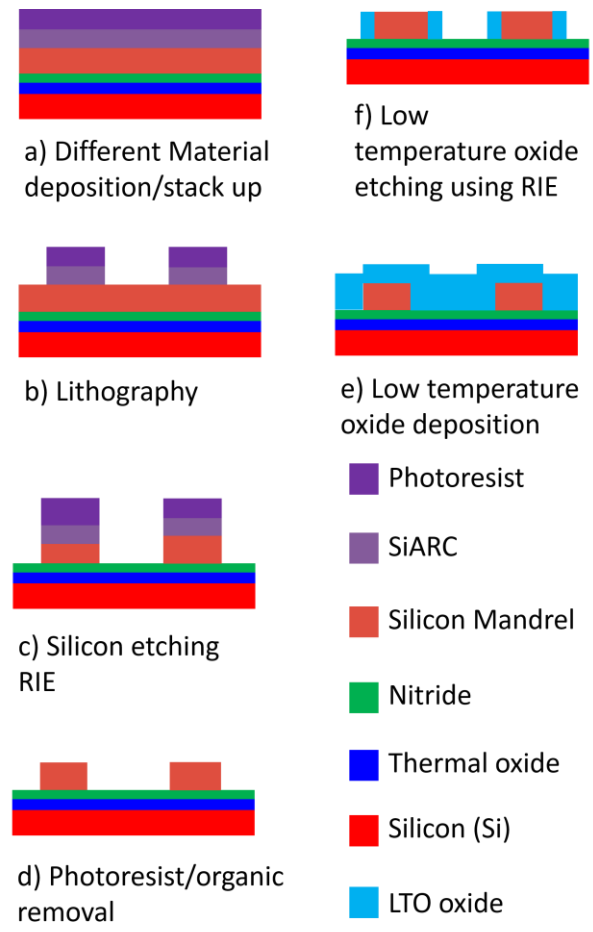


Fig.1. Fin fabrication flow

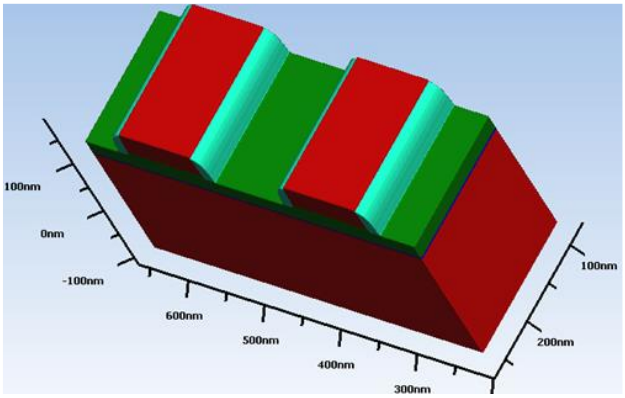


Fig.2. 3D conventor view on simulated spacer with mandrel silicon

lithography pattern is transferred on to mandrel silicon which is later etched using Reactive Ion Etching (RIE). Spacer oxide is

deposited using low temperature process. Using RIE low temperature oxide is removed using RIE everywhere except at spacers. Fabrication steps are given in the figure 1 below. 3D structure of completed fin formation from coventor simulator is shown in fig.2. Complete details of different RIE techniques, oxide and nitride depositions methods are discussed in below sections.

2) Low Pressure Chemical Vapor Deposition of Nitride

Silicon Nitride layer (Si_3N_4) is highly used in FinFET as a barrier layer for impurity ions and oxidation mask. These films are generally deposited using Chemical Vapor Deposition (CVD) technique under dichlorosilane SiH_2Cl_2 and ammonia NH_3. Although these films have high uniformity, they suffer from very high stress greater than 1Gpa. Therefore, low stress films are grown on silicon or silicon oxide using silane SiH4 and NH3 and the residual stress is less than 1000MPa. Stress of the film is reduced if the deposition temperature increases. For instance, at highest temperature 775℃ low stress nitride films of 27Pa are obtained [4].

3) Thermal Oxide Growth:

Thermal oxidation is a way to grow, thin oxide on the surface of the wafer. Oxygen at high temperatures diffuses into the silicon wafer and react to form silicon oxide. The growth of oxide on silicon depends on Deal-Grove model. Thermal oxidation is usually performed at temperatures around $800 - 1200$ ℃ resulting High Temperature Oxide (HTO). The reaction that takes place is:

$$Si + O_2 \rightarrow SiO_2$$

If the reaction occurs in oxygen chamber, then it is known as dry oxidation. Similarly, if water vapor is used for oxide formation then it is known as wet oxidation. Usually for thick oxides, wet oxidation is chosen but fast oxidation creates dangling bonds at the silicon interface and cause leakage current. Chemical reaction for wet oxidation is:

$$Si + H_2O \rightarrow SiO_2 + H_2$$

4) Low Temperature Oxide (LTO) Deposition

On the other hand, Low Temperature Oxide (LTO) can be deposited using Plasma Enhanced Chemical Vapor Deposition (PECVD) technique. Silicon compounds in combination with hydrogen such as SiH_4 and gases such as N_2O, O_2 or He are used. Low temperature good quality oxides are obtained around $300 - 350$ ℃. Also, in order to reduce hydrogen in oxide film qualities silicon halides such as $SiCl_4$ and SF_4 have been used with RF source frequency around 13.5MHz. [5].

5) Reactive Ion Etching (RIE) of Silicon

Etching is mainly divided into two types: wet and dry etching. In case of wet etching, the main advantage is etching rate is quite high but suffers from isotropic etch. Dry etching is mainly use for anisotropic conditions especially when the feature sizes are very critical.

Reactive based ion etching is plasma based dry etching method where dissociate and ionized relatively stable molecules are discharged from a glass glow forming chemically reactive and ionic species and the chemistry of the species is chosen in such a way that, they react with certain solid material to form volatile products. The key steps in plasma etching [6] are 1) Generation of glow charge 2) D.C bias formation 3) Diffusion/forced convection 4) Absorption 5) Reaction 6) Desorption 7) Exhaust.

For Si etching feeding gas usually used is SF_6. By electron impact ionization of the gas etching atmosphere consists of electrons, photons, radicals (F*) and positive (SF_5^+) and negative (F^-) ions. These ions bombard the si surface with the energy from the RF power source, undergo a reaction on si surface/etch and form volatile compounds and are pumped out.

B. Fin Cut

In order to achieve different operating voltages for Fins, fins are cut into various lengths. This process flow involves deposition of photoresist, patterning of the photo resist, removing the LTO oxide layer using RIE and lastly stripping off the photo resist.

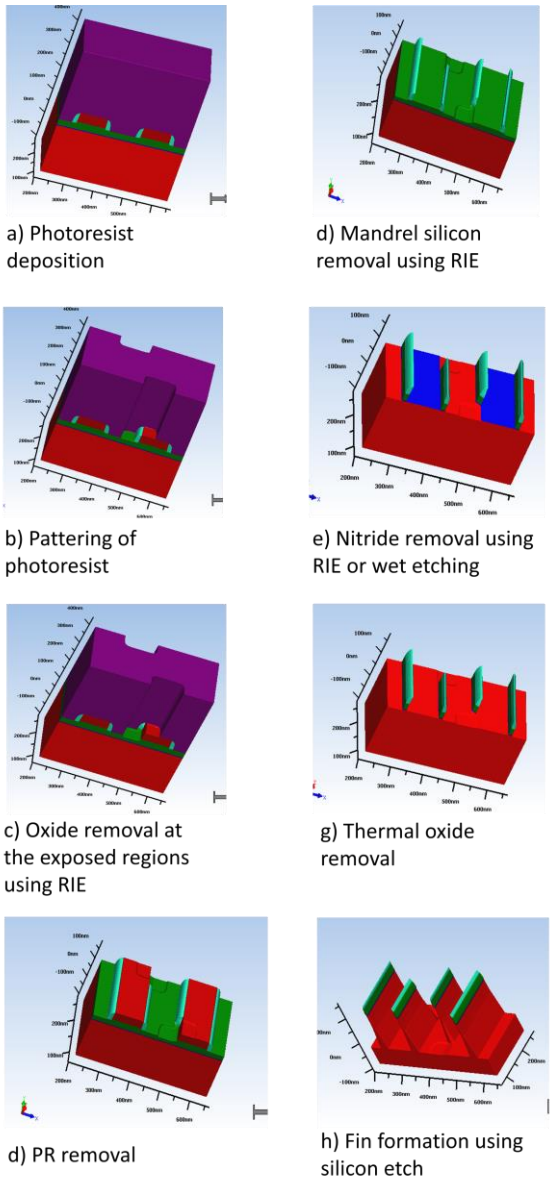


Fig.3. Fin cut fabrication process

The mandrel silicon is removed using mainly by RIE. Next the

barrier layer nitride can be removed by wet etching process using hot phosphoric acid solution followed by thermal oxide removal by RIE. Lastly, using spacer oxide as the mask, silicon is etched to form the fins. 3D view of Fin cut process flow is shown in Fig 3.

1) Reactive Ion Etching of Oxide Layer

Etch ratio is another important factor in RIE system where higher the value better the etching process is. Using RF cathode which is exposed to low pressure CF4-H2 etching gas can be used for oxide etching. Silicon oxide-silicon etch ratio is 35 to 1 and silicon-dioxide to resist etch rate ratio have been measured to be 10 to 1 (which is subjected to various resists). [7]

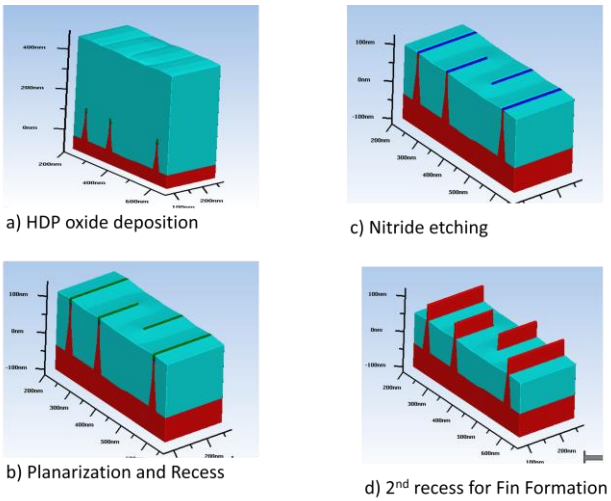


Fig.4. STI and CMP planarization

C. Shallow Trench Isolation (STI)

In Shallow Trench Isolation (STI) high density plasma with no pin holes and more purity on fins. Using Chemical Mechanical Planarization (CMP) the oxide is planarized to achieve uniform surface. Nitride acts as stop layer for polishing process. HDP and CMP processes are explained in detail below. The barrier nitride layer is removed using wet or dry etching. Recession step (oxide etching) is performed which determines the high of the FinFET. Complete STI process is described in Fig4. below.

1) High Density Plasma (HDP) Oxide Deposition

High Density Plasma Chemical Vapor Deposition is special form of PECVD which uses inductively coupled plasma (ICP) as a source to generate a higher plasma to deposit insulating films at low temperatures around $80 - 150$ ℃ of higher quality especially for STI trench fill application.

2) Chemical Mechanical Planarization

Due to decrease in wiring pitch, non-planarized surface topography results in various processing difficulties. These irregularities cause challenges in conformal coating of the resists. Planarized surface has enormous amount benefits such as a) higher photolithography and dry etch yields b) elimination of contact interruption and electro-migration effects. Shallow Trench Isolation (STI) has evolved as important technology in recent times [8]. This method consists of shallow trench on a silicon wafer, depositing oxide, and then planarizing with a Chemical Mechanical Polishing (CMP). This method can separate elements within a much narrow area and demonstrates better performance than the conventional Local Oxidation of Silicon (LOCOS) method.

D. Well Formation

After the STI step, P-Wells and N-Wells are formed by ion-implantation of dopants (Figure 5). This step is carried out earlier as this mitigates the well-STI interface matching problem. In this way, the height of the fins can be measured after the STI etch-back step. This height measurement can then be used to calculate an appropriate implant energy to make the top of the Wells coplanar with the top of the STI [9]. Prior to the well formation, the fins undergo a Rapid Thermal Processing (RTP) process, where sacrificial oxide layer is deposited u to protect the fins during the well formation process as shown in Figure 6(a).

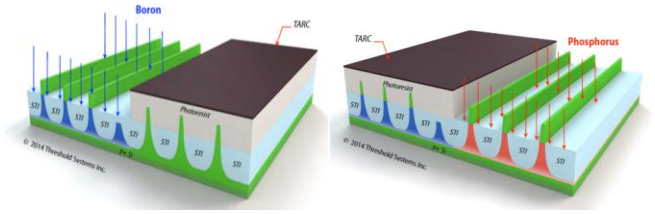


Figure 5. Dopant Implantation for P-well formation. (left); Dopant Implantation for N-Well formation (right) [9].

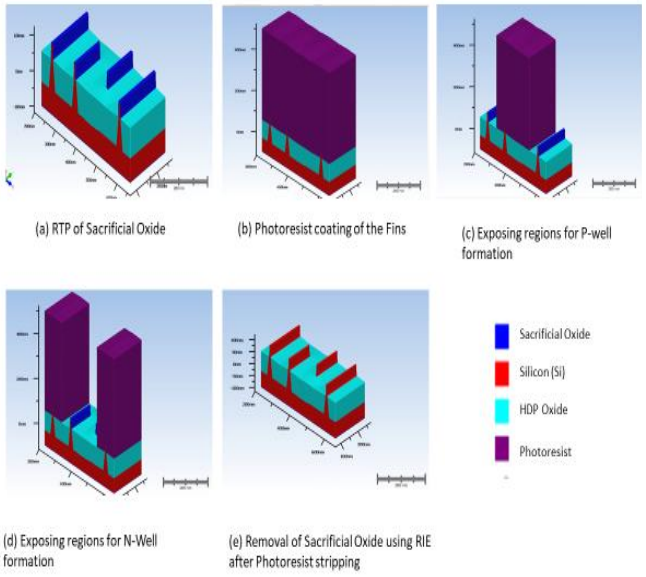


Figure 6. Well Formation.

Following this step, the P-well and N-well formation takes place as shown in figure 6 (b-e). However, this figure shows the lithographical steps involved in the formation of the wells. Figures 6 (b-d) show the lithographical steps involved in formation of P-well while Figure 6 (e) shows the lithographical step involving N-Well formation.
Photoresist is used to cover the areas where future N-wells will be formed while the exposed areas portray where the P-wells (Figure 6 b-c), Next, the exposed region of the wafers are implanted with Boron (mid-E13@10KeV, 7º) to define the P-Well. Figure 6(d) shows the N-well formation where, the exposed region of the wafers is implanted with Phosphorus (mid-E13@10-30KeV, 7º) to define the N-Well [9]. Finally, the Sacrificial oxide layer is etched away using dry etching via RIE process which is shown in Figure 6(e).

E. Dummy Gate Formation

The next step after P-Well and N-Well formation is the formation of a Dummy Gate. The dummy gate is formed before the formation of the Replacement Metal Gate (RMG) as the metal gate cannot bear high temperature processes which are required for future steps.

1. Deposition Steps

Figure 7 shows the process flow for the initial deposition steps involved in the formation of polysilicon based dummy gate. The steps shown involve Deposition and various layers such as sacrificial layers, capping layers, Optically Dispersive Layer (ODL) and Anti-Reflective Layer (ARC). The sacrificial layer is used for protecting the fins for selective etching steps which are carried out to define the dummy gate. Following this, the polysilicon gate is deposited using LPCVD and is then planarized using CMP as shown in Figure 7(c). The next deposition step involves the deposition of Si_3N_4 and Low temperature Oxide layers which serve as capping layers and hard masks respectively for the etching steps that follow. Finally, the last step of depositions includes that of an Optically Dispersive Layer (ODL) which is used as a mask while etching and also as a protective layer, this is usually a polymer. Additionally, an Anti-Reflection Layer is deposited over the ODL which also serves as a barrier coating and an etch stop layer.

2. Etching Steps

The etching steps which follow the deposition steps of the previous stage are shown in Figure 8. All the etching steps are carried out using RIE. The steps shown in figure show how the hard masks such as ODL and ARC are used for etching subsequent layers to define the Dummy gates. As shown, The ARC layer is first etched by using photoresist as a hard mask followed by a RIE dry etch of ODL layer and subsequent stripping of Photoresist. The ARC layer underneath the Photoresist acts as a hard mask to etch the Low temperature Oxide layer. Due to good selectivity of ARC, the remnant material is used as a hard mask to etch the Si_3N_4 capping layer.

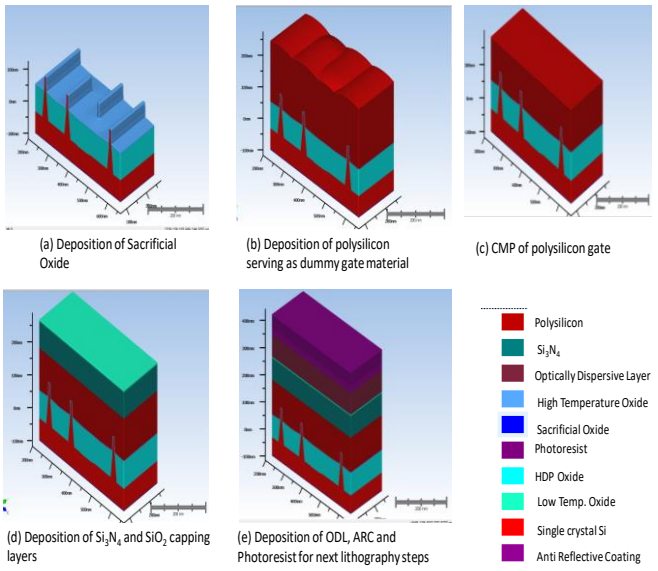


Figure 7. Initial Deposition steps for Dummy Gate Formation

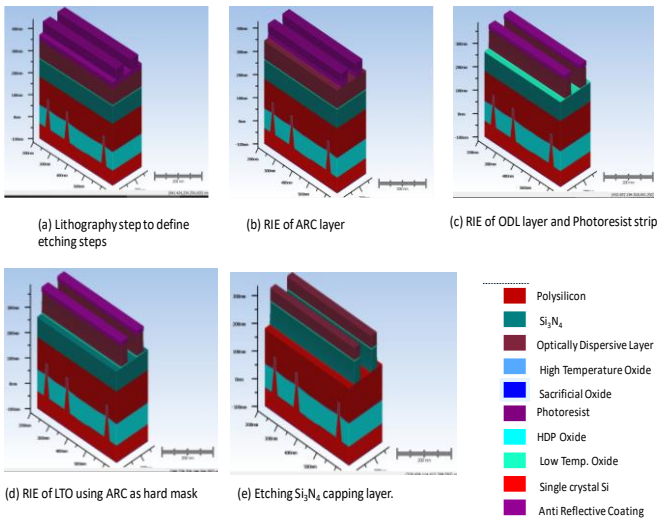


Figure 8. Subsequent Etching steps for dummy gate definition.

3. Defined Dummy Gate Formation.

The final defined Dummy gate formation is shown in Figure 9. The steps involving the lithography of the gate cut has been omitted as it is a repetition of the steps shown in Figure 7 (e) and 8(a-e). Initially, the ODL layer is removed using RIE. After this, the Deposition and Lithography steps are carried out to perform the final Gate Cut process where the dummy gates are

defined to cover the fins (coated with Sacrificial SiO_2) on the P-Well and the N-Well. The Si_3N_4 layer formed during the process is via PECVD process.

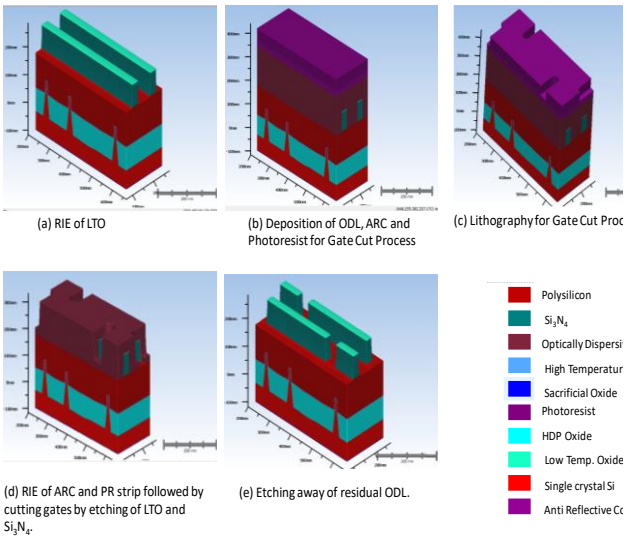


Figure 9. Final Gate Cutting Process.

The final Dummy Gate shown in Figure 10 comprises of the Polysilicon and a Si_3N_4 capping layer on top of it after the removal of LTO and etching of Polysilicon by dry etching.

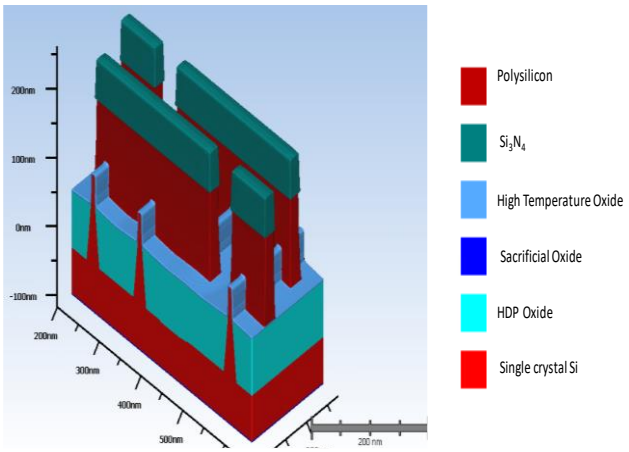


Figure 10. Dummy Gate

F. Source and Drain Formation.

After the formation of the dummy gate, the source and drain for the FinFet is formed. The steps showing the formation of the P side source and drain are shown in Figure 11. Firstly, a Low Temperature Oxide (LTO) layer is deposited as it serves as an etch stop layer. Following this a thick layer of Si_3N_4 is deposited using molecular layer deposition (MLD). This deposition technique is very similar to the atomic layer deposition (ALD) where self-timed surface reactions are carried out in a sequential manner [10]. The Si_3N_4 deposited in this step finds its application as that of a side wall spacer. After this, the Lithography step is performed to facilitate the RIE etching step for forming sidewall spacers. The Si_3N_4 is etched anisotropically as shown in Figure 11 (d). To recess the PFET region, RIE is performed again and residual Si_3N_4 spacers are etched away. Finally, a selective epitaxial deposition of SiGe is performed. In this step, the SiGe will nucleate in the exposed Si surface (on the fin) hence forming a PMOS Source/Drain fin (shown in Figure 11 (f)) as the other Si areas are covered with either a Si_3N_4 layer or Oxide layer.

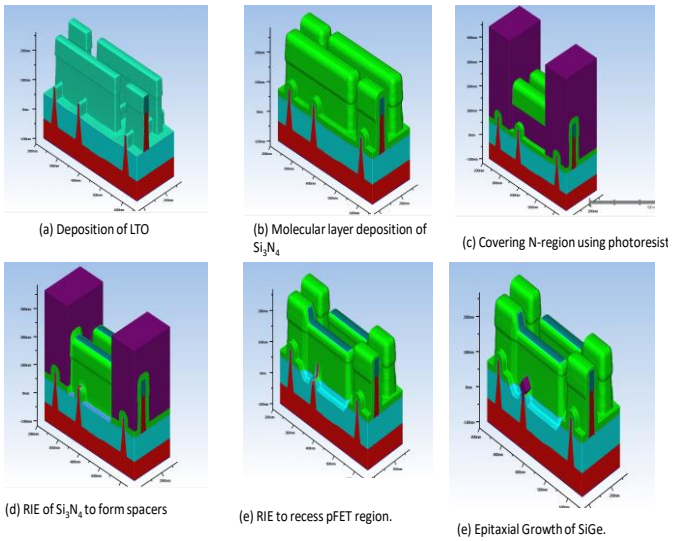


Figure 11. PMOS Source/Drain Formation

After the formation of the PMOS source and drain fin, the similar steps are carried out to form the NMOS source and drain fin, this is shown in Figure 12. In this method, initially, the Si_3N_4 is re-deposited by MLD following a lithography step where Photoresist is used to cover the P source and drain region and expose the regions where N source and drain recess and subsequent Source-Drain formation is supposed to follow. After the Lithography step, the excess spacer layer is etched away on the sidewalls using RIE and so is the Si_3N_4 on the top

surface. Finally, The SiC is epitaxially grown on top of the exposed Si surface (on fin) where the NMOS source and drain fin is formed. It is also important to note that there is a lateral tensile strain and vertical compressive strain in the channel due to the presence of SiC source and drain stressors which is a complementary effect to that observed in the SiGe source and drain stressors [11]. As a result of this, there is an enhanced hole mobility in the p-channel where SiGe stressors play a major role while there will be an enhanced electron mobility in the n-channel transistors which arises due to SiC stressors [11].

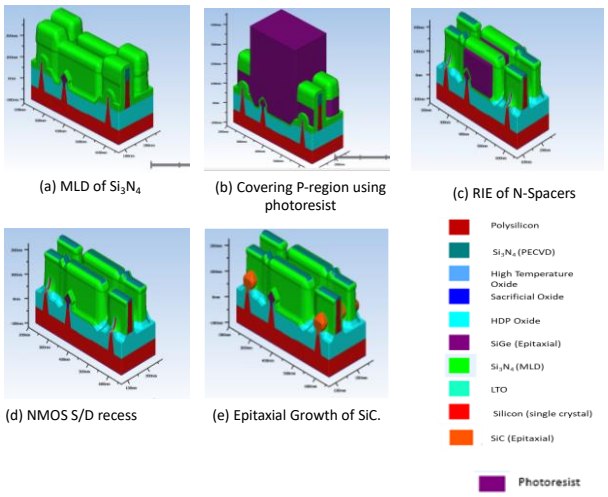


Figure 12. NMOS Source/Drain Formation

G. NiSi Salicide Formation

Silicides are compounds formed with silicon and refractory metals such as Ni and Pt. One of the main reasons of forming this layer after the formation of the Source/Drain formation and right before moving into the Replacement Metal Gate formation regime is that they form a shunting layer [12]. These layers also help reduce the sheet resistance of polysilicon and diffusion. NiSi has a high sintering and eutectic temperature in the range of 900-960C°.

Figure 13. shows the silicide formation. Initially, the surface undergoes an RIE clean step where excess Si_3N_4 is cleaned present on the Source and Drain areas. The next step involves deposition of NiSi layer which is usually carried out by Co-sputtering and Co-evaporation [12]. The Si_3N_4 spacer helps prevent formation of silicide on the side of the gate thus avoiding a short. Figure 13 (c) shows the self-alignment process of the silicide on the gate which is carried out by the RIE process. This self-aligned silicide is known as a salicide [12].

After the FinFET undergoes a Rapid Thermal Annealing (RTA) process, Finally the NiPt silicide is deposited and is then self-aligned to the gate as well as the Epitaxially grown PMOS Source/Drain and NMOS Source/Drain. This is done due to the low contact resistivity of the NiPt salicide and is shown in Figure 13(e) [13]. Following this step, the Replacement Metal Gate formation is carried out.

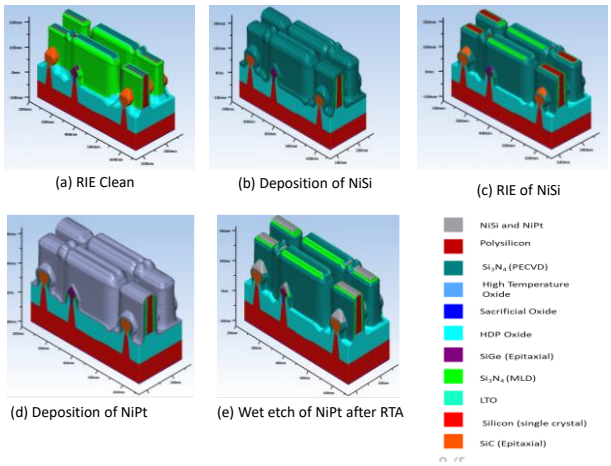


Figure 13. NiSi Salicide Formation

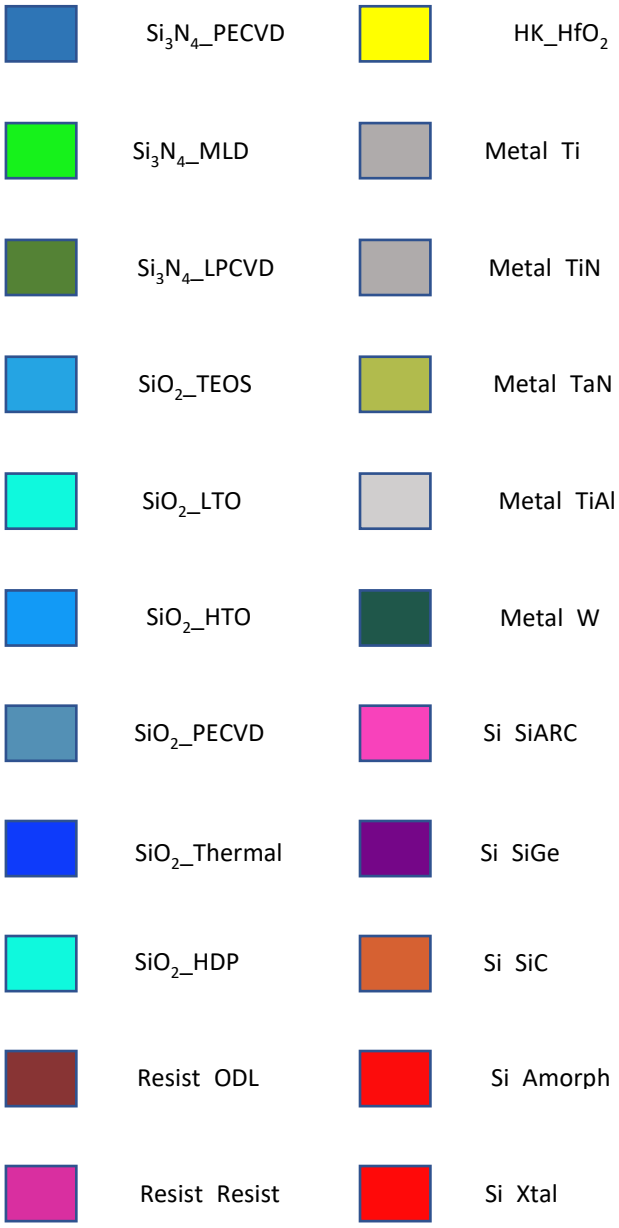
H. Replacement Metal Gate (RMG) Deposition

Most of the Metals we use as a gate material have low thermal budget. High temperatures might alter the threshold voltage. Also, some metals readily form silicides at relatively higher temperatures. Due to theses issue associated with metal gates, we use amorphous silicon as dummy gate during all the high temperature steps [sujit reference]. Once these high thermal budget steps are done, we replace the dummy gate with Replacement Metal Gate (RMG).

Before introducing the RMG, we deposit and planarize Interlayer Dielectric (ILD) around dummy gate. This will ensure isolation between RMG places on different types of fins. We use Two Step Etching to remove dummy gate material. In the first step we perform Non-selective etching. This will etch away the dummy gate material, the Oxide and the Nitride spacers surrounding the dummy gate material. This etch is intended to create a shallow recess trench at the top surface of ILD which will later be filled with Nitride Plug. In the second step we selectively etch the dummy gate material, the oxide spacers surrounding it and also the sacrificial oxide deposited around fins which separates fins and dummy gate materials. This step is followed by deposition of High K Dielectrics. We perform conformal Atomic Later Deposition of a thin Hafnium Oxide film. ALD is layer-by-layer process where the deposition of single layer comprises of several steps which are regulated by supply of precursors. Thus, very conformal and tightly regulated film growth is possible. We use ALD for the subsequent work function material deposition too.

Due to different Threshold voltage and work function requirements for N and P fins we require different sets of material assembly in contact with High-K dielectric. First, we deposit layers that are specific to a type of fin. These layers are deposited uniformly on both types of fins and are then etched

out from the regions where we do not need them. In this process we need Titanium Nitride and Tantalum Nitride (TiN, TaN) for p-type fins and Titanium Aluminum and Titanium Nitride (TiAl, TiN). First, we deposited p-type work function metals uniformly and then etched them from N type fins, Then, we deposited TiAl and TiN as n-type work function metals. Since subsequent layers deposited over work function metals do not have effect on the work function metal-dielectric interface, we need not have to etch them. Next, we deposit the Tungsten metal over these work function metal films. This Tungsten constitutes bulk of the Metal we use as gate material and is common to both p and n-type fins. We planarize and etch the gate metal slightly below the top surface of ILD in order to keep recessed space created by non-selective etch of dummy gate free for Nitride plug. Finally, we place the Nitride Plug on the Top of RMG. This provides isolation between gate and layers above it.



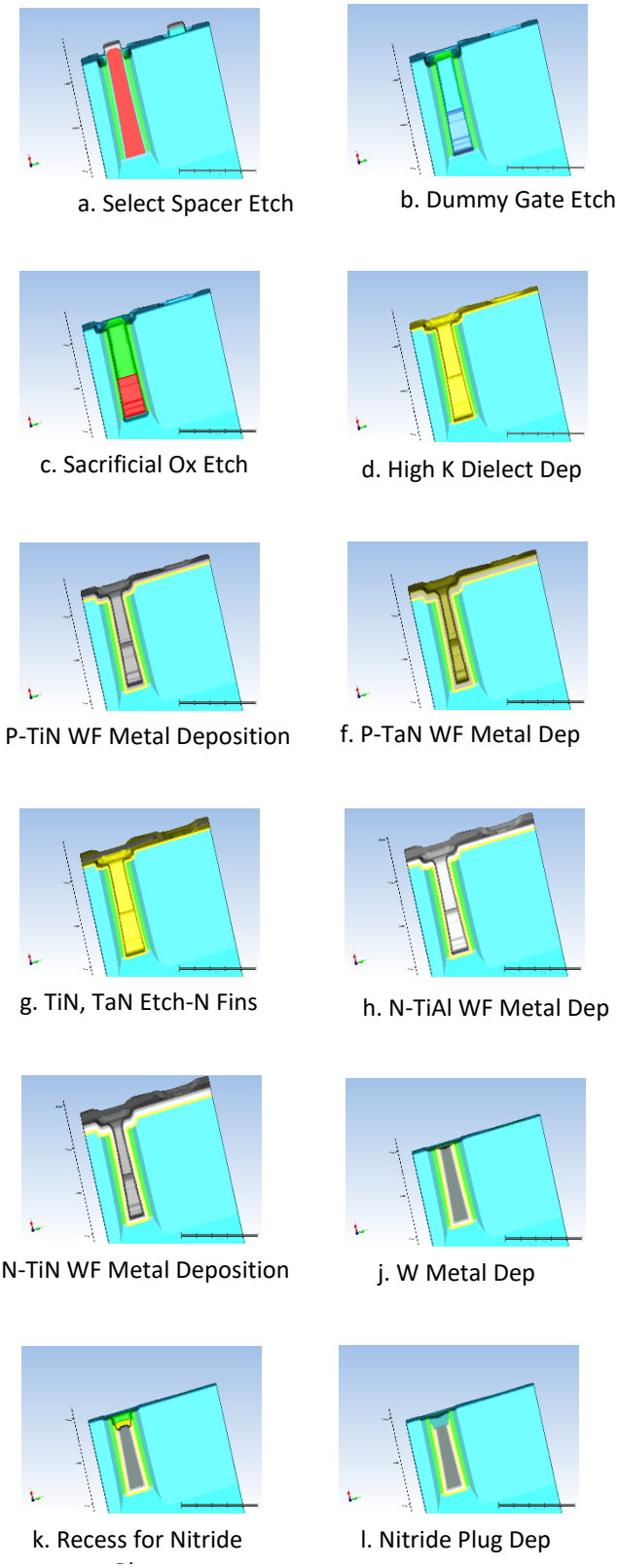
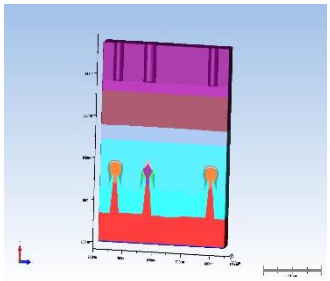


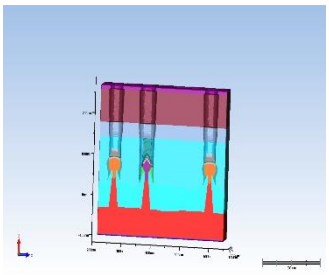
Figure 14: a-c: Dummy Gate Etch; d: High-K dielectric deposition; e-j: Metal Deposition; k-l: Nitride Plug

I. Metallization

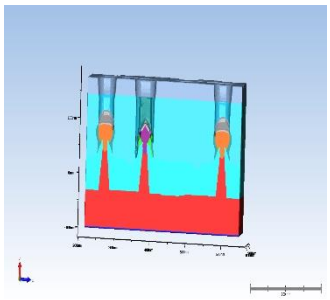
In the last step, we make the metal interconnects on the epitaxially grown source and drain. To make vias we perform two step photolithography. We start with the deposition of Insulator Silicon Oxide which separates the conductor line and electrically active areas of finFETs like Gate Metals. We deposit organic photoresist on the Insulator oxide. We perform second photolithography on this layer. Further, we deposit Amorphous Silicon and its photoresist and form vias pattern on this assembly first. Then in the second step we replicate the same pattern on the Insulator Oxides. After Reactive Ion Etching and Stripping off the Photoresist we see the vias through the insulator film to the top of the fins. To ensure formation of ohmic contacts, we deposit layers of different work function metals. Since we require conformal deposition of this very thin films, we use Atomic Layer Deposition for this purpose. Afterwards we deposit the regular Tungsten Metal and Planarized it to the level of ILD top surface.



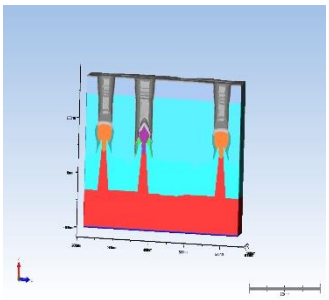
a. Litho 1 on



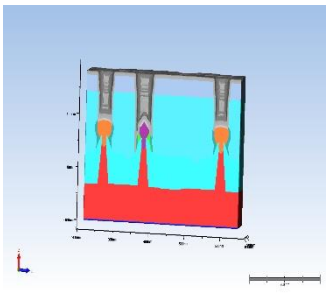
b. Litho 2 on



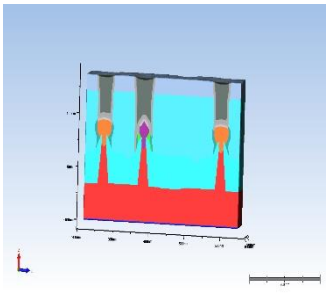
c. Wet etch of PR and



d. Ti WF Metal



e. TiN WF Metal



f. Tungsten Metal

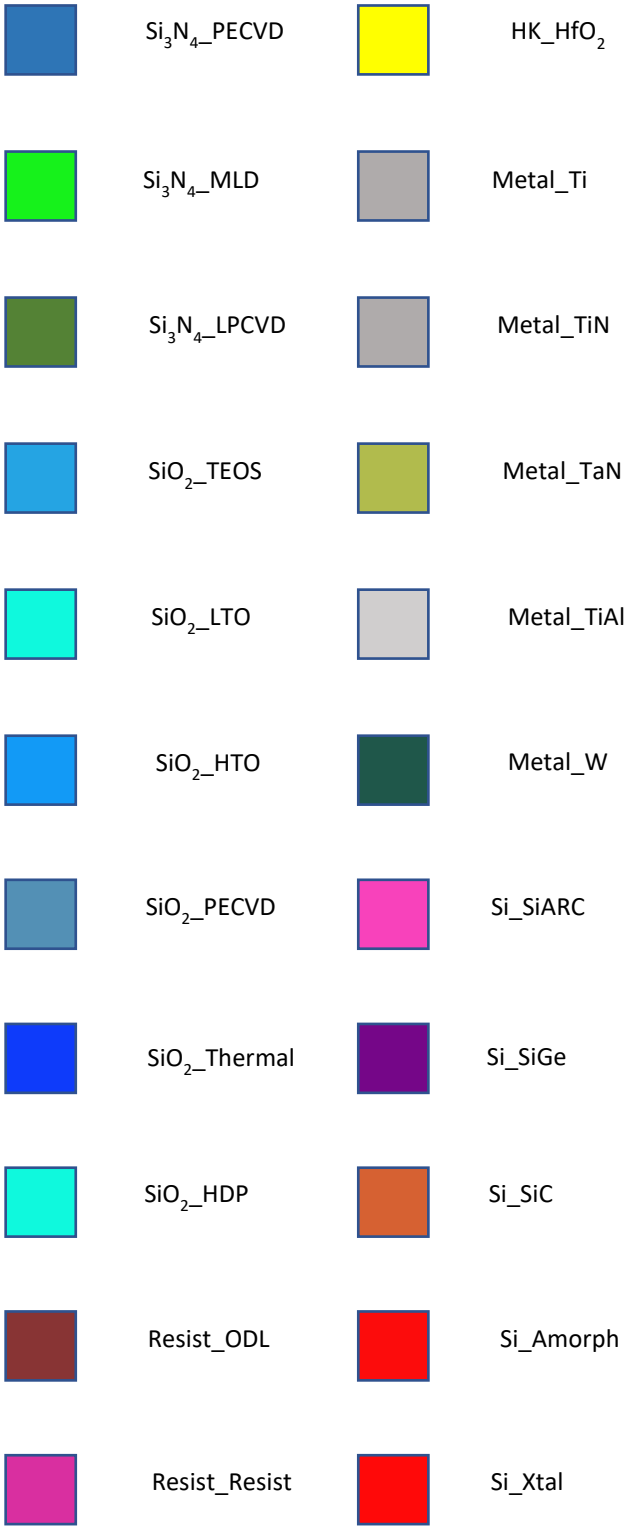


Figure 15: Source Drain Metallization

CONCLUSION

In this paper we analyzed the process flow of 16 nm finFET device. We summarized the fabrication techniques used in the process flow at the beginning. We went through the fin patterning process briefly discussing the lithography, deposition and etching steps associated with it. After fin patterning and fin-cut, we discussed the Shallow Trench Isolation of P and N-Type fins, formation of dummy gates. For performance enhancement we used epitaxially grown Source and Drain Regions. Film composition for Source Drain were different for P-Type from those grown for N-Type fins due to different stress requirements for each of them. The Source and Drain shapes were designed to minimize lattice defects. Due to thermal issues, metal gate was introduced at last replacing the dummy gate. Due to work-function requirement, different metal and intermetallic compounds were used for P and N-Type as contact material after High K Dielectric. The replacement gate process was finished with deposition of Tungsten as a bulk gate material. At last, the source and drain were connected to the circuit using metal lines. Using two step lithography, vias were formed from top of ILD to source and drain region. Finally, work-function metal films followed by tungsten (bulk metal) were deposited to complete the circuit connection. In short, 16 nm finFET fabrication is a convoluted process which requires state-of-the-art facilities and process design for precise fabrication of device.

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