phyCORE®-AM62Ax Direct Solder Connection (DSC)

Hardware Manual

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2 SOM Features

The phyCORE-AM62Ax Direct Solder Connection (DSC) offers the following features:

- Insert-ready, small (40.8 mm x 40.8 mm) System on Module (SOM) subassembly in low EMI design, achieved through advanced SMD technology
- Populated with the Texas Instruments AM62Ax System on Chip (SoC) (18 x 18 mm, 0.8 mm pitch BGA)
- Single supply voltage of 5V with on-board power management IC
- Up to 4GB LPDDR4 RAM
- Up to 128GB on-board eMMC
- 1x Octal/Quad SPI Flash Subsystem connected to a 64MB NOR Flash
- 1x Gigabit Ethernet PHY (signals brought out to connector as differential pairs)
- 1x 4KB I^2C EEPROM
- 1x On-board RTC
- 1x 270 pin 0.8mm pitch castellated edge DSC footprint that expose the following interfaces:
    - 2x MMC/SDIO modules
    - 2x USB 2.0 Ports
    - 1x 10/100/1000 Mbit Ethernet (signals brought out as RGMII)
    - 3x MCAN with CAN-FD support
    - 9x UART
    - 6x I^2C
    - 1x JTAG debug port
    - 4x SPI
    - 3.3V/1.8V GPIOs
    - 4x EPWM (Enhanced Pulse Width Modulator) modules
    - 3x ECAP (Enhanced Capture) modules
    - 3x EQEP (Enhanced Quadrature Encoder Pulse) modules
    - 1x GPMC (General Purpose Memory Controller) module
    - 1x TRC (Trace) module
    - 1x CPTS (Common Platform Time Sync) module
    - 12x Timer modules
    - 1x CSI (Camera Serial Interface) module
    - 3x McASP (Multichannel Audio Serial ports) modules
    - 1x 24-bit RGB parallel display module

NOTE:

Some of the features listed are not available simultaneously due to the multiplexing options of the various processor pins. Refer to the sections 5-12 of this manual for further information on available multiplexing options and the pinout of signals.

3 Conventions, Abbreviations and Acronyms

This hardware manual describes the PCL-075 System on Module, henceforth referred to as phyCORE-AM62Ax DSC. The manual specifies the phyCORE-AM62Ax DSC's design and function. Precise specifications for the Texas Instruments AM62Ax SoC can be found in the AM62Ax Technical Reference Manual.

We refrain from providing detailed part specific information within this manual which can be subject to changes. This is due to the continuous maintenance of our products. Please read *13.4 Product Change Management* for more information.

The BSP delivered with the phyCORE-AM62Ax DSC includes drivers and/or software for controlling all components such as interfaces, memory, etc. Therefore, programming close to the hardware (at the register level) is not necessary in most cases. For this reason, this manual contains no detailed description of the processor's registers, or information relevant for software development. Please refer to the AM62Ax Technical Reference Manual if such information is needed.

3.1 Conventions

The conventions used in this manual are as follows:

- Signals that are preceded by an "n" or end in z (e.g.: nRD or RDz), are designated as active low signals. That is, their active state is when they are driven low, or are driving low.
- A "0" indicates a logic zero or low-level signal, while a "1" represents a logic one or high-level signal.
- The hex-numbers given for addresses of I^2C devices always represent the 7 most-significant bits (MSB) of the address byte. The correct value of the least-significant bit (LSB) will depend on the desired command (read (1) or write (0)) and must be added to get the complete address byte. E.g. given the address in this manual 0x41 => the complete address byte = 0x83 reads from the device and 0x82 to writes to the device
- Text in *blue italics* indicate a cross-reference to an internal section of this Document. Click these links to quickly jump to the applicable part, chapter, table, or figure.
- Text in underlined in blue indicate an external link. Click these links to quickly jump to the applicable URL.
- References made to the DSC footprint always refer to the direct solder connector on the underside of the phyCORE-AM62Ax DSC System on Module.

3.2 Abbreviations and Acronyms

Many acronyms and abbreviations are used throughout this manual. Use the table below to navigate unfamiliar terms used in this document.

Table 1 Abbreviations and Acronyms used in this Manual

Abbreviation	Definition
BSP	Board Support Package (Software delivered with the Development Kit including an operating system (Linux) preinstalled on the module and Development Tools)

CB	Carrier Board; used in reference to the phyCORE Development Kit Carrier Board
DDR	Double data rate
DRAM	Dynamic random access memory
DSC	Direct Solder Connection
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
GPIO	General-Purpose Input/Output
GPT	General-Purpose Timer
J	Solder Jumper: these types of jumpers require solder equipment to remove and place
JP	Solderless Jumper: these types of jumpers can be removed and placed by hand with no special tools
JTAG	Joint Test Action Group (a serial bus protocol usually used for test purposes)
LCD	Liquid Crystal Display
PCB	Printed circuit board
PCI	Peripheral Component Interconnect
PCIe	PCI express
PCM/PCL	phyCORE Module (connectorized / direct solder)
PCN	Product Change Notification
PDI	PHYTEC Display Interface; defined to connect PHYTEC display adapter boards, or custom adapters
PEB	PHYTEC Expansion Board
PMIC	Power management IC
POR	Power-on reset
PRU	Programmable Realtime Unit
PWM	Pulse-width Modulation
RTC	Real-time clock
SOC	System on Chip
SD	Secure Digital
SMT	Surface mount technology
SOM	System on Module; used in reference to the BOARD DESIGNATOR/ SOM BOARD NAME module
SPI	Serial Peripheral Interface
S*x*	User button S*x* (e.g. S1, S2, etc.) used in reference to the available user buttons, or DIP-Switches on the Carrier Board
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus

3.3 Types of Signals

Different types of signals are brought out at the DSC footprint. *Table 2* below lists the abbreviations used to specify the type of a signal.

Table 2 Signal Types Used in this Manual

Signal Type	Description	Abbreviation
Analog	Analog	A
Power	Supply voltage input	PWR_I
Input	Digital input	I
Output	Digital output	O
IO	Bidirectional input/output	I/O
OD-Bidir PU	Open drain input/output with pull up	OD-BI
OD-Output	Open drain output without pull-up, requires an external pull-up	OD
5V Input PD	5 V tolerant input with pull down	5V_PD
USB IO	Differential line pairs 90 Ω USB level bidirectional input/output	USB_I/O
ETHERNET IO	Differential line pairs 100 Ω Ethernet level bidirectional input/output	ETH_I/O
MIPI CSI Input	Differential line pairs 100 Ω MIPI CSI level input	CSI_I

4 Introduction

Figure 1. phyCORE-AM62Ax DSC SOM

The phyCORE-AM62Ax DSC belongs to PHYTEC's phyCORE System on Module family. The phyCORE boards integrate all core elements of a SoC system on a single module and are designed in a manner that ensures their easy expansion and embedding in peripheral hardware developments.

The phyCORE-AM62Ax DSC is a small (40.8 mm x 40.8 mm) insert-ready System on Module populated with the Texas Instrument's AM62Ax SoC. Its universal design enables its insertion in a wide range of embedded applications. Most of the SoC signals and ports extend from the SoC to the DSC footprint on the bottom of the board, allowing it to be soldered down on a target application.

Implementing a phyCORE-AM62Ax DSC SOM as the core of your embedded design allows for increased focus on hardware peripherals and firmware without expending resources to re-invent microprocessor circuitry or other commonly used circuitry that has already been implemented on the phyCORE-AM62Ax DSC including a LPDDR4 RAM, an eMMC, an OSPI Flash, a power distribution network, an Ethernet PHY, an RTC, and an EEPROM. Production-ready board support packages (BSPs), design services for our hardware, and lifecycle maintenance of our parts will further reduce development time, risk, and allows for increased focus on product expertise. Take advantage of PHYTEC products to shorten time-to-market, reduce development costs, and avoid substantial design issues and risks. With this new innovative full system solution, new ideas can be brought to market in the most timely and cost-efficient manner.

Precise specifications for the processor populating the board can be found in the applicable processor reference manual or datasheet. The descriptions in this manual are based on the Texas Instrument's AM62Ax. No descriptions of compatible SoC derivative functions are included; these are not relevant for the basic functioning of the phyCORE-AM62Ax DSC.

4.1 Block Diagram

Figure 2. phyCORE-AM62Ax DSC Block Diagram

4.2 Physical Dimensions

Figure 3. phyCORE-AM62Ax DSC Dimensions Top View

Dimensions

Figure 4. phyCORE-AM62Ax DSC Dimensions End View

4.3 Component Placement Diagram

Figure 5. phyCORE-AM62Ax DSC Component Placement (processor side)

Figure 6. phyCORE-AM62Ax DSC Component Placement (connector side)

A searchable pdf of the phyCORE-AM62Ax DSC component placement can be found here: here.

4.4 Technical and Electrical Specifications

Table 3 Technical Specifications

Specification	
Dimensions	40.8 mm x 40.8 mm x 4.18 mm
Mass	~11.3g
Storage Temperature	-40C to +85C
Operating Temperature	-40C to +85C
Typical Idling Power Consumption[1]	2.2W[1]

[1] Calculated from idle I_{vcc} in *Table 4*

Table 4 Recommended Operating Conditions for the Input and Output Power Domains

Symbol	Description	Conditions	Min	Typical	Max	Unit
VIN	5V SOM input voltage		4.5	5	5.5	VDC
VBAT	Backup battery for RTC		1.2	3	5.5	VDC
I_{VIN}	5V SOM operating current	Idle in Linux with external interfaces down/disconnected (except for Serial RS-232 and SD card)	-	433	-	mA
		Measured while device was under load[1]	-	693	-	mA
		Measured with VDD_3V3_OUT supplying 2A of current alongside the test suite in the row above	-	2013	-	mA
I_{VBAT}	RTC operating current		-	40	-	nA

[1] The load included the following interfaces/commands: the "memtester 500M" command was run, ETH0 was plugged in with iperf3 running, and two instances of the following command were run (yes >/dev/null &), The Yes Command

4.5 Minimum Requirements for Operation

PHYTEC recommends the following minimum requirements for basic operation of the phyCORE-AM62Ax DSC SOM:

- Connect all available 5V input pins to a power supply on a custom carrier board that provides at least 2500 mA (1250 mA if VDD_3V3_OUT is not used in your design).
- Connect all ground pins to ground.
- Implement a power sequencing circuit to avoid driving external power to the I/O pins of the PHYCORE-AM62Ax DSC SOM before the module is fully powered up. More details on this can be found in section *5.4 Power Sequencing*.
- Implement at least one of the supported boot devices to support loading and executing application software. Refer to section *6.3 System Boot Configuration* for more details regarding supported boot modes. The phyCORE-AM62Ax DSC SOM provides an on-board eMMC, but it is recommended to support another boot source for development and debugging. PHYTEC suggests SD boot for which an example circuit can be seen in section 6.2.2.3 *MMC Reference Circuit*

- Strap the boot signals to the desired levels at Power on Reset (POR) to configure the required boot mode for your application (i.e. using a DIP switch). This is required on the carrier board to override the default boot mode set on the SOM. Refer to section *6.3 System Boot Configuration* for more information.
- Implement a serial debug port (such as via UART0) to interface with the module for development. An example can be found in section *11.3 UART0.*
- Implement a reset button for easy reset of the module.

4.6 Solder Jumpers

For configuration purposes the phyCORE-AM62Ax DSC SOM has several solder jumpers. *Figure 7* illustrates the numbering of the solder jumper pads, while *Figure 8* indicates the location and the default configuration of the solder jumpers on the board. *Table 5* provides a functional summary of the solder jumpers which can be changed to adapt the phyCORE-AM62Ax DSC SOM to specific design needs. It shows their default positions, possible alternative positions, type, and functions. The jumpers are a 0201 package size with a 1/16W or higher power rating.

Figure 7. Position Solder Jumper Pad Numbering Scheme

Table 5 Solder Jumper Settings

Jumper	Position	Description	Type
J1	**1+2**	**Sets the VDDSHV0 domain to 3.3V**	0 Ω
	2+3	Sets the VDDSHV0 domain to 1.8V	
J3	**1+2**	**Sets the VDDSHV2 domain to 3.3V**	0 Ω
	2+3	Sets the VDDSHV2 domain to 1.8V	
J4	**1+2**	**Sets the VDDSHV3 domain to 3.3V**	0 Ω
	2+3	Sets the VDDSHV3 domain to 1.8V	
J12	**1+2**	**Sets the VDDSHV6 domain to 3.3V**	0 Ω
	2+3	Sets the VDDSHV6 domain to 1.8V	
J13	**1+2**	**Sets the VDDSHV_MCU domain to 3.3V**	0 Ω
	2+3	Sets the VDDSHV_MCU domain to 1.8V	
J14	**1+2**	**Sets the VDDSHV_CANUART domain to 3.3V**	0 Ω
	2+3	Sets the VDDSHV_CANUART domain to 1.8V	
	2+4	Connects the VDDSHV_CANUART domain to PIO_VDDSHV (a 3.3V domain)	
J19	**1+2**	**Connect GPMC0_CLK to X_GPMC0_CLK**	0 Ω
	2+3	Connect GPMC0_CLK to SD_VSEL	

Jumper	Position	Description	Type
		The state of SD_VSEL determine the voltage level of SoC_VDDSHV5_SDIO.	
J21	**1+2**	**Connect GPMC0_CSn1 to X_GPMC0_CSn1**	0 Ω
	2+3	Connect GPMC0_CSn1 to SD_VSEL The state of SD_VSEL determine the voltage level of SoC_VDDSHV5_SDIO.	

NOTE:
Jumper settings show the default position in **bold, blue text.** Pin 1 is highlighted with an alternate color in *Figure 7* and the solder jumper locations *Figure 8.*

Some of the phyCORE-AM62Ax DSC power domains can be configured for 1.8V or 3.3V operation via the solder jumpers in the table above. This allows for configuring the voltage levels of the associated I/O signals under these domains to meet application requirements. These domains are detailed in the table below:

Table 6 Voltage Domain Configurations

Voltage Domain	Jumper	Associated Signals
VDDSHV_MCU	J13	EMU0, EMU1, TCK, TDI, TDO, TMS, TRSTN, MCU_I2C0_SCL, MCU_I2C0_SDA MCU_SPI0_CLK, MCU_SPI0_D0, MCU_SPI0_D1, MCU_OSC0_XI, MCU_OSC0_XO, MCU_SPI0_CS0, MCU_SPI0_CS1, WKUP_I2C0_SCL, WKUP_I2C0_SDA, WKUP_CLKOUT0, MCU_RESETSTATZ, MCU_RESETZ
VDDSHV_CANUART	J14	WKUP_UART0_RXD, WKUP_UART0_TXD, WKUP_UART0_CTSN, WKUP_UART0_RTSN, MCU_UART0_RXD, MCU_UART0_TXD, MCU_UART0_CTSN, MCU_UART0_RTSN, MCU_MCAN0_RX, MCU_MCAN0_TX, MCU_MCAN1_RX, MCU_MCAN1_TX, PMIC_LPM_EN0
VDDSHV0	J1	MMC1_SDWP, MMC1_SDCD, USB0_DRVVBUS, USB1_DRVVBUS, MCASP0_AXR0, MCASP0_AXR1, MCASP0_AXR2, MCASP0_AXR3, MCASP0_ACLKX, MCASP0_ACLKR, MCASP0_AFSX, MCASP0_AFSR, I2C0_SCL, I2C0_SDA, I2C1_SCL, I2C1_SDA, SPI0_D0, SPI0_D1, SPI0_CS0, SPI0_CS1, SPI0_CLK, MCAN0_RX, MCAN0_TX, UART0_CTSN, UART0_RTSN, UART0_RXD, UART0_TXD, EXT_REFCLK1, PORZ_OUT, RESET_REQZ, RESETSTATZ, EXTINTN
VDDSHV2	J3	RGMII1_RD0, RGMII1_RD1, RGMII1_RD2, RGMII1_RD3, RGMII1_RXC, RGMII1_RX_CTL, RGMII1_TD0, RGMII1_TXC, RGMII1_TX_CTL, RGMII1_TD1, RGMII1_TD2, RGMII1_TD3, RGMII2_RD0, RGMII2_RXC, RGMII2_RX_CTL, RGMII2_TD0, RGMII2_TXC, RGMII2_TX_CTL, RGMII2_RD1, RGMII2_RD2, RGMII2_RD3, RGMII2_TD1, RGMII2_TD2, RGMII2_TD3, MDIO0_MDC, MDIO0_MDIO
VDDSHV3	J4	GPMC0_AD0, GPMC0_AD1, GPMC0_AD2, GPMC0_AD3, GPMC0_AD4, GPMC0_AD5, GPMC0_AD6, GPMC0_AD7, GPMC0_AD8, GPMC0_AD9, GPMC0_AD10, GPMC0_AD11, GPMC0_AD12, GPMC0_AD13, GPMC0_AD14, GPMC0_CLK, GPMC0_ADVN_ALE, GPMC0_OEN_REN, GPMC0_WEN, GPMC0_BE0N_CLE, GPMC0_BE1N, GPMC0_WAIT0, GPMC0_WAIT1, GPMC0_WPN, GPMC0_DIR, GPMC0_CSN0, GPMC0_CSN1, GPMC0_CSN2, GPMC0_CSN3,GPMC0_AD15, VOUT0_DATA0, VOUT0_PCLK, VOUT0_DE, VOUT0_VSYNC, VOUT0_HSYNC, VOUT0_DATA1, VOUT0_DATA2, VOUT0_DATA3, VOUT0_DATA4, VOUT0_DATA5, VOUT0_DATA6, VOUT0_DATA7, VOUT0_DATA8, VOUT0_DATA9, VOUT0_DATA10, VOUT0_DATA11, VOUT0_DATA12, VOUT0_DATA13, VOUT0_DATA14, VOUT0_DATA15
VDDSHV6	J12	MMC2_CLK, MMC2_DAT0, MMC2_DAT1, MMC2_DAT2, MMC2_DAT3, MMC2_SDWP, MMC2_SDCD, MMC2_CMD

If manual jumper modification is required, please ensure that the board as well as surrounding components and sockets remain undamaged while desoldering. Overheating the board can cause the solder pads to loosen, rendering the module inoperable. Follow the instructions carefully for whatever method of removal is used.

CAUTION:
If any modifications to the module are performed, regardless of their nature, the manufacturer warranty is voided.

Figure 8. Jumper Locations (Connector side)

4.7 Pin Descriptions

Most of the processor signals extend to the DSC footprint on the bottom of the module. *Figure 9-11* show recommended landing pattern with dimensions and pin details for soldering down the SOM to a custom carrier board.

Figure 9. Landing Pattern Pinning Detail

Recommended Landing Pattern

Figure 10. Landing Pattern (SOM Edge Dimensions)

Recommended Landing Pattern

Figure 11. Landing Pattern Detail (SOM Corner Dimensions)

Recommended Landing Pattern

Figure 12. Landing Pattern Dimensions (Pin Alignment)

Tables 7-10 provide an overview of the pinout of the phyCORE-Connector with signal names and descriptions specific to the phyCORE-AM62Ax SOM as well as the processor ball it connects to, if any. An example of how this information translates to our schematic is shown in *Figure 13*. The tables also discuss the appropriate voltage domain, signal type, and a description of the functionality. The signal type also includes information about the signal direction.

Figure 13. Pinout example using X_VOUT0_VSYNC in our schematic

Most of the processor pins have multiple multiplexed functions. As most of these pins are connected directly to the SOC footprint, alternative functions are available by using the phyCORE-AM62Ax DSC SOM's pin multiplexing options. Signal names and descriptions in the following tables 7-10, however, refer to the specification of the phyCORE-AM62Ax DSC SOM schematic and may not line up with the functionality defined in the BSP. For information about pin multiplexing contact PHYTEC Support. Please refer to the pinout tables in sections 5-12 to learn about alternative functions. To utilize a specific pin's alternative function, the corresponding registers must be configured within the appropriate driver of the BSP.

Some of the signals which are brought out on the SOC footprint are used to configure the boot mode for specific boot options. These signals should not be driven by any device on the baseboard during reset unless that device is specifically being used to configure the boot pins. The signals that affect the boot configuration are labeled with "BOOTMODE" in the signal name. Details regarding these signals can be found under section *6.3 System Boot Configuration*.

CAUTION:
The Texas Instruments AM62Ax is a multi-voltage operated SoC and as such, special attention should be paid to the interface voltage levels to avoid unintentional damage to the SoC and other on-board components. Please ensure that all module connections do not exceed their expressed maximum voltage/current or drive power before the SOM is fully powered as damage from improper connections varies according to use and application.

It is the user's responsibility to take appropriate safety measures to ensure that the module connections are protected from overloading through connected peripherals.

Please refer to the pinout tables at the end of this section as well as in the various interface sections *5-12* for more information about the operating characteristics. Refer to section *5.4 Power Sequencing* for more information about preventing damage from powering up too early.

4.8 Pinout Table

Table 7 phyCORE-AM62Ax DSC Connector X1, Pins 1-47 Pinout

X1, Pins 1-47					
Pin	**SOM Signal Name**	**Type**	**Level**	**Processor Ball**	**Description**
1	X_GPMC0_CSn2	I/O	3.3V[1]	M22	GPMC Chip Select 2 (active low)
2	X_GPMC0_CSn1	I/O	3.3V[1]	M21	GPMC Chip Select 1 (active low)
3	X_GPMC0_CSn0	I/O	3.3V[1]	M19	GPMC Chip Select 0 (active low)
4	X_GPMC0_AD0/BOOTMODE_0[3]	I/O	3.3V[1]	N21	GPMC Data 0 Input/Output (100K pullup on SOM)
5	X_GPMC0_AD1/BOOTMODE_1[3]	I/O	3.3V[1]	N20	GPMC Data 1 Input/Output (100K pullup on SOM)
6	X_GPMC0_AD1/BOOTMODE_2[3]	I/O	3.3V[1]	N19	GPMC Data 2 Input/Output (100K pulldown on SOM)
7	X_GPMC0_AD3/BOOTMODE_3[3]	I/O	3.3V[1]	N18	GPMC Data 3 Input/Output (100K pullup on SOM)
8	X_GPMC0_AD4/BOOTMODE_4[3]	I/O	3.3V[1]	N17	GPMC Data 4 Input/Output (100K pulldown on SOM)
9	X_GPMC0_AD5/BOOTMODE_5[3]	I/O	3.3V[1]	P18	GPMC Data 5 Input/Output (100K pulldown on SOM)
10	X_GPMC0_AD6/BOOTMODE_6[3]	I/O	3.3V[1]	P19	GPMC Data 6 Input/Output (100K pullup on SOM)
11	X_GPMC0_AD7/BOOTMODE_7[3]	I/O	3.3V[1]	P21	GPMC Data 7 Input/Output (100K pulldown on SOM)
12	X_GPMC0_AD8/BOOTMODE_8[3]	I/O	3.3V[1]	P22	GPMC Data 8 Input/Output (100K pullup on SOM)
13	X_GPMC0_AD9/BOOTMODE_9[3]	I/O	3.3V[1]	R19	GPMC Data 9 Input/Output (100K pullup on SOM)
14	X_GPMC0_AD10/BOOTMODE_10[3]	I/O	3.3V[1]	R20	GPMC Data 10 Input/Output (100K pullup on SOM)
15	X_GPMC0_AD11/BOOTMODE_11[3]	I/O	3.3V[1]	R22	GPMC Data 11 Input/Output (100K pulldown on SOM)
16	X_GPMC0_AD12/BOOTMODE_12[3]	I/O	3.3V[1]	T22	GPMC Data 12 Input/Output (100K pullup on SOM)
17	X_GPMC0_AD13/BOOTMODE_13[3]	I/O	3.3V[1]	R21	GPMC Data 13 Input/Output (100K pullup on SOM)
18	X_GPMC0_AD14/BOOTMODE_14[3]	I/O	3.3V[1]	T20	GPMC Data 14 Input/Output (100K pulldown on SOM)
19	X_GPMC0_AD15/BOOTMODE_15[3]	I/O	3.3V[1]	T21	GPMC Data 15 Input/Output (100K pulldown on SOM)
20	X_GPMC0_WAIT0	I/O	3.3V[1]	R18	GPMC External Indication of Wait
21	X_GPMC0_DIR	I/O	3.3V[1]	K18	GPMC Data Bus Signal Direction Control
22	X_GPMC0_CLK	I/O	3.3V[1]	N22	GPMC clock
23	SoC_VDDSHV5_SDIO[2]	PWR_IO	3.3V	-	SD IO voltage
24	VBAT	PWR_I	3.0V	-	Battery Backup Supply Input for RTC
25	VIN	PWR_I	5.0V	-	Main Power Supply Input
26	VIN	PWR_I	5.0V	-	Main Power Supply Input
27	X_VOUT0_PCLK	I/O	3.3V[1]	AA22	Video Output Pixel Clock Output
28	X_VOUT0_DE	I/O	3.3V[1]	U17	Video Output Data Enable
29	X_VOUT0_VSYNC	I/O	3.3V[1]	V17	Video Output Vertical Sync
30	X_VOUT0_HSYNC	I/O	3.3V[1]	T18	Video Output Horizontal Sync
31	X_VOUT0_DATA15	I/O	3.3V[1]	Y22	Video Output Data

X1, Pins 1-47					
Pin	SOM Signal Name	Type	Level	Processor Ball	Description
32	X_VOUT0_DATA14	I/O	3.3V[1]	Y21	Video Output Data
33	X_VOUT0_DATA13	I/O	3.3V[1]	W19	Video Output Data
34	X_VOUT0_DATA12	I/O	3.3V[1]	W20	Video Output Data
35	X_VOUT0_DATA11	I/O	3.3V[1]	W21	Video Output Data
36	X_VOUT0_DATA10	I/O	3.3V[1]	W22	Video Output Data
37	X_VOUT0_DATA9	I/O	3.3V[1]	V18	Video Output Data
38	X_VOUT0_DATA8	I/O	3.3V[1]	V19	Video Output Data
39	X_VOUT0_DATA7	I/O	3.3V[1]	V21	Video Output Data
40	X_VOUT0_DATA6	I/O	3.3V[1]	V22	Video Output Data
41	X_VOUT0_DATA5	I/O	3.3V[1]	U18	Video Output Data
42	X_VOUT0_DATA4	I/O	3.3V[1]	Y19	Video Output Data
43	X_VOUT0_DATA3	I/O	3.3V[1]	U19	Video Output Data
44	X_VOUT0_DATA2	I/O	3.3V[1]	U20	Video Output Data
45	X_VOUT0_DATA1	I/O	3.3V[1]	U21	Video Output Data
46	X_VOUT0_DATA0	I/O	3.3V[1]	U22	Video Output Data
47	X_MDIO0_MDC	I/O	3.3V[1]	V12	MDIO Clock (1.5K pullup on SOM)

[1:] The voltage level for this signal is configurable for 1.8V or 3.3V. The default voltage level is listed here, but always check the actual jumper setting for the applicable SOM configuration. Refer to section *4.6 Solder Jumpers* for details.
[2:] More information about this signal can be found in section *5 Power*
[3:] This signal should not be driven during reset. More information can be found in section *6.3 System Boot Configuration*

Table 8 phyCORE-AM62Ax DSC Connector X1, Pins 48-94 Pinout

X1, Pins 48-94					
Pin	Signal Name	Type	Level	Processor Ball	Description
48	X_MDIO0_MDIO	I/O	3.3V[1]	V13	MDIO Data (1.5K pullup on SOM)
49	X_CPSW_RGMII2_RX_CTL	I/O	3.3V[1]	W18	RGMII Receive Control
50	X_CPSW_RGMII2_RXC	I/O	3.3V[1]	AA20	RGMII Receive Clock
51	X_CPSW_RGMII2_RD3	I/O	3.3V[1]	AB20	RGMII Receive Data 3
52	X_CPSW_RGMII2_RD2	I/O	3.3V[1]	AB21	RGMII Receive Data 2
53	X_CPSW_RGMII2_RD1	I/O	3.3V[1]	Y20	RGMII Receive Data 1
54	X_CPSW_RGMII2_RD0	I/O	3.3V[1]	AA21	RGMII Receive Data 0
55	X_CPSW_RGMII2_TX_CTL	I/O	3.3V[1]	Y19	RGMII Transmit Control
56	X_CPSW_RGMII2_TXC	I/O	3.3V[1]	AB19	RGMII Transmit Clock
57	X_CPSW_RGMII2_TD0	I/O	3.3V[1]	AA19	RGMII Transmit Data 0
58	X_CPSW_RGMII2_TD1	I/O	3.3V[1]	Y18	RGMII Transmit Data 1
59	X_CPSW_RGMII2_TD2	I/O	3.3V[1]	AA18	RGMII Transmit Data 2
60	X_CPSW_RGMII2_TD3	I/O	3.3V[1]	W17	RGMII Transmit Data 3
61	X_CPSW_ETH0_GPIO_0	I/O	3.3V[1]	-	SOM Ethernet PHY GPIO 0[2]
62	X_CPSW_ETH0_LED_ACTIVITY	O	3.3V	-	Ethernet LED Activity Signal
63	X_CPSW_ETH0_D-	I/O	Differential	-	Ethernet Data D Negative
64	X_CPSW_ETH0_D+	I/O	Differential	-	Ethernet Data D Positive
65	X_CPSW_ETH0_C-	I/O	Differential	-	Ethernet Data C Negative
66	X_CPSW_ETH0_C+	I/O	Differential	-	Ethernet Data C Positive
67	X_CPSW_ETH0_B-	I/O	Differential	-	Ethernet Data B Negative
68	X_CPSW_ETH0_B+	I/O	Differential	-	Ethernet Data B Positive
69	X_CPSW_ETH0_A-	I/O	Differential	-	Ethernet Data A Negative
70	X_CPSW_ETH0_A+	I/O	Differential	-	Ethernet Data A Positive
71	X_CPSW_ETH0_LED_LINK	O	3.3V	-	Ethernet LED Link Signal
72	X_CPSW_ETH0_nINT	I/O	3.3V[1]	-	SOM Ethernet PHY Interrupt (active low, 2.2K pullup on SOM)
73	X_USB0_DRVVBUS	I/O	3.3V[1]	C20	USB VBUS control output (active high)
74	X_USB0_DM	I/O	Differential	AA10	USB 2.0 Differential Data (negative)

X1, Pins 48-94					
Pin	**Signal Name**	**Type**	**Level**	**Processor Ball**	**Description**
75	X_USB0_DP	I/O	Differential	AA9	USB 2.0 Differential Data (positive)
76	X_USB0_VBUS	A/I	5V	V8	USB Level-shifted VBUS Input (resistor/diode network on SOM)
77	X_USB1_DRVVBUS	I/O	3.3V[1]	D19	USB VBUS control output (active high)
78	X_USB1_DM	I/O	Differential	Y11	USB 2.0 Differential Data (negative)
79	X_USB1_DP	I/O	Differential	Y10	USB 2.0 Differential Data (positive)
80	X_USB1_VBUS	A/I	5V	V6	USB Level-shifted VBUS Input (resistor/diode network on SOM)
81	X_CSI0_RXCLKP	I	Differential	AB13	CSI Differential Receive Clock Input (positive)
82	X_CSI0_RXCLKN	I	Differential	AB14	CSI Differential Receive Clock Input (negative)
83	X_CSI0_RXP1	I	Differential	Y14	CSI Differential Receive Input (positive)
84	X_CSI0_RXN1	I	Differential	Y13	CSI Differential Receive Input (negative)
85	X_CSI0_RXP2	I	Differential	AA12	CSI Differential Receive Input (positive)
86	X_CSI0_RXN2	I	Differential	AA13	CSI Differential Receive Input (negative)
87	X_CSI0_RXP3	I	Differential	AB10	CSI Differential Receive Input (positive)
88	X_CSI0_RXN3	I	Differential	AB11	CSI Differential Receive Input (negative)
89	X_CSI0_RXP0	I	Differential	W13	CSI Differential Receive Input (positive)
90	X_CSI0_RXN0	I	Differential	W12	CSI Differential Receive Input (negative)
91	VDD_3V3_OUT	PWR_O	3.3V	-	VCC 3.3V Output (2A)
92	VDD_3V3_OUT	PWR_O	3.3V	-	VCC 3.3V Output (2A)
93	VDD_3V3_OUT	PWR_O	3.3V	-	VCC 3.3V Output (2A)
94	VDD_3V3_OUT	PWR_O	3.3V	-	VCC 3.3V Output (2A)

[1:] The voltage level for this signal is configurable for 1.8V or 3.3V. The default voltage level is listed here, but always check the actual jumper setting for the applicable SOM configuration. Refer to section *4.6 Solder Jumpers* for details.

Table 9 phyCORE-AM62Ax DSC Connector X1, Pins 95-141 Pinout

X1, Pins 95-141					
Pin	**Signal**	**Type**	**Level**	**Processor Ball**	**Description**
95	-	-	-	-	-
96	-	-	-	-	-
97	-	-	-	-	-
98	-	-	-	-	-
99	-	-	-	-	-
100	-	-	-	-	-
101	-	-	-	-	-
102	-	-	-	-	-
103	-	-	-	-	-
104	-	-	-	-	-
105	-	-	-	-	-
106	-	-	-	-	-
107	-	-	-	-	-
108	-	-	-	-	-
109	-	-	-	-	-
110	-	-	-	-	-
111	X_WKUP_UART0_RTSN	I/O	3.3V[1]	C8	UART Request to Send (active low)
112	X_WKUP_UART0_CTSN	I/O	3.3V[1]	C10	UART Clear to Send (active low)
113	X_WKUP_UART0_RXD	I/O	3.3V[1]	C9	UART Receive Data
114	X_WKUP_UART0_TXD	I/O	3.3V[1]	E9	UART Transmit Data
115	X_MCU_MCAN0_RX	I/O	3.3V[1]	E8	MCAN Receive Data

X1, Pins 95-141					
Pin	**Signal**	**Type**	**Level**	**Processor Ball**	**Description**
116	X_MCU_MCAN0_TX	I/O	3.3V[1]	C7	MCAN Transmit Data
117	X_MCU_MCAN1_RX	I/O	3.3V[1]	B9	MCAN Receive Data
118	X_MCU_MCAN1_TX	I/O	3.3V[1]	D7	MCAN Transmit Data
119	X_MCU_I2C0_SCL	OD-I/O	3.3V[1]	E12	MCU I2C0 Clock (Requires pullup)
120	X_MCU_I2C0_SDA	OD-I/O	3.3V[1]	D9	MCU I2C0 Data (Requires pullup)
121	X_MCU_SPI0_CLK	I/O	3.3V[1]	B13	SPI Clock
122	X_MCU_SPI0_D0	I/O	3.3V[1]	A15	SPI Data 0
123	X_MCU_SPI0_D1	I/O	3.3V[1]	B12	SPI Data 1
124	X_MCU_SPI0_CS1	I/O	3.3V[1]	C11	SPI Chip Select 1
125	X_WKUP_I2C0_SCL	OD-I/O	3.3V[1]	D13	WKUP I2C0 Clock (Requires pullup)
126	X_WKUP_I2C0_SDA	OD-I/O	3.3V[1]	E13	WKUP I2C0 Data (Requires pullup)
127	X_MCU_UART0_CTSN	I/O	3.3V[1]	B11	UART Clear to Send (active low)
128	X_MCU_UART0_RTSN	I/O	3.3V[1]	D10	UART Request to Send (active low)
129	X_MCU_UART0_RXD	I/O	3.3V[1]	B8	UART Receive Data
130	X_MCU_UART0_TXD	I/O	3.3V[1]	F8	UART Transmit Data
131	X_WKUP_CLKOUT0	I/O	3.3V[1]	B10	WKUP Domain CLKOUT0 output
132	X_EXT_REFCLK1	I/O	3.3V[1]	B16	External clock input to Main Domain
133	X_SPI0_CLK	I/O	3.3V[1]	A17	SPI Clock
134	X_SPI0_D0	I/O	3.3V[1]	B15	SPI Data 0
135	X_SPI0_D1	I/O	3.3V[1]	E15	SPI Data 1
136	X_SPI0_CS0	I/O	3.3V[1]	D16	SPI Chip Select 0
137	X_SPI0_CS1	I/O	3.3V[1]	C16	SPI Chip Select 1
138	X_UART0_CTSN	I/O	3.3V[1]	F14	UART Clear to Send (active low)
139	X_UART0_RTSN	I/O	3.3V[1]	C15	UART Request to Send (active low)
140	X_UART0_RXD	I/O	3.3V[1]	E14	UART Receive Data
141	X_UART0_TXD	I/O	3.3V[1]	D15	UART Transmit Data

[1:] The voltage level for this signal is configurable for 1.8V or 3.3V. The default voltage level is listed here, but always check the actual jumper setting for the applicable SOM configuration. Refer to section *4.6 Solder Jumpers* for details

Table 10 phyCORE-AM62Ax DSC Connector X1, Pins 142-188 Pinout

X1, Pins 142-188					
Pin	**Signal**	**Type**	**Level**	**Processor Ball**	**Description**
142	X_MCAN0_RX	I/O	3.3V[1]	C18	MCAN Receive Data
143	X_MCAN0_TX	I/O	3.3V[1]	B17	MCAN Transmit Data
144	X_I2C0_SCL	I/O	3.3V[1]	D17	I2C0 Clock (2.2K pullup on SOM)
145	X_I2C0_SDA	I/O	3.3V[1]	E16	I2C0 Data (2.2K pullup on SOM)
146	X_I2C1_SCL	I/O	3.3V[1]	C17	I2C1 Clock
147	X_I2C1_SDA	I/O	3.3V[1]	E17	I2C1 Data
148	X_MCASP0_AFSR	I/O	3.3V[1]	B21	MCASP Receive Frame Sync
149	X_MCASP0_AFSX	I/O	3.3V[1]	A20	MCASP Transmit Frame Sync
150	X_MCASP0_ACLKR	I/O	3.3V[1]	A21	MCASP Receive Bit Clock
151	X_MCASP0_ACLKX	I/O	3.3V[1]	A19	MCASP Transmit Bit Clock
152	X_MCASP0_AXR3	I/O	3.3V[1]	C19	MCASP Serial Data
153	X_MCASP0_AXR2	I/O	3.3V[1]	B19	MCASP Serial Data
154	X_MCASP0_AXR1	I/O	3.3V[1]	B18	MCASP Serial Data (Input/Output)
155	X_MCASP0_AXR0	I/O	3.3V[1]	B20	MCASP Serial Data (Input/Output)
156	X_MMC1_SDWP	I/O	3.3V[1]	D18	SD Write Protect (10K pullup on SOM)

X1, Pins 142-188					
Pin	**Signal**	**Type**	**Level**	**Processor Ball**	**Description**
157	X_MMC1_SDCD	I/O	3.3V[1]	E18	SD card Detect (10K pullup on SOM)
158	X_MMC1_CLK	I/O	3.3V[1]	E22	MMC/SD/SDIO Clock (49.9K pulldown on SOM)
159	X_MMC1_DAT0	I/O	3.3V[1]	B22	MMC/SD/SDIO Data
160	X_MMC1_DAT1	I/O	3.3V[1]	D21	MMC/SD/SDIO Data
161	X_MMC1_DAT2	I/O	3.3V[1]	C22	MMC/SD/SDIO Data
162	X_MMC1_DAT3	I/O	3.3V[1]	D22	MMC/SD/SDIO Data
163	X_MMC1_CMD	I/O	3.3V[1]	C21	MMC/SD/SDIO Command
164	X_MMC2_SDWP	I/O	3.3V[1]	E21	SD Write Protect (10K pullup on SOM)
165	X_MMC2_SDCD	I/O	3.3V[1]	F22	SD Card Detect (10K pullup on SOM)
166	X_MMC2_CLK	I/O	3.3V[1]	H22	MMC/SD/SDIO Clock (49.9K pulldown on SOM)
167	X_MMC2_DAT0	I/O	3.3V[1]	E20	MMC/SD/SDIO Data
168	X_MMC2_DAT1	I/O	3.3V[1]	F21	MMC/SD/SDIO Data
169	X_MMC2_DAT2	I/O	3.3V[1]	F20	MMC/SD/SDIO Data
170	X_MMC2_DAT3	I/O	3.3V[1]	G21	MMC/SD/SDIO Data
171	X_MMC2_CMD	I/O	3.3V[1]	G22	MMC/SD/SDIO Command
172	X_GPMC0_BE1n	I/O	3.3V[1]	M18	GPMC Upper-Byte Enable (active low)
173	X_GPMC0_BE0n_CLE	I/O	3.3V[1]	L19	GPMC Lower-Byte Enable (active low) or Command Latch Enable
174	X_GPMC0_ADVn_ALE	I/O	3.3V[1]	L18	GPMC Address Valid (active low) or Address Latch Enable
175	X_GPMC0_CSn3	I/O	3.3V[1]	M20	GPMC Chip Select 3 (active low)
176	X_GPMC0_WAIT1	I/O	3.3V[1]	R17	GPMC External Indication of Wait
177	X_GPMC0_WPn	I/O	3.3V[1]	K17	GPMC Flash Write Protect (active low)
178	X_GPMC0_OEn_REn	I/O	3.3V[1]	L17	GPMC Output Enable (active low) or Read Enable (active low)
179	X_GPMC0_WEn	I/O	3.3V[1]	K19	GPMC Write Enable (active low)
180	X_RESETSTATz	O	3.3V[1]	F19	Main Domain warm reset status output (10K pulldown on SOM)
181	X_MCU_SAFETY_ERRORn	I/O	1.8V	B8	Error Signal Output
182	X_PMIC_EN	I	5V	-	PMIC power enable (100k pullup on SOM)
183	X_nRESET_IN	I	3.3V	-	Reset input (active low, 10K pullup on SOM)
184	X_PGOOD	OD-O	3.3V	-	Power good output (100K pullup on SOM)
185	X_MCU_RESETSTATz	I/O	3.3V[1]	D14	MCU Domain warm reset status output (10K pulldown on SOM)
186	X_MCU_RESETz	I	3.3V[1]	C12	MCU Domain warm reset (100K pullup on SOM)
187	X_PORz_OUT	O	3.3V[1]	F18	Main Domain POR status output (1.5K pulldown on SOM)
188	X_RESET_REQz	I	3.3V[1]	E19	Main Domain external warm reset request input (100K pullup on SOM)

[1:] The voltage level for this signal is configurable for 1.8V or 3.3V. The default voltage level is listed here, but always check the actual jumper setting for the applicable SOM configuration. Refer to section *4.6 Solder Jumpers* for details.

Table 11 phyCORE-AM62Ax DSC Connector X1, Pins 189-270 Pinout

X1, Pins 189-270					
Pin	**Signal**	**Type**	**Level**	**Processor Ball**	**Description**
189-236	GND	-	-	-	Ground
237	X_RTC_INT	I/O	3.3V[1]	F17	RTC Interrupt (10K pullup on SOM)
238	X_EMU1	I/O	3.3V[1]	E10	Emulation Control 1 (5.76K pullup on SOM)
239	X_EMU0	I/O	3.3V[1]	C13	Emulation Control 0 (5.76K pullup on SOM)
240	X_RTC_EVI	I	3.3V[1]	-	RTC Event Input (10K pullup on SOM)
241	X_VPP_EN	I	3.3V	-	Enable pin for VPP rail (10K pulldown on SOM)

X1, Pins 189-270					
Pin	**Signal**	**Type**	**Level**	**Processor Ball**	**Description**
242	X_TRSTN	I	3.3V[1]		JTAG Reset (10K pulldown on SOM)
243	X_TMS	I	3.3V[1]	B11	JTAG Test Mode Select Input (10K pullup on SOM)
244	X_TDO	O	3.3V[1]	D12	JTAG Test Data Output
245	X_TDI	I	3.3V[1]	A11	JTAG Test Data Input (10K pullup on SOM)
246	X_TCK	I	3.3V[1]	A10	JTAG Test Clock Input (10K pullup on SOM)
247-270	GND	-	-	-	Ground

[1]: The voltage level for this signal is configurable for 1.8V or 3.3V. The default voltage level is listed here, but always check the actual jumper setting for the applicable SOM configuration. Refer to section *4.6 Solder Jumpers* for details.

4.9 Thermal Management

Thermal management is necessary to ensure proper operation of the phyCORE-AM62Ax DSC SOM, especially when integrated inside of an enclosure as the AM62Ax SOC processor generates considerable heat.

The phyCORE-AM62Ax DSC has an ambient temperature rating of -40C to 85C with a critical junction temperature of 105C. PHYTEC has found that a fan and a heatsink help prevent overheating at the higher end of the phyCORE-AM62Ax DSC's temperature operating range (during our temperature testing the SOM would experience overheating shutdowns when ambient temperatures went above 75C without an active cooling system (heatsink and fan)). The following parts are used to attach the fan to the phyCORE-AM62Ax DSC SOM processor and to connect the fan power cable to the connector on the PHYTEC phyCORE-AM62Ax DSC Carrier Board:

Table 12 Thermal Management Parts

Recommended Thermal Component	Part Number
Heatsink	BDN10-3CB/A01
5VDC Fan	CFM-2510B-0100-218-22
Fan Connector	47054-1000
4x Fan Crimping Terminals	0850-0113
Carrier Board Connector	47053-1000
3x #4 5/8'' Screws	90190A112

The heatsink is mounted on top of the processor with heatsink adhesive. Then the crimping terminals are crimped to the exposed fan wires, which allows the fan to be mounted to the 5-pin connector that mates with the PHYTEC Carrier board. Finally, the fan is secured to the heatsink with screws. The PHYTEC Carrier Board supplies 5V power to the fan via the 47053-1000 connector. The fan circuit on the AM62Ax DSC Carrier Board is shown below and allows for user control over the fan.

Figure 14. Fan design reference circuit

4.10 Layout Guidelines

4.10.1 High-Speed Differential Signal Routing Guidelines

Spacing

- Implement proper trace width and spacing to yield the recommended differential impedance value.
- Spacing between the differential pairs and other traces should be at least twice the distance between the inter-pair spacing.
- Avoid routing high-speed signals near other sensitive circuits (such as crystals, oscillators, switching regulators, clock signals, etc.).

Routing

- Route the two traces of a differential pair on the same layer(s).
- Route signals over an adjacent, solid ground reference plane. Ensure there are no layers between the routing layer and reference layer.
- Avoid routing across a gap or cut-out in the reference plane or across different reference planes. Cuts in the reference plane should be avoided in general.
- Avoid sharp bends on differential lanes.
- Minimize total trace length.
- Keep the length of the two traces in a differential pair as close as possible. Recommended length matching is listed in the various Design In Guide sub-sections contained in this document as well as the length of the traces on the

SOM. This information can be used to further correct or avoid worsening any SOM trace length mismatches in your own design.

Vias and Stubs

- Avoid routing through vias when possible. The number of vias on the differential pairs should be minimized. If necessary, each signal of the differential pair should be routed through matching number of vias. In the case of multiple differential lanes in the same interface, all lines should have the same number of vias.
- Minimize discontinuities on the signal path (such as stubs) and avoid placing test points, external components like 0Ω resistors, or any other components that are not required when possible.
- Surface-mount receptacles are preferred over through-hole connectors, as signals can be routed on the top layer of the PCB without introducing vias to the signal path. If through-hole pins are necessary, it may be beneficial to route signals on the bottom layer.

4.10.2 General Signal Routing Guidelines

- Pay special attention to signal placement, trace impedances, maximum trace length, and trace length tolerances when routing SOM signals.
- Place and route high-speed signals, such as CSI, Ethernet, USB, etc. before placing and routing any other interfaces. This is recommended to ensure that the stricter trace lengths and length matching requirements of these interfaces are met.
- Place and route the remaining interfaces after the high-speed interfaces are completely routed.
- All communication signals/interfaces should have an accompanying solid reference plane.
- Separate clocks and other high-speed signals as much as possible from nearby traces to reduce crosstalk. A general rule is to use a clearance of at least 3 times the trace width.

5 Power

The following sub-sections discuss the power configuration of the phyCORE-AM62Ax DSC in detail. *Table 13* summarizes the relationships between the voltage rails and the devices on the phyCORE-AM62Ax DSC SOM.

Table 13 External Supply Voltages

Signal	Direction	Power Draw / Deliver	Pins	Description
VIN	I	Draw 12.5W (2.5A) [1]	25, 26	5.0V Main Power Supply
VBAT	I	Draw 120 nW (40nA)	24	Backup Power for RTC
VDD_3V3_OUT	O	Deliver 6.6W (2A)	91, 92, 93, 94	3.3V voltage source for external circuity. VDD_3V3_OUT goes high after the SOM voltages have stabilized and X_PGOOD goes high.
SoC_VDDSHV5_SDIO	O	Deliver 0.33W (100mA)	23	This rail can be used as a pullup voltage for the SD/MMC1 signals. The level of SoC_VDDSHV5_SDIO is driven by VSEL_SD to either 3.3V or 1.8V.

GND	O	None	189-236, 247-270	Ground

[1:] If your custom carrier board design will not use VDD_3V3_OUT, then the power draw will be 6.25W (1.25A)

5.1 Primary System Power (VIN)

The phyCORE-AM62Ax DSC SOM operates from a primary voltage supply (VIN) with a nominal value of +5V. On-board PMIC and switching regulators generate the additional voltage supplies required by the phyCORE-AM62Ax DSC and on-board components from VIN supplied to the SOM.

For proper operation, the phyCORE-AM62Ax DSC SOM must be supplied with a voltage source of 5V (±5 %) with a minimum 2.5A capacity at the VIN pins on the DSC footprint (if you do not plan to use VDD_3V3_OUT in your custom CB design only 1.25A of capacity is required). These pins are 25 and 26 on the X1 connector. In testing the current draw of the SOM did not exceed 1.25A, but it is important to perform a power analysis to determine how much current your complete system (both SOM and custom CB) requires. The phyCORE-AM62Ax DSC Carrier Board provides an easy access current shunt to measure SOM current under various operating conditions as part of your system power analysis. The reference designator of the shunt is R492 and has a value of 15 mΩ (and a size of 1206). Use the maximum measured SOM current combined with the current requirement for your carrier board peripheral devices to design your power system appropriately.

Connect all +5V VIN input pins to your power supply and all ground pins to ground.

5.1.1 Primary Power Reference Circuit

An example reference circuit for powering the SOM is shown below.

Figure 15. Primary Power VIN(VCC_5V0_MAIN) reference circuit

The circuit consists of:

- A USB-C connector for connecting an external USB-C power cable to the system
- A diode circuit (D49) that will trip in case of an overload preventing damage to the rest of the circuit

The reference circuits below showcase additional functionality that can be added to the primary power circuit. *Figure 16* is a circuit for measuring the input current to the SOM. It contains:

- A small resistor (R492) that the current is measured across
- A connector to connect to a current measurement board

Figure 16. SOM current reader reference circuit

Figure 17 is an alternative input power for industrial applications. It also contains a protection circuit that prevents overloads in current/voltage from damaging the SOM. It contains:

- A phoenix connector for connecting a 5V external power source to the system
- A fuse/diode circuit (F1/D5) that will trip in case of an overload preventing damage to the rest of the circuit
- A transistor network that provides reverse polarity protection

Figure 17. Phoenix connector power input with overload protection reference circuit

5.2 Backup Power (VBAT)

To keep the Real-Time Clock (RTC) module running, a secondary voltage source of 1.2-5.5V can be supplied to the phyCORE-AM62Ax DSC SOM at the VBAT pin (pin 24 of DSC footprint X1). For the RTC to maintain time when main system power is removed, the VBAT input must be supplied with power. The RTC draws 40 nA at 3V and is the only draw on VBAT. For more information regarding the recommended operating voltage of the Backup Power Source VBAT, refer to *Table 4*.

5.3 Reset

Several reset inputs and outputs are accessible at the DSC footprint as listed in *Table 14* below. The X_nRESET_IN, X_MCU_RESETz, and X_RESET_REQz signals can be driven low to trigger cold/warm resets of different domains without cycling power on the carrier board. We recommend designing reset buttons into your system that will tie the reset signals to ground when pressed, allowing for manual control over system reset. These buttons can later be depopulated for production purposes but are generally useful during board bring up and verification.

The X_PMIC_EN signal is connected to the enable pin of the PMIC and will prevent the PMIC from starting when pulled low. The X_MCU_RESETSTATz, X_RESETSTATz, X_PORz_OUT, and X_PGOOD signals are status outputs. PGOOD indicates when the SOM power is stable and X_MCU_RESETSTATz / X_RESETSTATz / X_PORz_OUT are status outputs for X_MCU_RESETz / X_RESET_REQz / X_nRESET_IN respectively.

Most of the reset signals are connected to pullups/pulldowns (X_nRESET_IN also has an attached capacitor) so pullups/pulldowns are not needed on custom CBs for these signals. This information is in *Table 14* as well as shown in the figure below.

Figure 18. Reset signals pullups, pulldowns, and capacitors populated on the SOM

Table 14 Reset Pin Description

X1 Pin #	Signal	Type	Level	Description
182	X_PMIC_EN (100K pullup on SOM)	I	5V	Enable pin for PMIC
183	X_nRESET_IN (10K pullup on SOM)	I	3.3V	Cold system Reset
186	X_MCU_RESETz (100K pullup on SOM)	I	3.3V[1]	Warm Reset of MCU Domain
188	X_RESET_REQz (100K pullup on SOM)	I	3.3V[1]	Warm Reset of MAIN Domain

185	X_MCU_RESETSTATz (10K pulldown on SOM)	O	3.3V[1]	MCU Domain Reset Status Output
187	X_PORz_OUT (1.5K pulldown on SOM)	O	3.3V[1]	Cold Reset Status Output
180	X_RESETSTATz (10K pulldown on SOM)	O	3.3V[1]	MAIN Domain Reset Status Output
184	X_PGOOD (100K pullup on SOM)	OD-O	3.3V	SOM/PMIC Power Good Status Output
241	X_VPP_EN (10K pulldown on SOM)	I	3.3V	Enable pin for VPP rail

[1:] The voltage level for this signal is configurable for 1.8V or 3.3V. The default voltage level is listed here, but always check the actual jumper setting for the applicable SOM configuration. Refer to section *4.6 Solder Jumpers* for details.

5.4 Power Sequencing

It is mandatory to avoid driving the I/O pins of the phyCORE-AM62Ax DSC SOM when the SOM is not fully powered up. Prematurely driving the pins may cause current to flow through the I/O pins before the processor is properly powered, potentially resulting in damage or unknown behavior after power-up or reset. Therefore, the peripheral carrier board power should be switched on/enabled by the X_PGOOD signal to avoid powering external peripherals and circuits that directly interface with the phyCORE-AM62Ax DSC SOM I/Os until their respective voltage domains are powered. X_PGOOD is a 3.3V level signal that is pulled high once the PMIC has finished its power sequencing and the SOM has been powered on. This should be used to sequence the baseboard power supplies (3.3V, 1.8V, etc.). This ensures that the I/O domains on the SOM are powered before any external circuits or peripherals drive power to the processor pins. To accomplish this, it is recommended to integrate load switches to turn on the peripheral voltage rails after the SOM has finished powering up or use VDD_3V3_OUT to power the peripherals. An example of this is shown in the reference circuit below.

Figure 19. Carrier board power reference circuit

5.5 Safe Shutdown and Sudden Power Loss

Like a PC, a sudden power loss can result in a corrupted filesystem that renders your system unable to boot. When possible, initiating an OS controlled shutdown procedure is advised. Under Linux a poweroff or shutdown command will safely shutdown the system, allowing subsequent safe removal of power.

If sudden power loss is a concern in your system, then consider designing a battery backup or other similar failsafe solution. An appropriate battery backup provides enough temporary power for the system to complete a safe shutdown. The safe shutdown should be triggered via an interrupt to the processor when primary system power loss is detected. Another solution is to have a read-only file system as this would ensure nothing is modified in an unexpected manner in the event of an unexpected shutdown.

6 System Memory

The following sub-sections detail each memory type supported on the phyCORE-AM62Ax DSC as well as how to configure which memory system to boot from. This section is split into memories populated on the SOM and potential CB memory interfaces.

6.1 SOM Memory

6.1.1 LPDDR4 RAM

The RAM on the phyCORE-AM62Ax DSC is comprised of one LPDDR4 SDRAM chip for a 32-bit wide interface providing up to 4GB of SDRAM which can run at up to 4266Mb/s/pin. These chips are connected to the dedicated DDR subsystem of the AM62Ax SOC processor. Typically, the LPDDR4 SDRAM initialization is performed by a bootloader or operating system following a power-on reset and must not be changed at a later point by any application code. When writing custom code independent of an operating system or bootloader, SDRAM must be initialized through the appropriate SDRAM configuration registers on the AM62Ax SOC processor. Refer to the AM62Ax Technical Reference Manual about accessing and configuring these registers. Contact our sales team for information on the available LPDDR4 population options: https://PHYTEC.com/contact/

6.1.2 EEPROM

The phyCORE-AM62Ax DSC is populated with one nonvolatile 32KB EEPROM with an I^2C interface. This memory can be used to store configuration data or other general-purpose data. The device is accessed through the I2C0 on the AM62Ax SOC at address 0x50.

6.1.3 eMMC Flash

An eMMC flash device is populated on the SOM as a programmable nonvolatile storage. The eMMC flash is connected to the MMC0 8-bit interface of the phyCORE-AM62Ax DSC which supports the JEDEC eMMC electrical standard v5.1. Contact our sales team for information on the available eMMC population options: https://PHYTEC.com/contact/

6.1.4 OSPI

An Octal Serial Peripheral Interface (OSPI) Flash is populated on the SOM as a programmable nonvolatile storage. The OSPI interface supports single, dual, quad, or octal read/write access to the flash device. The OSPI Flash can be used for a fast boot. Contact our sales team for information on the available OSPI population options: https://PHYTEC.com/contact/

Some of the OSPI signals on the SOM are worth noting since their use on the SOM either does not match their processor ball name or are used for an entirely different circuit. OSPI0_CSN3 is used for the OSPI reset, OSPI0_CSN1 is used as the EEPROM Write Protect (WP) pin, and OSPI2_CSN is connected to the OSPI interrupt pin or the heartbeat LEDs discussed in section *12.5 Heartbeat LEDs.* This information is also shown in the figure below.

Figure 20. OSPI0 CSN signal use

6.2 External Memory Bus

6.2.1 GPMC

The General-Purpose Memory Control (GPMC) module can be used as a data path to an external memory device. The GPMC can support:

- An asynchronous or synchronous 8-bit memory or device (non-burst device)
- An asynchronous or synchronous 16-bit memory or device
- A 16-bit non-multiplexed NOR Flash device
- A 16-bit address and data multiplexed NOR Flash device
- An 8-bit and 16-bit NAND flash device
- A 16-bit pseudo-SRAM device

Table 15 GPMC Signal Connections at the SOC footprint

Processor Signal	X1 Pin #(s)	SOM Signal(s)	Type	Level	Description
GPMC0_ADVn_ALE	174	X_GPMC0_ADVn_ALE	O	3.3V[1]	GPMC Address Valid (active low) or Address Latch Enable
GPMC0_CLK	22	X_GPMC0_CLK	O	3.3V[1]	GPMC clock
GPMC0_DIR	21	X_GPMC0_DIR	O	3.3V[1]	GPMC Data Bus Signal Direction Control
GPMC0_OEn_REn	178	X_GPMC0_OEn_REn	O	3.3V[1]	GPMC Output Enable (active low) or Read Enable (active low)
GPMC0_WEn	179	X_GPMC0_WEn	O	3.3V[1]	GPMC Write Enable (active low)
GPMC0_WPn	177	X_GPMC0_WPn	O	3.3V[1]	GPMC Flash Write Protect (active low)
GPMC0_A0	46	X_VOUT0_DATA0	O	3.3V[1]	GPMC Address 0 Output
GPMC0_A1	45	X_VOUT0_DATA1	O	3.3V[1]	GPMC Address 1 Output
GPMC0_A2	44	X_VOUT0_DATA2	O	3.3V[1]	GPMC Address 2 Output
GPMC0_A3	43	X_VOUT0_DATA3	O	3.3V[1]	GPMC Address 3 Output
GPMC0_A4	42	X_VOUT0_DATA4	O	3.3V[1]	GPMC Address 4 Output
GPMC0_A5	41	X_VOUT0_DATA5	O	3.3V[1]	GPMC Address 5 Output
GPMC0_A6	40	X_VOUT0_DATA6	O	3.3V[1]	GPMC Address 6 Output
GPMC0_A7	39	X_VOUT0_DATA7	O	3.3V[1]	GPMC Address 7 Output
GPMC0_A8	38	X_VOUT0_DATA8	O	3.3V[1]	GPMC Address 8 Output
GPMC0_A9	37	X_VOUT0_DATA9	O	3.3V[1]	GPMC Address 9 Output
GPMC0_A10	36	X_VOUT0_DATA10	O	3.3V[1]	GPMC Address 10 Output
GPMC0_A11	35	X_VOUT0_DATA11	O	3.3V[1]	GPMC Address 11 Output
GPMC0_A12	34	X_VOUT0_DATA12	O	3.3V[1]	GPMC Address 12 Output
GPMC0_A13	33	X_VOUT0_DATA13	O	3.3V[1]	GPMC Address 13 Output
GPMC0_A14	32	X_VOUT0_DATA14	O	3.3V[1]	GPMC Address 14 Output
GPMC0_A15	31	X_VOUT0_DATA15	O	3.3V[1]	GPMC Address 15 Output
GPMC0_A16	30	X_VOUT0_HSYNC	O	3.3V[1]	GPMC Address 16 Output
GPMC0_A17	28	X_VOUT0_DE	O	3.3V[1]	GPMC Address 17 Output
GPMC0_A18	29	X_VOUT0_VSYNC	O	3.3V[1]	GPMC Address 18 Output
GPMC0_A19	27	X_VOUT0_PCLK	O	3.3V[1]	GPMC Address 19 Output
GPMC0_A20	175	X_GPMC0_CSn3	O	3.3V[1]	GPMC Address 20 Output
GPMC0_A21	176	X_GPMC0_WAIT1	O	3.3V[1]	GPMC Address 21 Output
GPMC0_A22	177	X_GPMC0_WPn	O	3.3V[1]	GPMC Address 22 Output
GPMC0_AD0	4	X_GPMC0_AD0/BOOTMODE_0[3] (100K pullup on SOM)	I/O	3.3V[1]	GPMC Data 0 Input/Output
GPMC0_AD1	5	X_GPMC0_AD1/BOOTMODE_1[3] (100K pullup on SOM)	I/O	3.3V[1]	GPMC Data 1 Input/Output
GPMC0_AD2	6	X_GPMC0_AD2/BOOTMODE_2[3] (100K pulldown on SOM)	I/O	3.3V[1]	GPMC Data 2 Input/Output
GPMC0_AD3	7	X_GPMC0_AD3/BOOTMODE_3[3] (100K pullup on SOM)	I/O	3.3V[1]	GPMC Data 3 Input/Output
GPMC0_AD4	8	X_GPMC0_AD4/BOOTMODE_4[3] (100K pulldown on SOM)	I/O	3.3V[1]	GPMC Data 4 Input/Output
GPMC0_AD5	9	X_GPMC0_AD5/BOOTMODE_5[3] (100K pulldown on SOM)	I/O	3.3V[1]	GPMC Data 5 Input/Output
GPMC0_AD6	10	X_GPMC0_AD6/BOOTMODE_6[3] (100K pullup on SOM)	I/O	3.3V[1]	GPMC Data 6 Input/Output
GPMC0_AD7	11	X_GPMC0_AD7/BOOTMODE_7[3] (100K pulldown on SOM)	I/O	3.3V[1]	GPMC Data 7 Input/Output

Processor Signal	X1 Pin #(s)	SOM Signal(s)	Type	Level	Description
GPMC0_AD8	12	X_GPMC0_AD8/BOOTMODE_8[3] (100K pullup on SOM)	I/O	3.3V[1]	GPMC Data 8 Input/Output
GPMC0_AD9	13	X_GPMC0_AD9/BOOTMODE_9[3] (100K pullup on SOM)	I/O	3.3V[1]	GPMC Data 9 Input/Output
GPMC0_AD10	14	X_GPMC0_AD10/BOOTMODE_10[3] (100K pullup on SOM)	I/O	3.3V[1]	GPMC Data 10 Input/Output
GPMC0_AD11	15	X_GPMC0_AD11/BOOTMODE_11[3] (100K pulldown on SOM)	I/O	3.3V[1]	GPMC Data 11 Input/Output
GPMC0_AD12	16	X_GPMC0_AD12/BOOTMODE_12[3] (100K pullup on SOM)	I/O	3.3V[1]	GPMC Data 12 Input/Output
GPMC0_AD13	17	X_GPMC0_AD13/BOOTMODE_13[3] (100K pullup on SOM)	I/O	3.3V[1]	GPMC Data 13 Input/Output
GPMC0_AD14	18	X_GPMC0_AD14/BOOTMODE_14[3] (100K pulldown on SOM)	I/O	3.3V[1]	GPMC Data 14 Input/Output
GPMC0_AD15	19	X_GPMC0_AD15/BOOTMODE_15[3] (100K pulldown on SOM)	I/O	3.3V[1]	GPMC Data 15 Input/Output
GPMC0_BE0n_CLE	173	X_GPMC0_BE0n_CLE	O	3.3V[1]	GPMC Lower-Byte Enable (active low) or Command Latch Enable
GPMC0_BE1n	172	X_GPMC0_BE1n	O	3.3V[1]	GPMC Upper-Byte Enable (active low)
GPMC0_CSn0	3	X_GPMC0_CSn0	O	3.3V[1]	GPMC Chip Select 0 (active low)
GPMC0_CSn1	2	X_GPMC0_CSn1	O	3.3V[1]	GPMC Chip Select 1 (active low)
GPMC0_CSn2	1	X_GPMC0_CSn2	O	3.3V[1]	GPMC Chip Select 2 (active low)
GPMC0_CSn3	175	X_GPMC0_CSn3	O	3.3V[1]	GPMC Chip Select 3 (active low)
GPMC0_WAIT0	20	X_GPMC0_WAIT0	I	3.3V[1]	GPMC External Indication of Wait
GPMC0_WAIT1	176	X_GPMC0_WAIT1	I	3.3V[1]	GPMC External Indication of Wait

[1:] The voltage level for this signal is configurable for 1.8V or 3.3V. The default voltage level is listed here, but always check the actual jumper setting for the applicable SOM configuration. Refer to section *4.6 Solder Jumpers* for details.
[3:] This signal should not be driven during reset. More information can be found in section *6.3 System Boot Configuration.*

6.2.2 SD/MMC/SDIO

The AM62Ax SOC processor provides three Secure Digital/MultiMedia Card interfaces as MMC0, MMC1, and MMC2. Only MMC1(SDIO) and MMC2 are accessible at the SOC footprint as the MMC0 interface is connected to the on-board eMMC. The MMC1/MMC2 ports provides a 4-bit wide data bus that supports SD Host Controller Standard Specification 4.10, SD Physical Layer Specification v3.01, and SDIO Specification v3.00.

6.2.2.1 MMC Pinout

Table 16 MMC Connections at the SOC footprint

SOM Signal(s)	X1 Pin #(s)	Type	Level	Description
X_MMC1_SDCD (10K pullup on SOM)	157	I	3.3V[1]	MMC1 Card Detection
X_MMC1_SDWP (10K pullup on SOM)	156	I	3.3V[1]	MMC1 Write Protect
X_MMC1_DAT3	162	I/O	3.3V[1]	MMC1 Data 3
X_MMC1_DAT2	161	I/O	3.3V[1]	MMC1 Data 2
X_MMC1_DAT1	160	I/O	3.3V[1]	MMC1 Data 1
X_MMC1_DAT0	159	I/O	3.3V[1]	MMC1 Data 0
X_MMC1_CLK (49.9K pulldown on SOM)	158	I/O	3.3V[1]	MMC1 Clock
X_MMC1_CMD	163	I/O	3.3V[1]	MMC1 Command
X_MMC2_SDCD (10K pullup on SOM)	138	I	3.3V[1]	MMC2 Card Detection
	165			
	146			
X_MMC2_SDWP (10K pullup on SOM)	147	I	3.3V[1]	MMC2 Write Protect
	139			
	164			
X_MMC2_DAT3	170	I/O	3.3V[1]	MMC2 Data 3
X_MMC2_DAT2	169	I/O	3.3V[1]	MMC2 Data 2
X_MMC2_DAT1	168	I/O	3.3V[1]	MMC2 Data 1
X_MMC2_DAT0	167	I/O	3.3V[1]	MMC2 Data 0
X_MMC2_CLK (49.9K pulldown on SOM)	166	I/O	3.3V[1]	MMC2 Clock
X_MMC2_CMD	171	I/O	3.3V[1]	MMC2 Command

[1]: *The voltage level for these signals is configurable between 1.8V and 3.3V. The default voltage level is listed here, but always check the actual jumper setting for the applicable SOM configuration. Refer to* section *4.6 Solder Jumpers for details.*

6.2.2.2 MMC Design In Considerations

- MMC signals should be length matched within 12700 µm as described in *Table 17*.
- Keep MMC trace lengths as short as possible.
- Route the MMC clock with enough clearance from other signals, when possible, to reduce crosstalk. A general rule is to use a clearance of at least 3 times the trace width.
- It is recommended to place series termination resistors (22Ω or similar is recommended) near the SD card reader/WIFI module on the data and command signals.
- SD card power should be connected to a 3.3V power supply regardless of the MMC IO voltage level.
- SD card power needs to be toggled with SoC warm reset status (in our reference design we use X_RESETSTATz).

Table 17 phyCORE-AM62Ax DSC MMC1 Layout Characteristics

Signal Name	SOM Trace Length (µm)	Length Matching (µm)	Single Ended Impedance (Ω)
X_MMC1_DAT3	26542	12700	50
X_MMC1_DAT2	25329		
X_MMC1_DAT1	25672		
X_MMC1_DAT0	25262		
X_MMC1_CLK	28221		
X_MMC1_CMD	25234		
X_MMC2_DAT3	23578	12700	50
X_MMC2_DAT2	23193		
X_MMC2_DAT1	23366		
X_MMC2_DAT0	23174		
X_MMC2_CLK	26157		
X_MMC2_CMD	23937		

6.2.2.3 MMC Reference Circuit

Two reference circuits using MMC are shown in the figures below. The first connects the MMC1 signals to a micro-SD card reader for use as either a data storage device or a boot device.

Figure 21. MMC1 SD-card Reader Reference Schematic

Figure 22. MMC1 Load Switch Reference Schematic

The circuit consists of:

- An SD-card reader with CMD/DATA line pullups
- A load switch

The second reference circuit connects MMC2 to a E key M.2 connector for use in WIFI/BT applications.

Figure 23. M.2 WIFI MMC2 Connector Reference Schematic

Figure 24. M.2 WIFI MMC2 Level Translators Reference Schematic

The circuit consists of:

- A E key M.2 connector to connect to a module
- Two voltage translators that serve as buffers for the bootmode signals with jumpers allowing the module to operate at either 3.3V or 1.8V.
- A 32.768KHz oscillator

6.3 System Boot Configuration

Although most features of the phyCORE-AM62Ax DSC SOM are configured or programmed during the initialization routine, other features which impact program execution must be configured prior to initialization via pin termination. During the power-on reset cycle, the operational system boot mode of the phyCORE-AM62Ax DSC SOM is determined by the configuration of the BOOTMODE [15:0] signals. The BOOTMODE signals must be held at the desired configuration until X_PORz_OUT goes high to be properly latched into the system. For development and debugging purposes, the BOOTMODE pins are available at the DSC footprint and are named X_GPMC0_AD#/BOOTMODE#. These signals are strapped to default values using on-board resistors. *Table 18* below lists the various BOOTMODE configurations as well as the default configuration on the SOM, which is to boot from eMMC with SD card as a backup. Further BOOTMODE options are discussed in the AM62Ax Technical Reference Manual.

Figure 25. BOOTMODE pullups/pulldowns

Table 18 BOOTMODE Description

BOOTMODE pins	Description	Pin Settings	Pin Behavior
BOOTMODE[15:14]	Reserved by the processor	XX	None
BOOTMODE[13:10]	Backup boot mode selection	X000	None
		0001	USB device mode
		1001	USB host mode
		X011	UART
		0100	Ethernet RGMII with internal TX delay
		1100	Ethernet RMII with external clock source
		0101	MMC0
		1101 (Default)	MMC1
		X110	SPI
		X111	I^2C
BOOTMODE[9:3]	Primary boot mode selection and config	X00_0001	OSPI boot, Iclock is external, Boot flash is off
		X01_0001	OSPI boot, Iclock is internal, Boot flash is off
		X10_0001	OSPI boot, Iclock is external, Boot flash is on
		X11_0001	OSPI boot, Iclock is internal, Boot flash is oon
		0XX_1001 (Default)	eMMC boot
		1X0_1000	SDIO boot in filesystem mode
		1X1_1000	SDIO boot in raw mode
BOOTMODE[2:0]	PLL Reference Clock selection	000	19.2 MHz
		001	20 MHz
		010	24 MHz
		011 (Default)	25 MHz
		100	26 MHz
		101	27 MHz

[1:] X means the pin is reserved by the processor and must be tied either high or low. The direction doesn't matter as long as the pin is not left floating.

To modify the default boot configuration on a custom carrier board, it is recommended to use 1kΩ pull-up resistors or 10kΩ pull-down resistors to override the SOM settings. For startup/verification testing, PHYTEC recommends designing the boot configuration circuit to include a DIP switch. This will make it easy to swap between various boot modes (an example circuit is shown below). This DIP switch can then be de-populated for production.

Figure 26. Reference Schematic for BOOTMODE configuration

7 Serial Interfaces

The following sub-sections detail each of the serial interfaces supported on the phyCORE-AM62Ax DSC.

7.1 CAN

The phyCORE-AM62Ax DSC SOM provides three Controller Area Network (MCAN) ports. The CAN interfaces support CAN and CAN FD (flexible data-rate) specifications, conforming with CAN protocol version 2.0 part A, B and ISO 11898-1:2015.

7.1.1 CAN Pinout

Table 19 MCAN Connections at the SOC footprint

X1 Pin #(s)	SOM Signal(s)	Type	Level	Description
142	X_MCAN0_RX	I	3.3V[1]	MCAN0 Receive Data
143	X_MCAN0_TX	O	3.3V[1]	MCAN0 Transmit Data
115	X_MCU_MCAN0_RX	I	3.3V[1]	MCU_MCAN0 Receive Data
116	X_ MCU_MCAN0_TX	O	3.3V[1]	MCU_MCAN0 Transmit Data
117	X_MCU_MCAN1_RX	I	3.3V[1]	MCU_MCAN1 Receive Data
118	X_ MCU_MCAN1_TX	O	3.3V[1]	MCU_MCAN1 Transmit Data

[1]: The voltage level for this signal is configurable for 1.8V or 3.3V. The default voltage level is listed here, but always check the actual jumper setting for the applicable SOM configuration. Refer to section *4.6 Solder Jumpers* for details

7.1.2 CAN Reference Circuit

An example reference circuit for connecting the MCAN0 signals to a 2X5 connector is shown below.

Figure 27. MCAN0 Reference Schematic

The circuit consists of:

- A 2x5 2.54mm pitch header
- A CAN FD Transceiver to convert the MCAN0 signals into differential CAN bus signal levels

7.2 Ethernet

The phyCORE-AM62Ax DSC SOM brings out two external 10/100/1000 Mbps Ethernet ports:

- One is translated on the SOM by a DP83867IRRGZ Ethernet PHY (a robust, low power transceiver) into the Media Dependent Interface (MDI) differential Ethernet data pairs that are accessible at the DSC footprint. This Ethernet PHY:
  - Supports 10-BASE-Te, 100BASE-TX, and 1000BASE-T protocols to interface directly to twisted pair media through an external transformer.
  - Provides two LED control outputs and one GPIO signal. The GPIO and LED I/O also serve as bootstrap pins for PHY configuration. Be careful to avoid pulling or driving these signals during power up and reset.
- The other, CPSW_RGMII2, is brought out as RGMII/RMII

The on-board Ethernet PHY offers several default configuration options that include settings such as the PHY address and RGMII clock skew. Options such as these can be set via external strapping resistors which are described in the datasheet. The table below lists the default Ethernet PHY strapping configuration; however, these settings can be changed via the register settings of the PHY if necessary. Refer to the DP83867IRRGZ datasheet for further details on these configuration and strapping options (DP83867IRRGZ Datasheet).

NOTE:
Adjusting strapping options and PHY registers is not necessary when using PHYTEC provided BSPs.

Table 20 Ethernet PHY Default Strapping Configuration

Strapping Option	Default Setting	Strapping Signals
PHY Address	1	CPSW_RGMII1_RD0 CPSW_RGMII1_RD2
Mirror Mode	Disabled	CPSW_ETH0_LED0
Auto-negotiation	Enabled (advertise ability of 10/100/1000)	CPSW_RGMII1_RX_CTL
RGMII TX Clock Skew	2 ns	CPSW_ETH0_LED1 CPSW_ETH0_LED2
RGMII RX Clock Skew	2 ns	X_CPSW_ETH0_GPIO_0 X_CPSW_ETH0_GPIO_1

7.2.1 Ethernet Pinout

Table 21 Ethernet Connections at the SOC footprint

Processor Signal	X1 Pin #(s)	SOM Signal(s)	Type	Level	Description
-	62	X_CPSW_ETH0_LED_ACTIVITY	OD	3.3V	LED Link Signal
-	71	X_CPSW_ETH0_LED_LINK	OD	3.3V	LED Activity Signal
-	61	X_CPSW_ETH0_GPIO_0	I/O	3.3V[1]	SOM Ethernet PHY GPIO 0
-	72	X_CPSW_ETH0_nINT	I/O	3.3V[1]	SOM Ethernet PHY Interrupt (active low, 2.2K pullup on SOM)

Processor Signal	X1 Pin #(s)	SOM Signal(s)	Type	Level	Description
-	70	X_CPSW_ETH0_A+	ETH_I/O	Differential	Ethernet Data A Positive
-	69	X_CPSW_ETH0_A-	ETH_I/O	Differential	Ethernet Data A Negative
-	68	X_CPSW_ETH0_B+	ETH_I/O	Differential	Ethernet Data B Positive
-	67	X_CPSW_ETH0_B-	ETH_I/O	Differential	Ethernet Data B Negative
-	66	X_CPSW_ETH0_C+	ETH_I/O	Differential	Ethernet Data C Positive
-	65	X_CPSW_ETH0_C-	ETH_I/O	Differential	Ethernet Data C Negative
-	64	X_CPSW_ETH0_D+	ETH_I/O	Differential	Ethernet Data D Positive
-	63	X_CPSW_ETH0_D-	ETH_I/O	Differential	Ethernet Data D Negative
MDIO0_MDIO	48	X_MDIO0_MDIO (1.5K pullup on SOM)	I/O	3.3V[1]	CPSW Management Data IO
MDIO0_MDC	47	X_MDIO0_MDC (1.5K pullup on SOM)	O	3.3V[1]	CPSW Management Data Clock
RGMII2_RX_CTL	49	X_CPSW_RGMII2_RX_CTL	I	3.3V[1]	CPSW RGMII2 Receive Control
RGMII2_RXC	50	X_CPSW_RGMII2_RXC	I	3.3V[1]	CPSW RGMII2 Receive Clock
RGMII2_RD0	54	X_CPSW_RGMII2_RD0	I	3.3V[1]	CPSW RGMII2 Receive Data 0
RGMII2_RD1	53	X_CPSW_RGMII2_RD1	I	3.3V[1]	CPSW RGMII2 Receive Data 1
RGMII2_RD2	52	X_CPSW_RGMII2_RD2	I	3.3V[1]	CPSW RGMII2 Receive Data 2
RGMII2_RD3	51	X_CPSW_RGMII2_RD3	I	3.3V[1]	CPSW RGMII2 Receive Data 3
RGMII2_TX_CTL	55	X_CPSW_RGMII2_TX_CTL	O	3.3V[1]	CPSW RGMII1 Transmit Control
RGMII2_TXC	56	X_CPSW_RGMII2_TXC	I/O	3.3V[1]	CPSW RGMII1 Transmit Clock
RGMII2_TD0	57	X_CPSW_RGMII2_TD0	O	3.3V[1]	CPSW RGMII1 Transmit Data 0
RGMII2_TD1	58	X_CPSW_RGMII2_TD1	O	3.3V[1]	CPSW RGMII1 Transmit Data 1
RGMII2_TD2	59	X_CPSW_RGMII2_TD2	O	3.3V[1]	CPSW RGMII1 Transmit Data 2
RGMII2_TD3	60	X_CPSW_RGMII2_TD3	O	3.3V[1]	CPSW RGMII1 Transmit Data 3
RMII2_CRS_DV	56	X_CPSW_RGMII2_TXC	I	3.3V[1]	RMII2 Carrier Sense / Data Valid
RMII2_REF_CLK	50	X_CPSW_RGMII2_RXC	I	3.3V[1]	RMII Reference Clock
RMII2_RX_ER	49	X_CPSW_RGMII2_RX_CTL	I	3.3V[1]	RMII2 Receive Data Error
RMII2_TX_EN	55	X_CPSW_RGMII2_TX_CTL	O	3.3V[1]	RMII2 Transmit Enable
RMII2_RXD0	54	X_CPSW_RGMII2_RD0	I	3.3V[1]	RMII2 Receive Data 0
RMII2_RXD1	53	X_CPSW_RGMII2_RD1	I	3.3V[1]	RMII2 Receive Data 1
RMII2_TXD0	57	X_CPSW_RGMII2_TD0	O	3.3V[1]	RMII2 Transmit Data 0
RMII2_TXD1	58	X_CPSW_RGMII2_TD1	O	3.3V[1]	RMII2 Transmit Data 1

[1]: The voltage level for this signal is configurable for 1.8V or 3.3V. The default voltage level is listed here, but always check the actual jumper setting for the applicable SOM configuration. Refer to section *4.6 Solder Jumpers* for details.
[2]: The signal brought out at this pin is controlled by a jumper. Refer to section *4.6 Solder Jumpers* for details.

7.2.2 Ethernet Design In Guide

7.2.2.1 CPSW_ETH0 Ethernet Design In Considerations

- Connecting the phyCORE-AM62Ax DSC SOM to an existing 10/100/1000Base-T network involves adding an RJ45 and appropriate magnetic devices in the design. See the reference circuit in section *7.2.3 Ethernet Reference Circuits* for an example.
- Avoid any other signal lines crossing the Ethernet signals.
- More general differential pair routing guidelines are in section *4.10.1 High-Speed Differential Signal Routing Guidelines.*

Table 22 phyCORE-AM62Ax DSC CPSW_ETH0 Layout Characteristics

Signal Name	Length (µm)			Intrapair Length Matching (µm)	Interpair Length Matching (µm)	Single Ended Impedance (Ω)	Differential Impedance (Ω)
	SOM Trace	Max Total	Max CB Trace				
X_CPSW_ETH0_A-	6152	101600	95448	254	2000	~50	100
X_CPSW_ETH0_A+	6154	101600	95446			~50	
X_CPSW_ETH0_B-	6197	101600	95403	254	2000	~50	100
X_CPSW_ETH0_B+	6204	101600	95396			~50	
X_CPSW_ETH0_C-	6230	101600	95370	254	2000	~50	100
X_CPSW_ETH0_C+	6211	101600	95389			~50	
X_CPSW_ETH0_D-	6275	101600	95325	254	2000	~50	100
X_CPSW_ETH0_D+	6264	101600	95336			~50	

7.2.2.2 RGMII Design In Considerations

- Place the Ethernet PHY as close as possible to the SOM connector and keep the trace lengths of the RGMII signals as short as possible.
- Add a 10kΩ pull-down resistor on any unused input or I/O signal on this interface if it is not connected to a PHY.
- Avoid any cuts in the ground plane or other references planes within the RGMII routing region.
- Place termination resistors (recommended to use 0Ω) near the PHY on all the RGMII RX* signals.
- The MDIO clock and data signals do not need to be matched as strictly as RGMII. However, it is recommended to route these together and keep them length matched within 2540 µm.
- RGMII v2.0 Timing Requirements (shown in the table below) specify that the clock and data will be generated simultaneously by the transmitting source, which requires a skew be introduced between clock and data.

Table 23 phyCORE-AM62Ax DSC RGMII Timing Requirements

Parameter	Minimum	Typical	Maximum	Units
Data to clock output skew at transmitter	-500	0	500	ps
Data to clock output skew at receiver	1	1.8	2.6	ns

The skew can be introduced with additional PCB trace delay added to the clock signal on the carrier board or by adjusting the internal delay settings at the PHY or processor. However, please note that an internal delay may not be available on your selected ethernet PHY or it may not have sufficient adjustment to account for the required skew. The skew between the clock and each individual data and control signal should not fall below the 1ns minimum or exceed the 2.6ns maximum.

Ensure signals are properly length matched to meet these RGMII timing specifications. The following tables show the signal groups (TX vs. RX) that should be length matched and the trace length of each signal on the SOM. It is recommended to length match the control and data signals within 2540 µm, and then the trace length of the clock should be the average

length of these control and data signals plus an additional 1.8ns delay. The recommended clock trace length on a carrier board is calculated using the following equation:

(Average total length of control/data signals on SOM) + (Average total length of control/data signals on Carrier Board) + (1.8ns delay) – (Clock Trace Length on the SOM)

An example of using this equation to calculate the recommended clock lengths when implementing a physical delay for RGMII2 is shown in the equations below. The 1.8ns was translated to an estimated length using the general rule of 6.5ps/mm. However, the actual physical trace delay will vary depending on the PCB stackup, materials, etc.

- Transmit Clock Length Calculation with Physical Trace Delay: (22847 µm) + (Average total length of control/data signals on Carrier Board) + (276860 µm) – (22887 µm)
- Receive Clock Length Calculation with Physical Trace Delay: (22910 µm) + (Average total length of control/data signals on Carrier Board) + (276860 µm) – (22757 µm)

Table 24 phyCORE-AM62Ax DSC RGMII2 Trace Length Characteristics

Signal Name	SOM Trace Length (µm)			Match Group	Recommended Length Match
	SOM Trace	Max Total	Max CB Trace		
RGMII2_TXC	19042	120000	100958	RGMII2 Transmit	AVERAGE_LENGTH(TXCTL, TXD0, TXD1, TXD2, TXD3) + 1.8ns
RGMII2_TXCTL	19052	120000	100948		2540 µm
RGMII2_TD0	18951	120000	101049		
RGMII2_TD1	19204	120000	100796		
RGMII2_TD2	19018	120000	100982		
RGMII2_TD3	19019	120000	100981		
RGMII2_RXC	23136	120000	96864	RGMII2 Receive	AVERAGE_LENGTH(RXCTL, RXD0, RXD1, RXD2, RXD3) + 1.8ns
RGMII2_RXCTL	23473	120000	96527		2540 µm
RGMII2_RD0	23351	120000	96649		
RGMII2_RD1	23302	120000	96698		
RGMII2_RD2	22992	120000	97008		
RGMII2_RD3	23063	120000	96937		

7.2.3 Ethernet Reference Circuits

Example reference circuits for connecting the CPSW_RGMII1 differential signals from the on-board PHY to an RJ45 connector and CPSW_RGMII2 signals to an Ethernet PHY are shown below.

Figure 28. RJ45 Reference Schematic

The circuit consists of:

- An Ethernet Jack
- Two TVS diode arrays for ESD protection
- Two resistor networks to manage the Ethernet LEDs in the jack

Figure 29. RGMII PHY RJ45 Reference Schematic

Figure 30. RGMII PHY Strapping Resistors Reference Schematic

Figure 31. RGMII PHY Reference Schematic

The circuit consists of:

- An Ethernet PHY to convert the RGMII signals to differential Ethernet signals

- An AND gate to manage Ethernet reset and allow for the user to reset the PHY
- Strapping resistors to manage the PHY settings
- An RJ45 jack for connection to external networks

7.3 I^2C

The Inter-Integrated Circuit (I^2C) interface is a two-wire, bidirectional serial bus that provides a simple and efficient method for data exchange among devices. The phyCORE-AM62Ax DSC SOM provides six independent multimaster fast-mode I^2C modules. The I^2C interfaces provide the following functionality:

- Compliance with the Philips I^2C specification version 2.1.
- Support standard mode (up to 100Kb/s), fast mode (up to 400Kb/s), and high-speed mode (up to 3.4Mb/s).

Aside from I2C0, which has pullups on the SOM, all the I^2C signals require pullups in your custom CB design.

NOTE:
MCU_I2C0 and WKUP_I2C0 are open drain fail safe (I2C OD FS) buffer signals and have no internal functionality in the processor to pull the signal to a high voltage. While we recommend that all I2C signals in your design have an external pullup, if MCU_I2C0 and WKUP_I2C0 are muxed to a different functionality in your design, pullups will still be required on those signals.

CAUTION:
I2C0 is used by the on-board PMIC (I^2C address 0x30), EEPROM (I^2C address 0x50), and RTC (I^2C address 0x52). Ensure any external use of the I2C0 line does not interfere with this communication.

7.3.1 I²C Pinout

Table 25 I²C Connections at the SOC footprint

Processor Signal	X1 Pin #(s)	SOM Signal	Type	Level	Description
MCU_I2C0_SCL	119	X_MCU_I2C0_SCL	OD-O	3.3V[1]	MCU I2C0 Clock
MCU_I2C0_SDA	120	X_MCU_I2C0_SDA	OD-I/O	3.3V[1]	MCU I2C0 Data
WKUP_I2C0_SCL	125	X_WKUP_I2C0_SCL	OD-O	3.3V[1]	WKUP I2C0 Clock
WKUP_I2C0_SDA	126	X_WKUP_I2C0_SDA	OD-I/O	3.3V[1]	WKUP I2C0 Data
I2C0_SCL	144	X_I2C0_SCL (2.2K pullup on SOM)	OD-O	3.3V[1]	Main I2C0 Clock
I2C0_SDA	145	X_I2C0_SDA (2.2K pullup on SOM)	OD-I/O	3.3V[1]	Main I2C0 Data
I2C1_SCL	146	X_I2C1_SCL	OD-O	3.3V[1]	Main I2C1 Clock
I2C1_SDA	147	X_I2C1_SDA	OD-I/O	3.3V[1]	Main I2C1 Data
I2C2_SCL	1	X_GPMC0_CSn2	OD-O	3.3V[1]	Main I2C2 Clock
I2C2_SDA	175	X_GPMC0_CSn3	OD-I/O	3.3V[1]	Main I2C2 Data
I2C3_SCL	138	X_UART0_CTSN	OD-O	3.3V[1]	Main I2C3 Clock
I2C3_SDA	139	X_UART0_RTSN	OD-I/O	3.3V[1]	Main I2C3 Data

[1:] The voltage level for this signal is configurable for 1.8V or 3.3V. The default voltage level is listed here, but always check the actual jumper setting for the applicable SOM configuration. Refer to section *4.6 Solder Jumpers* for details.

7.4 SPI

The Serial Peripheral Interface (SPI) is a transmit/receive, master/slave synchronous serial bus. The phyCORE-AM62Ax DSC SOM provides access to four SPI ports at the SOC footprint.

7.4.1 SPI Pinout

Table 26 SPI Connections at the SOC footprint

Processor Signal	X1 Pin #(s)	SOM Signal(s)	Type	Level	Description
SPI0_CLK	133	X_SPI0_CLK	I/O	3.3V[1]	SPI0 Clock
SPI0_CS0	136	X_SPI0_CS0	I/O	3.3V[1]	SPI0 Chip Select 0
SPI0_CS1	137	X_SPI0_CS1	I/O	3.3V[1]	SPI0 Chip Select 1
SPI0_CS2	138	X_UART0_CTSN	I/O	3.3V[1]	SPI0 Chip Select 2
SPI0_CS3	139	X_UART0_RTSN	I/O	3.3V[1]	SPI0 Chip Select 3
SPI0_D0	134	X_SPI0_D0	O	3.3V[1]	SPI0 Data In/Out(configurable in SW) [2]
SPI0_D1	135	X_SPI0_D1	I	3.3V[1]	SPI0 Data In/Out(configurable in SW) [2]
SPI2_CLK	147	X_I2C1_SDA	I/O	3.3V[1]	SPI2 Clock
	150	X_MCASP0_ACLKR			
SPI2_CS0	148	X_MCASP0_AFSR	I/O	3.3V[1]	SPI2 Chip Select 0
SPI2_CS1	146	X_I2C1_SCL	I/O	3.3V[1]	SPI2 Chip Select 1
	151	X_MCASP0_ACLKX			
SPI2_CS2	154	X_MCASP0_AXR1	I/O	3.3V[1]	SPI2 Chip Select 2
SPI2_CS3	132	X_EXT_REFCLK1	I/O	3.3V[1]	SPI2 Chip Select 3
	149	X_MCASP0_AFSX			
SPI2_D0	152	X_MCASP0_AXR3	O	3.3V[1]	SPI2 Data In/Out(configurable in SW) [2]
	140	X_UART0_RXD			
SPI2_D1	153	X_MCASP0_AXR2	I	3.3V[1]	SPI2 Data In/Out(configurable in SW) [2]

Processor Signal	X1 Pin #(s)	SOM Signal(s)	Type	Level	Description
	141	X_UART0_TXD			
MCU_SPI0_CLK	121	X_MCU_SPI0_CLK	I/O	3.3V[1]	MCU SPI0 Clock
MCU_SPI0_CS1	124	X_MCU_SPI0_CS1	I/O	3.3V[1]	MCU SPI0 Chip Select 1
MCU_SPI0_CS2	113	X_WKUP_UART0_RXD	I/O	3.3V[1]	MCU SPI0 Chip Select 2
	117	X_MCU_MCAN1_RX			
MCU_SPI0_CS3	116	X_MCU_MCAN0_TX	I/O	3.3V[1]	MCU SPI0 Chip Select 3
MCU_SPI0_D0	122	X_MCU_SPI0_D0	O	3.3V[1]	MCU SPI0 Data In/Out(configurable in SW) [2]
MCU_SPI0_D1	123	X_MCU_SPI0_D1	I	3.3V[1]	MCU SPI0 Data In/Out(configurable in SW) [2]
MCU_SPI1_CLK	111	X_WKUP_UART0_RTSN	I/O	3.3V[1]	MCU SPI1 Clock
	117	X_MCU_MCAN1_RX			
MCU_SPI1_CS0	112	X_WKUP_UART0_CTSN	I/O	3.3V[1]	MCU SPI1 Chip Select 0
MCU_SPI1_CS1	118	X_MCU_MCAN1_TX	I/O	3.3V[1]	MCU SPI1 Chip Select 1
MCU_SPI1_CS2	114	X_WKUP_UART0_TXD	I/O	3.3V[1]	MCU SPI1 Chip Select 2
	117	X_MCU_MCAN1_RX			
MCU_SPI1_CS3	115	X_MCU_MCAN0_RX	I/O	3.3V[1]	MCU SPI1 Chip Select 3
MCU_SPI1_D0	127	X_MCU_UART0_CTSN	O	3.3V[1]	MCU SPI1 Data In/Out(configurable in SW) [2]
MCU_SPI1_D1	128	X_MCU_UART0_RTSN	I	3.3V[1]	MCU SPI1 Data In/Out(configurable in SW) [2]

[1]: The voltage level for this signal is configurable for 1.8V or 3.3V. The default voltage level is listed here, but always check the actual jumper setting for the applicable SOM configuration. Refer to section *4.6 Solder Jumpers* for details.
[2]: In our SPI DTB node we define ti,pindir-d0-out-d1-in = <1>; to set D0 as data out and D1 as Data In

7.5 UART

The Universal Asynchronous Receiver/Transmitter module is a slave peripheral that utilizes direct memory access (DMA) for data transfer or interrupt polling via a host CPU. There are ten UART modules provided, and each can be used for configuration and data exchange with external peripheral devices. UART0 is the default console and as such PHYTEC recommends bringing out UART0 for console access. More information on using it as a debug console is provided in section *11.3 UART0*.

7.5.1 UART Pinout

Table 27 UART Connections at the SOC footprint

Processor Signal	X1 Pin #(s)	SOM Signal(s)	Type	Level	Description
UART0_CTSN	138	X_UART0_CTSN	I	3.3V[1]	UART0 Clear to Send
UART0_RTSN	139	X_UART0_RTSN	O	3.3V[1]	UART0 Request to Send
UART0_RXD	140	X_UART0_RXD	I	3.3V[1]	UART0 Receive Data
UART0_TXD	141	X_UART0_TXD	O	3.3V[1]	UART0 Transmit Data
UART1_CTSN	152	X_MCASP0_AXR3	I	3.3V[1]	UART1 Clear to Send
UART1_DTRN	143	X_MCAN0_TX	O	3.3V[1]	UART1 Data Terminal Ready (active low)
UART1_RIN	142	X_MCAN0_RX	I	3.3V[1]	UART1 Ring Indicator
UART1_RTSN	153	X_MCASP0_AXR2	O	3.3V[1]	UART1 Request to Send
UART1_RXD	146	X_I2C1_SCL	I	3.3V[1]	UART1 Receive Data
	148	X_MCASP0_AFSR			

Processor Signal	X1 Pin #(s)	SOM Signal(s)	Type	Level	Description
UART1_TXD	147	X_I2C1_SDA	O	3.3V[1]	UART1 Transmit Data
	150	X_MCASP0_ACLKR			
UART2_CTSN	159	X_MMC1_DAT0	I	3.3V[1]	UART2 Clear to Send
	27	X_VOUT0_PCLK			
	18	X_GPMC0_AD14/BOOTMODE_14[2] (100K pulldown on SOM)			
UART2_RTSN	29	X_VOUT0_VSYNC	O	3.3V[1]	UART2 Request to Send
	160	X_MMC1_DAT1			
	19	X_GPMC0_AD15/BOOTMODE_15[2] (100K pulldown on SOM)			
UART2_RXD	138	X_UART0_CTSN	I	3.3V[1]	UART2 Receive Data
	162	X_MMC1_DAT3			
	12	X_GPMC0_AD8/BOOTMODE_8[2] (100K pullup on SOM)			
	46	X_VOUT0_DATA0			
UART2_TXD	139	X_UART0_RTSN	O	3.3V[1]	UART2 Transmit Data
	161	X_MMC1_DAT2			
	13	X_GPMC0_AD9/BOOTMODE_9[2] (100K pullup on SOM)			
	45	X_VOUT0_DATA1			
UART3_CTSN	156	X_MMC1_SDWP (10K pullup on SOM)	I	3.3V[1]	UART3 Clear to Send
	28	X_VOUT0_DE			
UART3_RTSN	30	X_VOUT0_HSYNC	O	3.3V[1]	UART3 Request to Send
	157	X_MMC1_SDCD (10K pullup on SOM)			
UART3_RXD	158	X_MMC1_CLK (49.9K pulldown on SOM)	I	3.3V[1]	UART3 Receive Data
	14	X_GPMC0_AD10/BOOTMODE_10[2] (100K pullup on SOM)			
	44	X_VOUT0_DATA2			
UART3_TXD	163	X_MMC1_CMD	O	3.3V[1]	UART3 Transmit Data
	15	X_GPMC0_AD11/BOOTMODE_11[2] (100K pulldown on SOM)			
	43	X_VOUT0_DATA3			
UART4_CTSN	31	X_VOUT0_DATA15	I	3.3V[1]	UART4 Clear to Send
UART4_RTSN	32	X_VOUT0_DATA14	O	3.3V[1]	UART4 Request to Send
UART4_RXD	165	X_MMC2_SDCD (10K pullup on SOM)	I	3.3V[1]	UART4 Receive Data
	1	X_GPMC0_CSn2			
	16	X_GPMC0_AD12/BOOTMODE_12[2] (100K pullup on SOM)			
	42	X_VOUT0_DATA4			
UART4_TXD	164	X_MMC2_SDWP (10K pullup on SOM)	O	3.3V[1]	UART4 Transmit Data
	175	X_GPMC0_CSn3			
	17	X_GPMC0_AD13/BOOTMODE_13[2] (100K pullup on SOM)			
	41	X_VOUT0_DATA5			
UART5_CTSN	33	X_VOUT0_DATA13	I	3.3V[1]	UART5 Clear to Send
UART5_RTSN	34	X_VOUT0_DATA12	O	3.3V[1]	UART5 Request to Send
UART5_RXD	143	X_MCAN0_TX	I	3.3V[1]	UART5 Receive Data
	170	X_MMC2_DAT3			

Processor Signal	X1 Pin #(s)	SOM Signal(s)	Type	Level	Description
	18	X_GPMC0_AD14/BOOTMODE_14[2] (100K pulldown on SOM)			
	40	X_VOUT0_DATA6			
UART5_TXD	39	X_VOUT0_DATA7	O	3.3V[1]	UART5 Transmit Data
	142	X_MCAN0_RX			
	169	X_MMC2_DAT2			
	19	X_GPMC0_AD15/BOOTMODE_15[2] (100K pulldown on SOM)			
UART6_CTSN	35	X_VOUT0_DATA11	I	3.3V[1]	UART6 Clear to Send
UART6_RTSN	36	X_VOUT0_DATA10	O	3.3V[1]	UART6 Request to Send
UART6_RXD	152	X_MCASP0_AXR3	I	3.3V[1]	UART6 Receive Data
	157	X_MMC1_SDCD (10K pullup on SOM)			
	166	X_MMC2_CLK (49.9K pulldown on SOM)			
	38	X_VOUT0_DATA8			
	176	X_GPMC0_WAIT1			
UART6_TXD	153	X_MCASP0_AXR2	O	3.3V[1]	UART6 Transmit Data
	156	X_MMC1_SDWP (10K pullup on SOM)			
	171	X_MMC2_CMD			
	177	X_GPMC0_WPn			
	37	X_VOUT0_DATA9			
MCU_UART0_CTSN	127	X_MCU_UART0_CTSN	I	3.3V[1]	MCU_UART0 Clear to Send
MCU_UART0_RTSN	128	X_MCU_UART0_RTSN	O	3.3V[1]	MCU_UART0 Request to Send
MCU_UART0_RXD	129	X_MCU_UART0_RXD	I	3.3V[1]	MCU_UART0 Receive Data
MCU_UART0_TXD	130	X_MCU_UART0_TXD	O	3.3V[1]	MCU_UART0 Transmit Data
WKUP_UART0_CTSN	112	X_WKUP_UART0_CTSN	I	3.3V[1]	WKUP_UART0 Clear to Send
WKUP_UART0_RTSN	111	X_WKUP_UART0_RTSN	O	3.3V[1]	WKUP_UART0 Request to Send
WKUP_UART0_RXD	113	X_WKUP_UART0_RXD	I	3.3V[1]	WKUP_UART0 Receive Data
WKUP_UART0_TXD	114	X_WKUP_UART0_TXD	O	3.3V[1]	WKUP_UART0 Transmit Data

[1:] The voltage level for this signal is configurable for 1.8V or 3.3V. The default voltage level is listed here, but always check the actual jumper setting for the applicable SOM configuration. Refer to section *4.6 Solder Jumpers* for details.
[2:] This signal should not be driven during reset. More information can be found in section *6.3 System Boot Configuration*

7.6 USB

The phyCORE-AM62Ax DSC SOM provides two USB2.0 Dual-Role Device (DRD) Subsystems with integrated USB VBUS detection.

7.6.1 USB Pinout

Table 28 USB Connections at the SOC footprint

X1 Pin #(s)	SOM Signal(s)	Type	Level	Description
76	X_USB0_VBUS	A/I	5V	USB Level-shifted VBUS Input (resistor/diode network on SOM)
73	X_USB0_DRVVBUS	O	3.3V[1]	USB VBUS control output (active high)
74	X_USB0_DM	USB_I/O	Differential	USB OTG1 2.0 Differential Data Negative
75	X_USB0_DP	USB_I/O	Differential	USB OTG1 2.0 Differential Data Positive
80	X_USB1_VBUS	A/I	5V	USB Level-shifted VBUS Input (resistor/diode network on SOM)
77	X_USB1_DRVVBUS	O	3.3V[1]	USB VBUS control output (active high)
78	X_USB1_DM	USB_I/O	Differential	USB OTG1 2.0 Differential Data Negative
79	X_USB1_DP	USB_I/O	Differential	USB OTG1 2.0 Differential Data Positive

[1]: The voltage level for this signal is configurable for 1.8V or 3.3V. The default voltage level is listed here, but always check the actual jumper setting for the applicable SOM configuration. Refer to section *4.6 Solder Jumpers* for details.

7.6.2 USB Design In Considerations

- X_USB#_DP/X_USB#_DM trace lengths should be matched and should be no more than 12 inches in total length (SOM + Carrier Board), though 4 inches is considered typical. The table below shows the length of the USB2.0 traces on the SOM and required constraints.

Table 29 phyCORE-AM62Ax DSC USB0 Layout Characteristics

Signal Name	Length (µm)			Length Matching (µm)	Single Ended Impedance (Ω)	Differential Impedance (Ω)
	SOM Trace	Max Total	Max CB Trace			
X_USB0_DP	17796	304800	287004	1270	50	90
X_USB0_DM	18006	304800	286794		50	
X_USB1_DP	20877	304800	283923	1270	50	90
X_USB1_DM	20882	304800	283918		50	

7.6.3 USB Reference Circuits

Example reference circuits for connecting the USB1 signals to a HUB and then connecting the HUB to a USB 2.0 connector as well as connecting USB0 to a USB-C connector are shown below.

Figure 32. USB-HUB Reference Schematic

Figure 33. USB 2.0 Connector Reference Schematic

The above circuits consist of the following parts:

- A USB-HUB to convert the USB2.0 and SERDES signals into four USB outputs
- Two USB power switches to shut down the USB power rails if the current exceeds 0.6A
- Two TVS diode arrays and two common mode filters (CMF) for ESD and EMI considerations
- A two port USB 2.0 connector

Figure 34. USB-C Connector Reference Schematic

The above circuits consist of the following parts:

- A USB-C PD controller to manage the USB-C control signals
- A serial NOR memory and 2x5 header to program the USB-C controller
- Two TVS diode arrays for ESD and EMI considerations
- A USB-C connector

7.7 MCASP

The phyCORE-AM62Ax DSC SOM provides three Multichannel Audio Serial Ports (MCASP). The MCASP interfaces provide the following functionality:

- Supports Time Division Multiplexing (TDM), Inter-IC Sound (I2S), and similar formats
- Supports digital audio interface transmission formats (SPDIF, IEC60958-1, and AES-3)

7.7.1 MCASP Pinout

Table 30 MCASP Connections at the SOC footprint

Processor Signal	X1 Pin #(s)	SOM Signal(s)	Type	Level	Description
MCASP0_ACLKR	150	X_MCASP0_ACLKR	I/O	3.3V[1]	MCASP Receive Bit Clock
MCASP0_ACLKX	151	X_MCASP0_ACLKX	I/O	3.3V[1]	MCASP Transmit Bit Clock
MCASP0_AFSR	148	X_MCASP0_AFSR	I/O	3.3V[1]	MCASP Receive Frame Sync
MCASP0_AFSX	149	X_MCASP0_AFSX	I/O	3.3V[1]	MCASP Transmit Frame Sync
MCASP0_AXR0	155	X_MCASP0_AXR0	I/O	3.3V[1]	MCASP Serial Data (Input/Output)

MCASP0_AXR1	154	X_MCASP0_AXR1	I/O	3.3V[1]	MCASP Serial Data (Input/Output)
MCASP0_AXR2	153	X_MCASP0_AXR2	I/O	3.3V[1]	MCASP Serial Data (Input/Output)
MCASP0_AXR3	152	X_MCASP0_AXR3	I/O	3.3V[1]	MCASP Serial Data (Input/Output)
MCASP1_ACLKR	166	X_MMC2_CLK (49.9K pulldown on SOM)	I/O	3.3V[1]	MCASP Receive Bit Clock
	175	X_GPMC0_CSn3			
MCASP1_ACLKX	165	X_MMC2_SDCD (10K pullup on SOM)	I/O	3.3V[1]	MCASP Transmit Bit Clock
	173	X_GPMC0_BE0n_CLE			
MCASP1_AFSR	171	X_MMC2_CMD	I/O	3.3V[1]	MCASP Receive Frame Sync
	1	X_GPMC0_CSn2			
MCASP1_AFSX	164	X_MMC2_SDWP (10K pullup on SOM)	I/O	3.3V[1]	MCASP Transmit Frame Sync
	20	X_GPMC0_WAIT0			
MCASP1_AXR0	167	X_MMC2_DAT0	I/O	3.3V[1]	MCASP Serial Data (Input/Output)
	179	X_GPMC0_WEn			
MCASP1_AXR1	168	X_MMC2_DAT1	I/O	3.3V[1]	MCASP Serial Data (Input/Output)
	178	X_GPMC0_OEn_REn			
MCASP1_AXR2	169	X_MMC2_DAT2	I/O	3.3V[1]	MCASP Serial Data (Input/Output)
	174	X_GPMC0_ADVn_ALE			
MCASP1_AXR3	170	X_MMC2_DAT3	I/O	3.3V[1]	MCASP Serial Data (Input/Output)
	22	X_GPMC0_CLK			
MCASP1_AXR4	1	X_GPMC0_CSn2	I/O	3.3V[1]	MCASP Serial Data (Input/Output)
	171	X_MMC2_CMD			
MCASP1_AXR5	166	X_MMC2_CLK (49.9K pulldown on SOM)	I/O	3.3V[1]	MCASP Serial Data (Input/Output)
	175	X_GPMC0_CSn3			
MCASP2_ACLKR	58	X_CPSW_RGMII2_TD1	I/O	3.3V[1]	MCASP Receive Bit Clock
	19	X_GPMC0_AD15/BOOTMODE_15[2] (100K pulldown on SOM)			
MCASP2_ACLKX	60	X_CPSW_RGMII2_TD3	I/O	3.3V[1]	MCASP Transmit Bit Clock
	139	X_UART0_RTSN			
	17	X_GPMC0_AD13/BOOTMODE_13[2] (100K pullup on SOM)			
MCASP2_AFSR	53	X_CPSW_RGMII2_RD1	I/O	3.3V[1]	MCASP Receive Frame Sync
	18	X_GPMC0_AD14/BOOTMODE_14[2] (100K pulldown on SOM)			
MCASP2_AFSX	138	X_UART0_CTSN	I/O	3.3V[1]	MCASP Transmit Frame Sync
	59	X_CPSW_RGMII2_TD2			
	16	X_GPMC0_AD12/BOOTMODE_12[2] (100K pullup on SOM)			
MCASP2_AXR0	52	X_CPSW_RGMII2_RD2	I/O	3.3V[1]	MCASP Serial Data (Input/Output)
	143	X_MCAN0_TX			
	12	X_GPMC0_AD8/BOOTMODE_8[2] (100K pullup on SOM)			
MCASP2_AXR1	50	X_CPSW_RGMII2_RXC	I/O	3.3V[1]	MCASP Serial Data (Input/Output)
	142	X_MCAN0_RX			
	13	X_GPMC0_AD9/BOOTMODE_9[2] (100K pullup on SOM)			
MCASP2_AXR2	54	X_CPSW_RGMII2_RD0	I/O	3.3V[1]	MCASP Serial Data (Input/Output)

	14	X_GPMC0_AD10/BOOTMODE_10[2] (100K pullup on SOM)			
MCASP2_AXR3	49	X_CPSW_RGMII2_RX_CTL	I/O	3.3V[1]	MCASP Serial Data (Input/Output)
	15	X_GPMC0_AD11/BOOTMODE_11[2] (100K pulldown on SOM)			
MCASP2_AXR4	55	X_CPSW_RGMII2_TX_CTL	I/O	3.3V[1]	MCASP Serial Data (Input/Output)
	4	X_GPMC0_AD0/BOOTMODE_0[2] (100K pullup on SOM)			
MCASP2_AXR5	56	X_CPSW_RGMII2_TXC	I/O	3.3V[1]	MCASP Serial Data (Input/Output)
	5	X_GPMC0_AD1/BOOTMODE_1[2] (100K pullup on SOM)			
MCASP2_AXR6	6	X_GPMC0_AD2/BOOTMODE_2[2] (100K pulldown on SOM)	I/O	3.3V[1]	MCASP Serial Data (Input/Output)
	57	X_CPSW_RGMII2_TD0			
MCASP2_AXR7	53	X_CPSW_RGMII2_RD1	I/O	3.3V[1]	MCASP Serial Data (Input/Output)
	7	X_GPMC0_AD3/BOOTMODE_3[2] (100K pullup on SOM)			
MCASP2_AXR8	8	X_GPMC0_AD4/BOOTMODE_4[2] (100K pulldown on SOM)	I/O	3.3V[1]	MCASP Serial Data (Input/Output)
	58	X_CPSW_RGMII2_TD1			
MCASP2_AXR9	9	X_GPMC0_AD5/BOOTMODE_5[2] (100K pulldown on SOM)	I/O	3.3V[1]	MCASP Serial Data (Input/Output)
MCASP2_AXR10	10	X_GPMC0_AD6/BOOTMODE_6[2] (100K pullup on SOM)	I/O	3.3V[1]	MCASP Serial Data (Input/Output)
MCASP2_AXR11	11	X_GPMC0_AD7/BOOTMODE_7[2] (100K pulldown on SOM)	I/O	3.3V[1]	MCASP Serial Data (Input/Output)
MCASP2_AXR12	172	X_GPMC0_BE1n	I/O	3.3V[1]	MCASP Serial Data (Input/Output)
MCASP2_AXR13	21	X_GPMC0_DIR	I/O	3.3V[1]	MCASP Serial Data (Input/Output)
MCASP2_AXR14	3	X_GPMC0_CSn0	I/O	3.3V[1]	MCASP Serial Data (Input/Output)
MCASP2_AXR15	2	X_GPMC0_CSn1	I/O	3.3V[1]	MCASP Serial Data (Input/Output)

[1:] The voltage level for this signal is configurable for 1.8V or 3.3V. The default voltage level is listed here, but always check the actual jumper setting for the applicable SOM configuration. Refer to section *4.6 Solder Jumpers* for details.
[2:] This signal should not be driven during reset. More information can be found in section *6.3 System Boot Configuration.*

8 Display and Camera Interfaces

The following sub-sections detail each of the display/camera interfaces supported on the phyCORE-AM62Ax DSC.

8.1 VOUT

The phyCORE-AM62Ax DSC SOM brings out one 24-bit RGB parallel video output (VOUT). VOUT supports the following display interface modes:

- Parallel MIPI DPI 2.0 (Digital Pixel Interface): RGB 16/18/24-bit outputs with separate sync signals
- BT.656/BT.1120 interface: YUV422 outputs (8/10-bit modes) with embedded syncs

8.1.1 VOUT Pinout

Table 31 VOUT Connections at the SOC footprint

Processor Signal	X1 Pin #(s)	SOM Signal(s)	Type	Level	Description
VOUT_DE	28	VOUT_DE	O	3.3V[1]	Video Output Data Enable
VOUT0_EXTPCLKIN	176	X_GPMC0_WAIT1	I	3.3V[1]	Video Output External Pixel Clock Input
VOUT0_HSYNC	30	X_VOUT0_HSYNC	O	3.3V[1]	Video Output Horizontal Sync
VOUT0_PCLK	27	X_VOUT0_PCLK	O	3.3V[1]	Video Output Pixel Clock Output
VOUT0_VSYNC	29	X_VOUT0_SYNC	O	3.3V[1]	Video Output Vertical Sync
VOUT0_DATA0	46	X_VOUT0_DATA0	O	3.3V[1]	Video Output Data 0
VOUT0_DATA1	45	X_VOUT0_DATA1	O	3.3V[1]	Video Output Data 1
VOUT0_DATA2	44	X_VOUT0_DATA2	O	3.3V[1]	Video Output Data 2
VOUT0_DATA3	43	X_VOUT0_DATA3	O	3.3V[1]	Video Output Data 3
VOUT0_DATA4	42	X_VOUT0_DATA4	O	3.3V[1]	Video Output Data 4
VOUT0_DATA5	41	X_VOUT0_DATA5	O	3.3V[1]	Video Output Data 5
VOUT0_DATA6	40	X_VOUT0_DATA6	O	3.3V[1]	Video Output Data 6
VOUT0_DATA7	39	X_VOUT0_DATA7	O	3.3V[1]	Video Output Data 7
VOUT0_DATA8	38	X_VOUT0_DATA8	O	3.3V[1]	Video Output Data 8
VOUT0_DATA9	37	X_VOUT0_DATA9	O	3.3V[1]	Video Output Data 9
VOUT0_DATA10	36	X_VOUT0_DATA10	O	3.3V[1]	Video Output Data 10
VOUT0_DATA11	35	X_VOUT0_DATA11	O	3.3V[1]	Video Output Data 11
VOUT0_DATA12	34	X_VOUT0_DATA12	O	3.3V[1]	Video Output Data 12
VOUT0_DATA13	33	X_VOUT0_DATA13	O	3.3V[1]	Video Output Data 13
VOUT0_DATA14	32	X_VOUT0_DATA14	O	3.3V[1]	Video Output Data 14
VOUT0_DATA15	31	X_VOUT0_DATA15	O	3.3V[1]	Video Output Data 15
VOUT0_DATA16	12	X_GPMC0_AD8/BOOTMODE_8[2] (100K pullup on SOM)	O	3.3V[1]	Video Output Data 16
VOUT0_DATA17	13	X_GPMC0_AD9/BOOTMODE_9[2] (100K pullup on SOM)	O	3.3V[1]	Video Output Data 17
VOUT0_DATA18	14	X_GPMC0_AD10/BOOTMODE_10[2] (100K pullup on SOM)	O	3.3V[1]	Video Output Data 18
VOUT0_DATA19	15	X_GPMC0_AD11/BOOTMODE_11[2] (100K pulldown on SOM)	O	3.3V[1]	Video Output Data 19
VOUT0_DATA20	16	X_GPMC0_AD12/BOOTMODE_12[2] (100K pullup on SOM)	O	3.3V[1]	Video Output Data 20
VOUT0_DATA21	17	X_GPMC0_AD13/BOOTMODE_13[2] (100K pullup on SOM)	O	3.3V[1]	Video Output Data 21
VOUT0_DATA22	18	X_GPMC0_AD14/BOOTMODE_14[2] (100K pulldown on SOM)	O	3.3V[1]	Video Output Data 22
VOUT0_DATA23	19	X_GPMC0_AD15/BOOTMODE_15[2] (100K pulldown on SOM)	O	3.3V[1]	Video Output Data 23

[1:] The voltage level for this signal is configurable for 1.8V or 3.3V. The default voltage level is listed here, but always check the actual jumper setting for the applicable SOM configuration. Refer to section *4.6 Solder Jumpers* for details.
[2:] This signal should not be driven during reset. More information can be found in section *6.3 System Boot Configuration.*

8.2 CSI

The phyCORE-AM62Ax DSC SOM brings out one 4 lane CSI (camera serial interface). The CSI interfaces provide the following functionality:

- Compliant with MIPI CSI 1.3 and MIPI-DPHY 1.2
- Support for 1,2,3 or 4 data lane mode up to 2.5Gbps
- Supports up to 16 virtual channels per input

8.2.1 CSI Pinout

Table 32 CSI Connections at the SOC footprint

Processor Signal	X1 Pin #(s)	SOM Signal(s)	Type	Level	Description
CSI0_RXCLKN	82	X_CSI0_RXCLKN	CSI_I	Differential	CSI Differential Receive Clock Input (negative)
CSI0_RXCLKP	81	X_CSI0_RXCLKP	CSI_I	Differential	CSI Differential Receive Clock Input (positive)
CSI0_RXN0	90	X_CSI0_RXN0	CSI_I	Differential	CSI Differential Receive Input (negative)
CSI0_RXP0	89	X_CSI0_RXP0	CSI_I	Differential	CSI Differential Receive Input (positive)
CSI0_RXN1	84	X_CSI0_RXN1	CSI_I	Differential	CSI Differential Receive Input (negative)
CSI0_RXP1	83	X_CSI0_RXP1	CSI_I	Differential	CSI Differential Receive Input (positive)
CSI0_RXN2	86	X_CSI0_RXN2	CSI_I	Differential	CSI Differential Receive Input (negative)
CSI0_RXP2	85	X_CSI0_RXP2	CSI_I	Differential	CSI Differential Receive Input (positive)
CSI0_RXN3	88	X_CSI0_RXN3	CSI_I	Differential	CSI Differential Receive Input (negative)
CSI0_RXP3	87	X_CSI0_RXP3	CSI_I	Differential	CSI Differential Receive Input (positive)

8.2.2 CSI Design In Considerations

- CSI supports up to 4x data lanes and 1x clock lane.
- More general differential pair routing guidelines are in section *4.10.1 High-Speed Differential Signal Routing Guidelines.*

Table 33 phyCORE-AM62Ax DSC CSI0 Layout Characteristics

Signal Name	SOM Trace Length (µm)	Match Group	Recommended Intrapair Length Match	Recommended Interpair Length Match
CSI0_RXCLKN	27445	CSI	254 µm	1270 µm
CSI0_RXCLKP	27440			
CSI0_RXN0	27580			
CSI0_RXP0	27785			
CSI0_RXN1	27561			
CSI0_RXP1	27614			
CSI0_RXN2	27591			
CSI0_RXP2	27385			
CSI0_RXN3	27806			
CSI0_RXP3	27779			

8.2.3 CSI Reference Circuits

Example reference circuits for connecting the CSI signals to a 30-pin connector are shown below. The 30-pin connector pinout is designed to connect to a PHYTEC camera and supports both 3.3V and 5V cameras.

Figure 35. CSI Power Toggle Reference Schematic

Figure 36. CSI Connector Reference Schematic

The above circuits consist of the following parts:

- A power circuit to swap between 5V and 3.3V voltage power
- A 30-pin FFC connector

9 Control Interfaces

The following sub-sections detail each of the control interfaces supported on the phyCORE-AM62Ax DSC.

9.1 Enhanced Capture

The phyCORE-AM62Ax DSC SOM brings out 3x Enhanced Capture (ECAP) modules.

9.1.1 ECAP Pinout

Table 34 ECAP Connections at the SOC footprint

Processor Signal	X1 Pin #(s)	SOM Signal(s)	Type	Level	Description
ECAP0_IN_APWM_OUT	132	X_EXT_REFCLK1	I/O	3.3V[1]	Enhanced Capture (ECAP) Input or Auxiliary PWM (APWM) Output
	137	X_SPI0_CS1			
ECAP1_IN_APWM_OUT	154	X_MCASP0_AXR1	I/O	3.3V[1]	Enhanced Capture (ECAP) Input or Auxiliary PWM (APWM) Output
	152	X_MCASP0_AXR3			
	160	X_MMC1_DAT1			
	140	X_UART0_RXD			
ECAP2_IN_APWM_OUT	153	X_MCASP0_AXR2	I/O	3.3V[1]	Enhanced Capture (ECAP) Input or Auxiliary PWM (APWM) Output
	159	X_MMC1_DAT0			
	151	X_MCASP0_ACLKX			
	141	X_UART0_TXD			

[1:] The voltage level for this signal is configurable for 1.8V or 3.3V. The default voltage level is listed here, but always check the actual jumper setting for the applicable SOM configuration. Refer to section *4.6 Solder Jumpers* for details.

9.2 Enhanced Pulse-Width Modulation

The phyCORE-AM62Ax DSC SOM supports up to four Enhanced Pulse-Width Modulation (PWM) modules. Each PWM provides the following functionality:

- A dedicated 16-bit time-base counter with period and frequency control.
- Two PWM outputs that can be used as either:
  - Two independent PWM outputs with single-edge operation
  - Two independent PWM outputs with dual-edge symmetric operation
  - One independent PWM output with dual-edge asymmetric operation

9.2.1 EPWM Pinout

Table 35 EPWM Connections at the SOC footprint

Processor Signal	X1 Pin #(s)	SOM Signal(s)	Type	Level	Description
EHRPWM_TZn_IN0	135	X_SPI0_D1	I	3.3V[1]	EHRPWM Trip Zone Input 2 (active low)
EHRPWM_TZn_IN3	143	X_MCAN0_TX	I	3.3V[1]	EHRPWM Trip Zone Input 2 (active low)
EHRPWM_TZn_IN4	142	X_MCAN0_RX	I	3.3V[1]	EHRPWM Trip Zone Input 2 (active low)
EHRPWM_TZn_IN5	137	X_SPI0_CS1	I	3.3V[1]	EHRPWM Trip Zone Input 2 (active low)
EHRPWM0_A	136	X_SPI0_CS0	I/O	3.3V[1]	EHRPWM Output A
	148	X_MCASP0_AFSR			
EHRPWM0_B	150	X_MCASP0_ACLKR	I/O	3.3V[1]	EHRPWM Output B
	137	X_SPI0_CS1			
EHRPWM0_SYNCI	146	X_I2C1_SCL	I	3.3V[1]	Sync Input to EHRPWM module from an external pin
EHRPWM0_SYNCO	147	X_I2C1_SDA	O	3.3V[1]	Sync Output to EHRPWM module to an external pin

Processor Signal	X1 Pin #(s)	SOM Signal(s)	Type	Level	Description
EHRPWM1_A	133	X_SPI0_CLK	I/O	3.3V[1]	EHRPWM Output A
	154	X_MCASP0_AXR1			
EHRPWM1_B	134	X_SPI0_D0	I/O	3.3V[1]	EHRPWM Output B
	155	X_MCASP0_AXR0			
EHRPWM2_A	146	X_I2C1_SCL	I/O	3.3V[1]	EHRPWM Output A
	140	X_UART0_RXD			
EHRPWM2_B	147	X_I2C1_SDA	I/O	3.3V[1]	EHRPWM Output B
	141	X_UART0_TXD			

[1]: The voltage level for this signal is configurable for 1.8V or 3.3V. The default voltage level is listed here, but always check the actual jumper setting for the applicable SOM configuration. Refer to section *4.6 Solder Jumpers* for details.

9.3 Enhanced Quadrature Encoder Pulse

The phyCORE-AM62Ax DSC SOM brings out 3x Enhanced Quadrature Encoder Pulse (EQEP) modules.

9.3.1 EQEP Pinout

Table 36 EQEP Connections at the SOC footprint

Processor Signal	X1 Pin #(s)	SOM Signal(s)	Type	Level	Description
EQEP0_A	152	X_MCASP0_AXR3	I	3.3V[1]	EQEP Quadrature Input A
EQEP0_B	153	X_MCASP0_AXR2	I	3.3V[1]	EQEP Quadrature Input B
EQEP0_I	155	X_MCASP0_AXR0	I/O	3.3V[1]	EQEP Index
EQEP0_S	154	X_MCASP0_AXR1	I/O	3.3V[1]	EQEP Strobe
EQEP1_A	151	X_MCASP0_ACLKX	I	3.3V[1]	EQEP Quadrature Input A
EQEP1_B	149	X_MCASP0_AFSX	I	3.3V[1]	EQEP Quadrature Input B
EQEP1_I	150	X_MCASP0_ACLKR	I/O	3.3V[1]	EQEP Index
EQEP1_S	148	X_MCASP0_AFSR	I/O	3.3V[1]	EQEP Strobe
EQEP2_A	52	X_CPSW_RGMII2_RD2	I	3.3V[1]	EQEP Quadrature Input A
EQEP2_B	51	X_CPSW_RGMII2_RD3	I	3.3V[1]	EQEP Quadrature Input B
EQEP2_I	59	X_CPSW_RGMII2_TD2	I/O	3.3V[1]	EQEP Index
	143	X_MCAN0_TX			
	176	X_GPMC0_WAIT1			
EQEP2_S	60	X_CPSW_RGMII2_TD3	I/O	3.3V[1]	EQEP Strobe
	142	X_MCAN0_RX			
	21	X_GPMC0_DIR			

[1]: The voltage level for this signal is configurable for 1.8V or 3.3V. The default voltage level is listed here, but always check the actual jumper setting for the applicable SOM configuration. Refer to section *4.6 Solder Jumpers* for details.

10 Peripheral Interfaces

The following sub-sections detail each of the peripheral interfaces supported on the phyCORE-AM62Ax DSC.

10.1 CPTS

The phyCORE-AM62Ax DSC SOM brings out the Common Platform Time Sync (CPTS) module that is used to facilitate host control of time sync operations.

10.1.1 CPTS Pinout

Table 37 CPTS Connections at the SOC footprint

Processor Signal	X1 Pin #(s)	SOM Signal(s)	Type	Level	Description
CP_GEMAC_CPTS0_RFT_CLK	132	X_EXT_REFCLK1	I	3.3V[1]	CPTS Reference Clock
CP_GEMAC_CPTS0_TS_COMP	137	X_SPI0_CS1	O	3.3V[1]	CPTS Time Stamp Counter Compare
	162	X_MMC1_DAT3			
CP_GEMAC_CPTS0_TS_SYNC	133	X_SPI0_CLK	O	3.3V[1]	CPTS Time Stamp Counter Bit
	161	X_MMC1_DAT2			
CP_GEMAC_CPTS0_HW1TSPUSH	134	X_SPI0_D0	I	3.3V[1]	CPTS Hardware Time Stamp Push 1
	160	X_MMC1_DAT1			
CP_GEMAC_CPTS0_HW2TSPUSH	159	X_MMC1_DAT0	I	3.3V[1]	CPTS Hardware Time Stamp Push 2
	135	X_SPI0_D1			
SYNC1_OUT	132	X_EXT_REFCLK1	O	3.3V[1]	CPTS Time Stamp Generator Bit 1
SYNC2_OUT	143	X_MCAN0_TX	O	3.3V[1]	CPTS Time Stamp Generator Bit 2
SYNC3_OUT	142	X_MCAN0_RX	O	3.3V[1]	CPTS Time Stamp Generator Bit 3

[1]: The voltage level for this signal is configurable for 1.8V or 3.3V. The default voltage level is listed here, but always check the actual jumper setting for the applicable SOM configuration. Refer to section *4.6 Solder Jumpers* for details.

10.2 GPIO

The General-Purpose Input/Output interfaces provides pins that can be configured as either inputs or outputs. Many of the signals available at the SOC footprint can be multiplexed as GPIOs. The AM62Ax SOC processor supports five independent GPIO modules:

- GPIO0
- GPIO1
- MCU_GPIO0

The following table lists the number of GPIOs available from each of these GPIO modules at the SOC footprint, with a total of 127 GPIOs available depending on the multiplexing configuration. Note that not all GPIOs can be used simultaneously as there is overlap of connector pins between the GPIO modules.

Table 38 Total Available GPIO

GPIO Module	Number of GPIO Available
GPIO0	65
GPIO1	40
MCU_GPIO0	22
Total	127

Many of the GPIOs are multiplexed with other interfaces, some of which connect to on-board circuits. Review the tables below when using these GPIOs to check for pull-up and pull-down resistors, connected devices, etc.

CAUTION:
The majority of the GPIO pins can be either 1.8V or 3.3V depending on the jumper settings. Take care when using these signals and consider the voltage levels.

10.2.1 GPIO Pinout

Table 39 GPIO0 Accessibility at SOC footprint

Processor Signal	X1 Pin #(s)	SOM Signal(s)	Type	Level	Internal SOM Usage
GPIO0_15	4	X_GPMC0_AD0/BOOTMODE_0	I/O	3.3V[1]	100K pullup Do not drive during reset
GPIO0_16	5	X_GPMC0_AD1/BOOTMODE_1	I/O	3.3V[1]	100K pullup Do not drive during reset
GPIO0_17	6	X_GPMC0_AD2/BOOTMODE_2	I/O	3.3V[1]	100K pulldown Do not drive during reset
GPIO0_18	7	X_GPMC0_AD3/BOOTMODE_3	I/O	3.3V[1]	100K pullup Do not drive during reset
GPIO0_19	8	X_GPMC0_AD4/BOOTMODE_4	I/O	3.3V[1]	100K pulldown Do not drive during reset
GPIO0_20	9	X_GPMC0_AD5/BOOTMODE_5	I/O	3.3V[1]	100K pulldown Do not drive during reset
GPIO0_21	10	X_GPMC0_AD6/BOOTMODE_6	I/O	3.3V[1]	100K pullup Do not drive during reset
GPIO0_22	11	X_GPMC0_AD7/BOOTMODE_7	I/O	3.3V[1]	100K pulldown Do not drive during reset
GPIO0_23	12	X_GPMC0_AD8/BOOTMODE_8	I/O	3.3V[1]	100K pullup Do not drive during reset
GPIO0_24	13	X_GPMC0_AD9/BOOTMODE_9	I/O	3.3V[1]	100K pullup Do not drive during reset
GPIO0_25	14	X_GPMC0_AD10/BOOTMODE_10	I/O	3.3V[1]	100K pullup Do not drive during reset
GPIO0_26	15	X_GPMC0_AD11/BOOTMODE_11	I/O	3.3V[1]	100K pulldown Do not drive during reset
GPIO0_27	16	X_GPMC0_AD12/BOOTMODE_12	I/O	3.3V[1]	100K pullup Do not drive during reset
GPIO0_28	17	X_GPMC0_AD13/BOOTMODE_13	I/O	3.3V[1]	100K pullup Do not drive during reset
GPIO0_29	18	X_GPMC0_AD14/BOOTMODE_14	I/O	3.3V[1]	100K pulldown Do not drive during reset
GPIO0_30	19	X_GPMC0_AD15/BOOTMODE_15	I/O	3.3V[1]	100K pulldown Do not drive during reset
GPIO0_31	22	X_GPMC0_CLK	I/O	3.3V[1]	None
GPIO0_32	174	X_GPMC0_ADVn_ALE	I/O	3.3V[1]	None
GPIO0_33	178	X_GPMC0_OEn_REn	I/O	3.3V[1]	None
GPIO0_34	179	X_GPMC0_WEn	I/O	3.3V[1]	None
GPIO0_35	173	X_GPMC0_BE0n_CLE	I/O	3.3V[1]	None
GPIO0_36	172	X_GPMC0_BE1n	I/O	3.3V[1]	None

Processor Signal	X1 Pin #(s)	SOM Signal(s)	Type	Level	Internal SOM Usage
GPIO0_37	20	X_GPMC0_WAIT0	I/O	3.3V[1]	None
GPIO0_38	176	X_GPMC0_WAIT1	I/O	3.3V[1]	None
GPIO0_39	177	X_GPMC0_WPn	I/O	3.3V[1]	None
GPIO0_40	21	X_GPMC0_DIR	I/O	3.3V[1]	None
GPIO0_41	3	X_GPMC0_CSn0	I/O	3.3V[1]	None
GPIO0_42	2	X_GPMC0_CSn1	I/O	3.3V[1]	None
GPIO0_43	1	X_GPMC0_CSn2	I/O	3.3V[1]	None
GPIO0_44	175	X_GPMC0_CSn3	I/O	3.3V[1]	None
GPIO0_45	46	X_VOUT0_DATA0	I/O	3.3V[1]	None
GPIO0_46	45	X_VOUT0_DATA1	I/O	3.3V[1]	None
GPIO0_47	44	X_VOUT0_DATA2	I/O	3.3V[1]	None
GPIO0_48	43	X_VOUT0_DATA3	I/O	3.3V[1]	None
GPIO0_49	42	X_VOUT0_DATA4	I/O	3.3V[1]	None
GPIO0_50	41	X_VOUT0_DATA5	I/O	3.3V[1]	None
GPIO0_51	40	X_VOUT0_DATA6	I/O	3.3V[1]	None
GPIO0_52	39	X_VOUT0_DATA7	I/O	3.3V[1]	None
GPIO0_53	38	X_VOUT0_DATA8	I/O	3.3V[1]	None
GPIO0_54	37	X_VOUT0_DATA9	I/O	3.3V[1]	None
GPIO0_55	36	X_VOUT0_DATA10	I/O	3.3V[1]	None
GPIO0_56	35	X_VOUT0_DATA11	I/O	3.3V[1]	None
GPIO0_57	34	X_VOUT0_DATA12	I/O	3.3V[1]	None
GPIO0_58	33	X_VOUT0_DATA13	I/O	3.3V[1]	None
GPIO0_59	32	X_VOUT0_DATA14	I/O	3.3V[1]	None
GPIO0_60	31	X_VOUT0_DATA15	I/O	3.3V[1]	None
GPIO0_61	30	X_VOUT0_HSYNC	I/O	3.3V[1]	None
GPIO0_62	28	X_VOUT0_DE	I/O	3.3V[1]	None
GPIO0_63	29	X_VOUT0_VSYNC	I/O	3.3V[1]	None
GPIO0_64	27	X_VOUT0_PCLK	I/O	3.3V[1]	None
GPIO0_65	170	X_MMC2_DAT3	I/O	3.3V[1]	None
GPIO0_66	169	X_MMC2_DAT2	I/O	3.3V[1]	None
GPIO0_67	168	X_MMC2_DAT1	I/O	3.3V[1]	None
GPIO0_68	167	X_MMC2_DAT0	I/O	3.3V[1]	None
GPIO0_69	166	X_MMC2_CLK	I/O	3.3V[1]	49.9K pulldown
GPIO0_70	171	X_MMC2_CMD	I/O	3.3V[1]	None
GPIO0_71	165	X_MMC2_SDCD	I/O	3.3V[1]	10K pullup
GPIO0_72	164	X_MMC2_SDWP	I/O	3.3V[1]	10K pullup
GPIO0_85	48	X_MDIO0_MDIO	I/O	3.3V[1]	1.5K pullup and used by the internal SOM ETH PHY
GPIO0_86	47	X_MDIO0_MDC	I/O	3.3V[1]	1.5K pullup and used by the internal SOM ETH PHY
GPIO0_87	55	X_CPSW_RGMII2_TX_CTL	I/O	3.3V[1]	None
GPIO0_88	56	X_CPSW_RGMII2_TXC	I/O	3.3V[1]	None
GPIO0_89	57	X_CPSW_RGMII2_TD0	I/O	3.3V[1]	None
GPIO0_90	58	X_CPSW_RGMII2_TD1	I/O	3.3V[1]	None
GPIO0_91	59	X_CPSW_RGMII2_TD2	I/O	3.3V[1]	None

[1:] The voltage level for this signal is configurable for 1.8V or 3.3V. The default voltage level is listed here, but always check the actual jumper setting for the applicable SOM configuration. Refer to section *4.6 Solder Jumpers* for details.

Table 40 GPIO1 Accessibility at SOC footprint

Processor Signal	X1 Pin #(s)	SOM Signal(s)	Type	Level	Internal SOM Usage
GPIO1_0	60	X_CPSW_RGMII2_TD3	I/O	3.3V[1]	None
GPIO1_1	49	X_CPSW_RGMII2_RX_CTL	I/O	3.3V[1]	None
GPIO1_2	50	X_CPSW_RGMII2_RXC	I/O	3.3V[1]	None
GPIO1_3	54	X_CPSW_RGMII2_RD0	I/O	3.3V[1]	None
GPIO1_4	53	X_CPSW_RGMII2_RD1	I/O	3.3V[1]	None
GPIO1_5	52	X_CPSW_RGMII2_RD2	I/O	3.3V[1]	None
GPIO1_6	51	X_CPSW_RGMII2_RD3	I/O	3.3V[1]	None
GPIO1_7	152	X_MCASP0_AXR3	I/O	3.3V[1]	None
GPIO1_8	153	X_MCASP0_AXR2	I/O	3.3V[1]	None
GPIO1_9	154	X_MCASP0_AXR1	I/O	3.3V[1]	None
GPIO1_10	155	X_MCASP0_AXR0	I/O	3.3V[1]	None
GPIO1_11	151	X_MCASP0_ACLKX	I/O	3.3V[1]	None
GPIO1_12	149	X_MCASP0_AFSX	I/O	3.3V[1]	None
GPIO1_13	148	X_MCASP0_AFSR	I/O	3.3V[1]	None
GPIO1_14	150	X_MCASP0_ACLKR	I/O	3.3V[1]	None
GPIO1_15	136	X_SPI0_CS0	I/O	3.3V[1]	None
GPIO1_16	137	X_SPI0_CS1	I/O	3.3V[1]	None
GPIO1_17	133	X_SPI0_CLK	I/O	3.3V[1]	None
GPIO1_18	134	X_SPI0_D0	I/O	3.3V[1]	None
GPIO1_19	135	X_SPI0_D1	I/O	3.3V[1]	None
GPIO1_20	140	X_UART0_RXD	I/O	3.3V[1]	None
GPIO1_21	141	X_UART0_TXD	I/O	3.3V[1]	None
GPIO1_22	138	X_UART0_CTSN	I/O	3.3V[1]	None
GPIO1_23	139	X_UART0_RTSN	I/O	3.3V[1]	None
GPIO1_24	143	X_MCAN0_TX	I/O	3.3V[1]	None
GPIO1_25	142	X_MCAN0_RX	I/O	3.3V[1]	None
GPIO1_28	146	X_I2C1_SCL	I/O	3.3V[1]	None
GPIO1_29	147	X_I2C1_SDA	I/O	3.3V[1]	None
GPIO1_30	132	X_EXT_REFCLK1	I/O	3.3V[1]	None
GPIO1_31	237	X_RTC_INT	OD-I/O	3.3V[1]	10K pullup
GPIO1_42	162	X_MMC1_DAT3	I/O	3.3V[1]	None
GPIO1_43	161	X_MMC1_DAT2	I/O	3.3V[1]	None
GPIO1_44	160	X_MMC1_DAT1	I/O	3.3V[1]	None
GPIO1_45	159	X_MMC1_DAT0	I/O	3.3V[1]	None
GPIO1_46	158	X_MMC1_CLK	I/O	3.3V[1]	49.9K pulldown
GPIO1_47	163	X_MMC1_CMD	I/O	3.3V[1]	None
GPIO1_48	157	X_MMC1_SDCD	I/O	3.3V[1]	10K pullup
GPIO1_49	156	X_MMC1_SDWP	I/O	3.3V[1]	10K pullup
GPIO1_50	73	X_USB0_DRVVBUS	I/O	3.3V[1]	None
GPIO1_51	77	X_USB1_DRVVBUS	I/O	3.3V[1]	None

[1:] The voltage level for this signal is configurable for 1.8V or 3.3V. The default voltage level is listed here, but always check the actual jumper setting for the applicable SOM configuration. Refer to section *4.6 Solder Jumpers* for details.

Table 41 MCU_GPIO0 Accessibility at SOC footprint

Processor Signal	X1 Pin #(s)	SOM Signal(s)	Type	Level	Internal SOM Usage
MCU_GPIO0_1	124	X_MCU_SPI0_CS1	I/O	3.3V[1]	None
MCU_GPIO0_2	121	X_MCU_SPI0_CLK	I/O	3.3V[1]	None
MCU_GPIO0_3	122	X_MCU_SPI0_D0	I/O	3.3V[1]	None
MCU_GPIO0_4	123	X_MCU_SPI0_D1	I/O	3.3V[1]	None
MCU_GPIO0_5	129	X_MCU_UART0_RXD	I/O	3.3V[1]	None
MCU_GPIO0_6	130	X_MCU_UART0_TXD	I/O	3.3V[1]	None
MCU_GPIO0_7	127	X_MCU_UART0_CTSN	I/O	3.3V[1]	None
MCU_GPIO0_8	128	X_MCU_UART0_RTSN	I/O	3.3V[1]	None
MCU_GPIO0_9	113	X_WKUP_UART0_RXD	I/O	3.3V[1]	None
MCU_GPIO0_10	114	X_WKUP_UART0_TXD	I/O	3.3V[1]	None
MCU_GPIO0_11	112	X_WKUP_UART0_CTSN	I/O	3.3V[1]	None
MCU_GPIO0_12	111	X_WKUP_UART0_RTSN	I/O	3.3V[1]	None
MCU_GPIO0_13	116	X_MCU_MCAN0_TX	I/O	3.3V[1]	None
MCU_GPIO0_14	115	X_MCU_MCAN0_RX	I/O	3.3V[1]	None
MCU_GPIO0_15	118	X_MCU_MCAN1_TX	I/O	3.3V[1]	None
MCU_GPIO0_16	117	X_MCU_MCAN1_RX	I/O	3.3V[1]	None
MCU_GPIO0_17	119	X_MCU_I2C0_SCL (Requires pullup)	OD-I/O	3.3V[1]	None
MCU_GPIO0_18	120	X_MCU_I2C0_SDA (Requires pullup)	OD-I/O	3.3V[1]	None
MCU_GPIO0_19	125	X_WKUP_I2C0_SCL (Requires pullup)	OD-I/O	3.3V[1]	None
MCU_GPIO0_20	126	X_WKUP_I2C0_SDA (Requires pullup)	OD-I/O	3.3V[1]	None
MCU_GPIO0_21	185	X_MCU_RESETSTATz	I/O	3.3V[1]	10K pulldown
MCU_GPIO0_23	131	X_WKUP_CLKOUT0	I/O	3.3V[1]	10K pulldown

[1:] The voltage level for this signal is configurable for 1.8V or 3.3V. The default voltage level is listed here, but always check the actual jumper setting for the applicable SOM configuration. Refer to section *4.6 Solder Jumpers* for details.

10.3TIMER

The phyCORE-AM62Ax DSC SOM brings out 12x Timer modules. The modules have a 32-bit data bus width and provide interrupts generated on overflow, compare, and capture.

10.3.1 Timer Pinout

Table 42 Timer Signals

Processor Signal	X1 Pin #(s)	SOM Signal(s)	Type	Level	Description
TIMER_IO0	146	X_I2C1_SCL	I/O	3.3V[1]	Timer Inputs and Outputs
	162	X_MMC1_DAT3			
TIMER_IO1	147	X_I2C1_SDA	I/O	3.3V[1]	Timer Inputs and Outputs
	161	X_MMC1_DAT2			
TIMER_IO2	160	X_MMC1_DAT1	I/O	3.3V[1]	Timer Inputs and Outputs
	143	X_MCAN0_TX			

Processor Signal	X1 Pin #(s)	SOM Signal(s)	Type	Level	Description
TIMER_IO3	159	X_MMC1_DAT0	I/O	3.3V[1]	Timer Inputs and Outputs
	142	X_MCAN0_RX			
TIMER_IO4	132	X_EXT_REFCLK1	I/O	3.3V[1]	Timer Inputs and Outputs
	158	X_MMC1_CLK (49.9K pulldown on SOM)			
TIMER_IO5	163	X_MMC1_CMD	I/O	3.3V[1]	Timer Inputs and Outputs
TIMER_IO6	138	X_UART0_CTSN	I/O	3.3V[1]	Timer Inputs and Outputs
	157	X_MMC1_SDCD (10K pullup on SOM)			
TIMER_IO7	139	X_UART0_RTSN	I/O	3.3V[1]	Timer Inputs and Outputs
	156	X_MMC1_SDWP (10K pullup on SOM)			
MCU_TIMER_IO0	127	X_MCU_UART0_CTSN	I/O	3.3V[1]	Timer Inputs and Outputs
	115	X_MCU_MCAN0_RX			
MCU_TIMER_IO1	128	X_MCU_UART0_RTSN	I/O	3.3V[1]	Timer Inputs and Outputs
	124	X_MCU_SPI0_CS1			
MCU_TIMER_IO2	118	X_MCU_MCAN1_TX	I/O	3.3V[1]	Timer Inputs and Outputs
MCU_TIMER_IO3	117	X_MCU_MCAN1_RX	I/O	3.3V[1]	Timer Inputs and Outputs

[1]: The voltage level for this signal is configurable for 1.8V or 3.3V. The default voltage level is listed here, but always check the actual jumper setting for the applicable SOM configuration. Refer to section *4.6 Solder Jumpers* for details.

11 Debug Interfaces

The following sub-sections detail each of the debug interfaces supported on the phyCORE-AM62Ax DSC.

11.1 JTAG

The phyCORE-AM62Ax DSC SOM is equipped with a JTAG interface for downloading program code into the internal RAM or for debugging programs currently executing. The JTAG interface is accessible via the SOC footprint and provides seven standard IEEE1149.6 JTAG signals.

11.1.1 JTAG Pinout

Table 43 JTAG Connections at the SOC footprint

X1 Pin #(s)	SOM Signal(s)	Type	Level	Description
239	X_EMU0 (5.76K pullup on SOM)	I/O	3.3V[1]	Emulation Control 0
238	X_EMU1 (5.76K pullup on SOM)	I/O	3.3V[1]	Emulation Control 1
246	X_TCK (10K pullup on SOM)	I	3.3V[1]	JTAG Test Clock
245	X_TDI (10K pullup on SOM)	I	3.3V[1]	JTAG Test Data Input
244	X_TDO	O	3.3V[1]	JTAG Test Data Output
243	X_TMS (10K pullup on SOM)	I	3.3V[1]	JTAG Test Mode Select
242	X_TRSTN (10K pulldown on SOM)	I	3.3V[1]	JTAG Reset

[1]: The voltage level for this signal is configurable for 1.8V or 3.3V. The default voltage level is listed here, but always check the actual jumper setting for the applicable SOM configuration. Refer to section *4.6 Solder Jumpers* for details.

11.1.2 JTAG Reference Circuit

An example reference circuit for connecting the JTAG signals to a 2x20 connector is shown below. Note that the pinout is based on TI's compact 20-pin JTAG connector setup. More details on the specifics of that pinout can be found here JTAG Connectors and Pinout.

Figure 37. JTAG Reference Schematic

11.2 TRACE (TRC)

The phyCORE-AM62Ax DSC SOM is equipped with a TRACE (TRC) module that can be used to record operation of the ROM code and debug unexpected occurrences.

11.2.1 TRC Pinout

Table 44 TRC Connections at the SOC footprint

Processor Signal	X1 Pin #(s)	SOM Signal(s)	Type	Level	Description
TRC_CLK	4	X_GPMC0_AD0/BOOTMODE_0[2] (100K pullup on SOM)	O	3.3V[1]	Trace Clock
TRC_CTL	5	X_GPMC0_AD1/BOOTMODE_1[2] (100K pullup on SOM)	O	3.3V[1]	Trace Control
TRC_DATA0	6	X_GPMC0_AD2/BOOTMODE_2[2] (100K pulldown on SOM)	O	3.3V[1]	Trace Data 0
TRC_DATA1	7	X_GPMC0_AD3/BOOTMODE_3[2] (100K pullup on SOM)	O	3.3V[1]	Trace Data 1
TRC_DATA2	8	X_GPMC0_AD4/BOOTMODE_4[2] (100K pulldown on SOM)	O	3.3V[1]	Trace Data 2
TRC_DATA3	9	X_GPMC0_AD5/BOOTMODE_5[2] (100K pulldown on SOM)	O	3.3V[1]	Trace Data 3
TRC_DATA4	10	X_GPMC0_AD6/BOOTMODE_6[2] (100K pullup on SOM)	O	3.3V[1]	Trace Data 4
TRC_DATA5	11	X_GPMC0_AD7/BOOTMODE_7[2] (100K pulldown on SOM)	O	3.3V[1]	Trace Data 5
TRC_DATA6	22	X_GPMC0_CLK	O	3.3V[1]	Trace Data 6
TRC_DATA7	174	X_GPMC0_ADVn_ALE	O	3.3V[1]	Trace Data 7
TRC_DATA8	178	X_GPMC0_OEn_REn	O	3.3V[1]	Trace Data 8
TRC_DATA9	179	X_GPMC0_WEn	O	3.3V[1]	Trace Data 9
TRC_DATA10	173	X_GPMC0_BE0n_CLE	O	3.3V[1]	Trace Data 10
TRC_DATA11	172	X_GPMC0_BE1n	O	3.3V[1]	Trace Data 11
TRC_DATA12	20	X_GPMC0_WAIT0	O	3.3V[1]	Trace Data 12
TRC_DATA13	177	X_GPMC0_WPn	O	3.3V[1]	Trace Data 13
TRC_DATA14	21	X_GPMC0_DIR	O	3.3V[1]	Trace Data 14
TRC_DATA15	3	X_GPMC0_CSn0	O	3.3V[1]	Trace Data 15
TRC_DATA16	2	X_GPMC0_CSn1	O	3.3V[1]	Trace Data 16
TRC_DATA17	1	X_GPMC0_CSn2	O	3.3V[1]	Trace Data 17
TRC_DATA18	175	X_GPMC0_CSn3	O	3.3V[1]	Trace Data 18
TRC_DATA19	19	X_GPMC0_AD15/BOOTMODE_15[2] (100K pulldown on SOM)	O	3.3V[1]	Trace Data 19
TRC_DATA20	18	X_GPMC0_AD14/BOOTMODE_14[2] (100K pulldown on SOM)	O	3.3V[1]	Trace Data 20
TRC_DATA21	17	X_GPMC0_AD13/BOOTMODE_13[2] (100K pullup on SOM)	O	3.3V[1]	Trace Data 21
TRC_DATA22	16	X_GPMC0_AD12/BOOTMODE_12[2] (100K pullup on SOM)	O	3.3V[1]	Trace Data 22
TRC_DATA23	15	X_GPMC0_AD11/BOOTMODE_11[2] (100K pulldown on SOM)	O	3.3V[1]	Trace Data 23

[1:] The voltage level for this signal is configurable for 1.8V or 3.3V. The default voltage level is listed here, but always check the actual jumper setting for the applicable SOM configuration. Refer to section *4.6 Solder Jumpers* for details.
[2:] This signal should not be driven during reset. More information can be found in section *6.3 System Boot Configuration.*

11.3 UART0

The phyCORE-AM62Ax DSC SOM can also be communicated with using UART0 for downloading program code into the internal RAM or for debugging programs currently executing. UART0 is the default console and as such PHYTEC recommends bringing out UART0 for console access. The UART0 interface is accessible via the SOC footprint.

11.3.1 UART0 Pinout

Table 45 UART0 Connections at the SOC footprint

X1 Pin #(s)	SOM Signal(s)	Type	Level	Description
140	X_UART0_RX	I	3.3V[1]	UART0 Receive Data
141	X_UART0_TX	O	3.3V[1]	UART0 Transmit Data
138	X_UART0_CTS	I	3.3V[1]	UART0 Clear to Send
139	X_UART0_RTS	O	3.3V[1]	UART0 Request to Send

[1:] The voltage level for this signal is configurable for 1.8V or 3.3V. The default voltage level is listed here, but always check the actual jumper setting for the applicable SOM configuration. Refer to section *4.6 Solder Jumpers* for details.

11.3.2 UART0 Reference Circuits

An example reference circuit for connecting the UART0 signals to a Micro USB connector is shown below.

Figure 38. UART0 to USB Bridge Reference Schematic

Figure 39. UART0 to USB Buffers and Regulator Reference Schematic

The circuit consists of:

- Four buffers to isolate the UART signals from the bridge/header until SOM power is brought up and PGOOD has gone high (this is important as driving these signals high to early will prevent the SOM from powering on)
- A dual UART to USB bridge to convert the UART signals into USB signals

- A TVS diode array for ESD protection
- A micro-USB connector
- A DC regulator to convert the 5V USB power to 3.3V

A simpler design that just brings out the bare minimum UART signals for use with FTDI USB adapter cables is shown below. Note that the buffers are still required to prevent power back feeding into the SOM, preventing it from properly turning on.

Figure 40. Simple UART0 Reference Schematic

12 System Interfaces

The following sub-sections detail the system signals brought out to the phyCORE connectors from the MAIN, MCU, and WKUP domains of the AM62Ax processor that are not discussed elsewhere in the manual. It also covers the on-board RTC and the two heartbeat LEDs.

12.1 MAIN Pinout

Table 46 MAIN Connections at the SOC footprint

Processor Signal	X1 Pin #(s)	SOM Signal(s)	Type	Level	Description
CLKOUT0	132	X_EXT_REFCLK1	O	3.3V[1]	Clock Output
EXTINTn	237	X_RTC_INT (10K pullup on SOM)	I	3.3V[1]	External Interrupt
EXT_REFCLK1	132	X_EXT_REFCLK1	I	3.3V[1]	External clock input to Main Domain
GPMC0_FCLK_MUX	22	X_GPMC0_CLK	O	3.3V[1]	GPMC functional clock output
OBSCLK0	14	X_GPMC0_AD10/BOOTMODE_10[2] (100K pullup on SOM)	O	3.3V[1]	Observation clock output for test and debug
PORz_OUT	187	X_PORz_OUT (1.5K pulldown on SOM)	O	3.3V[1]	Main Domain POR status output
RESETSTATz	180	X_RESETSTATz (10K pulldown on SOM)	O	3.3V[1]	Main Domain warm reset status output
RESET_REQz	188	X_RESET_REQz (100K pullup on SOM)	I	3.3V[1]	Main Domain external warm reset request input
SYSCLKOUT0	132	X_EXT_REFCLK1	O	3.3V[1]	SYSCLK0 output from Main PLL controller for test and debug
AUDIO_EXT_REFCLK0	138	X_UART0_CTSN	I/O	3.3V[1]	External clock input/ouput for MCASP
	51	X_CPSW_RGMII2_RD3			
	155	X_MCASP0_AXR0			
AUDIO_EXT_REFCLK1	139	X_UART0_RTSN	I/O	3.3V[1]	External clock input/ouput for MCASP
	149	X_MCASP0_AFSX			
	177	X_GPMC0_WPn			

[1]: The voltage level for this signal is configurable for 1.8V or 3.3V. The default voltage level is listed here, but always check the actual jumper setting for the applicable SOM configuration. Refer to section *4.6 Solder Jumpers* for details.

[2]: This signal should not be driven during reset. More information can be found in section *6.3 System Boot Configuration.*

12.2 MCU Pinout

Table 47 MCU Connections at the SOC footprint

Processor Signal	X1 Pin #(s)	SOM Signal(s)	Type	Level	Description
MCU_OBSCLK0	124	X_MCU_SPI0_CS1	O	3.3V[1]	Observation clock output for test and debug
MCU_RESETSTATz	185	X_MCU_RESETSTATz (10K pulldown on SOM)	O	3.3V[1]	MCU Domain warm reset status output
MCU_RESETz	186	X_MCU_RESETz (100K pullup on SOM)	I	3.3V[1]	MCU Domain warm reset
MCU_ERRORn	181	X_MCU_SAFETY_ERRORn	I/O	1.8V	Error signal output from MCU Domain ESM
MCU_EXT_REFCLK0	124	X_MCU_SPI0_CS1	I	3.3V[1]	External input to MCU Domain
	118	X_MCU_MCAN1_TX			
MCU_SYSCLKOUT0	124	X_MCU_SPI0_CS1	O	3.3V[1]	MCU Domain system clock output for test and debug

[1]: The voltage level for this signal is configurable for 1.8V or 3.3V. The default voltage level is listed here, but always check the actual jumper setting for the applicable SOM configuration. Refer to section *4.6 Solder Jumpers* for details.

12.3 WKUP Pinout

Table 48 WKUP Connections at the SOC footprint

Processor Signal	X1 Pin #(s)	SOM Signal(s)	Type	Level	Description
WKUP_CLKOUT0	131	X_WKUP_CLKOUT0	O	3.3V[1]	WKUP Domain CLKOUT0 output

[1]: The voltage level for this signal is configurable for 1.8V or 3.3V. The default voltage level is listed here, but always check the actual jumper setting for the applicable SOM configuration. Refer to section *4.6 Solder Jumpers* for details.

12.4 RTC

The on-board RTC provides accurate time keeping (±1 ppm @ 25°C) at extremely low power consumption (40 nA @ 3 V). The RTC can keep track of the year, month, date, weekday, hour, minute, and seconds and has timer, alarm, and external event input functionality.

12.4.1 RTC Pinout

Table 49 RTC Connections at the SOC footprint

X1 Pin #(s)	SOM Signal(s)	Type	Level	Description
240	X_RTC_EVI[2] (10K pullup on SOM)	I	3.3V[1]	RTC Event Input
237	X_RTC_INT (10K pullup on SOM)	I	3.3V[1]	RTC Interrupt

[1]: The voltage level for this signal is configurable for 1.8V or 3.3V. The default voltage level is listed here, but always check the actual jumper setting for the applicable SOM configuration. Refer to section *4.6 Solder Jumpers* for details.
[2]: The signal brought out at this pin is controlled by a jumper. Refer to section *4.6 Solder Jumpers* for details.

12.5 Heartbeat LEDs

The phyCORE-AM62Ax has two LEDs, one green (connected to the Linux domain) and one red (connected to the MCU domain), named the heartbeat LEDs. In PHYTEC's software, the green LED is configured to flash in a heartbeat pattern once the SOM starts booting into Linux. This provides a visual indicator that the board is booting during debug. However, the user can configure the LEDs to behave in a manner most suitable to their design needs. The red LED is connected to MCU_GPIO0_0 (processor ball E11) and the green LED is connected to GPIO0_13 (processor ball K20).

13 Integrating and Updating the phyCORE-AM62Ax DSC

13.1 Integration

The various reference circuits contained in sections 5-12 as well as the information in section *4.5 Minimum Requirements for Operation* can be used as a starting point for integrating the phyCORE-AM62Ax DSC SOM into target circuitry. Additional information is available to facilitate the integration of the phyCORE-AM62Ax DSC SOM into customer applications, such as:

phyCORE-AM62Ax SOM and Carrier Board Schematic References:

- Schematics are made available upon request here.

phyCORE-AM62Ax Pin Resources:

- PHYTEC recommends the use of TI's System Configuration Tool
- Access to PHYTEC's pinmuxing tool is available here.

phyCORE-AM62Ax Symbol/Cell Resources:

- Symbols/cells of the SOM connector are available here.

Phone, e-mail, FAQ, wiki, and other online support by visiting http://PHYTEC.com/contact/

13.2 Modification

Removal of various components, such as the SoC and the standard quartz, is not advisable given the compact nature of the module. Should this nonetheless be necessary, please ensure that the board as well as surrounding components and sockets remain undamaged while de-soldering. Overheating the board can cause the solder pads to loosen, rendering the SOM inoperable.

CAUTION:
If any modifications to the module are performed, regardless of their nature, the manufacturer warranty is voided.

13.3 In-Field Updates

It is important that your system is designed so that firmware can be updated remotely in case there are issues in the field. PHYTEC recommends choosing at least one or more of the following design features:

- Include an Ethernet jack in your design that can be used to access the system. See section *7.2.2 Ethernet Design In Guide* for more details on integrating Ethernet into your design.

- Add a Wi-Fi module to your design connected to MMC2. See section *6.2.2.2 MMC Design In Considerations* for more details.
- Add an SD card slot from which new software can be flashed to the device. This is especially useful when internet is inaccessible, intermittent, or if Ethernet connection is not possible.

13.4 Product Change Management

Use of PHYTEC products ensures interchangeable SoC core circuitry in the event of obsolescence of parts used on our SOMs and SBCs. End users no longer need to redesign entire CPU circuitry and engage in version control to accommodate new or obsolete parts. Instead, PHYTEC manages this at the SOM-level. PHYTEC ensures continued availability of pin- and function-compatible SOMs and SBCs, further minimizing maintenance costs and risks. This pro-active product lifecycle management (PLM) policy has enabled deployment of the same PHYTEC SOM in designs for over twenty years. See https://www.phytec.com/support/product-lifecycle-management/ for more details on our Product Longevity, Product Obsolescence and Product Maintenance policies.

14 Additional Information

Members of PHYTEC's phyCORE® product family can be populated with different processors and offer various functions and configurations. PHYTEC supports a variety of ARM-based and other SoC in two ways.

1. As the basis for PHYTEC development kits and Single Board Computers, which serves as a reference and evaluation platform.
2. As insert-ready, fully functional phyCORE® OEM System on Modules (SOMs) and phyBOARD Single Board Computers (SBCs), which can be incorporated directly into the user's hardware design.

For more information go to: *https://PHYTEC.com/design-services/*

Declaration of Electromagnetic Conformity of the
PHYTEC phyCORE-AM62Ax DSC System On Module

PHYTEC System on Modules (SOM) and Single Board Computers (SBC) are designed as subcomponents for integration in electrical devices.

Combined with PHYTEC Carrier Boards, PHYTEC SOMs can be used as dedicated Evaluation Boards (i.e.: for use as a test and prototype platform for hardware/software development) in laboratory environments.

CAUTION:
PHYTEC products lacking protective enclosures are subject to damage by ESD and, hence, may only be unpacked, handled or operated in environments in which sufficient precautionary measures have been taken in respect to ESD-dangers. It is also necessary that only appropriately trained personnel (such as electricians, technicians, electronic manufacturing personnel and engineers) handle and/or operate these products.

PHYTEC products fulfill the rules and regulations of the European Union's Directive for Electromagnetic Conformity and the Federal Communications Commission Title 47 CFR Part 15 Subpart B only in accordance with the descriptions and rules of usage indicated in this hardware manual, particularly in respect to the external SOM connector, power interfaces and interfaces to host systems for programming.

NOTE:
Integration of PHYTEC products into target devices, as well as user modifications and extensions of PHYTEC products, is subject to renewed establishment of conformity to, and certification of, Electromagnetic Directives. Users should ensure conformance following any modifications to the products as well as implementation of the products into target systems.

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15 Revision History

Table 50 Document Revision History

Date	Version Number	Changes in this Manual
2023/10/30	L-1061e.A0	Preliminary Release