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IEEE Standard for Low-Rate Wireless Networks

Amendment 2: Ultra-Low Power Physical Layer

IEEE Computer Society

Sponsored by the
LAN/MAN Standards Committee

IEEE
3 Park Avenue
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USA

IEEE Std 802.15.4q™-2016
(Amendment to
IEEE Std 802.15.4™-2015
as amended by IEEE Std 802.15.4n™-2016)

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Approved 29 January 2016

IEEE-SA Standards Board

Abstract: Two alternate physical layers (PHYs), TASK and RS-GFSK, are specified in this amendment in addition to the PHYs of IEEE Std 802.15.4-2015. The amendment also defines the medium access control (MAC) modifications needed to support the implementation of the TASK and RS-GFSK PHYs. These alternate PHYs enable low-cost, ultra-low power consumption, as well as extended battery life, in various frequency bands and geographical regions under multiple regulatory domains.

Keywords: amendment, IEEE 802.15.4™, IEEE 802.15.4q™, low data rate, LR-WPAN, PAN, personal area network, PHY, physical layer, radio frequency, RF, ultra-low power, wireless personal area network, WPAN

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Introduction

This introduction is not part of IEEE Std 802.15.4q™-2016, IEEE Standard for Low-Rate Wireless Networks—Amendment 2: Ultra-Low Power Physical Layer.

For over a decade, the IEEE P802.15 Working Group successfully developed wireless personal area network (WPAN) standards (IEEE Std 802.15.4™) with low energy consumption in mind. However, further reduction in energy consumption is desired to address emerging markets like wearable devices, electronic shelf labeling, and automation where the energy sources, driven by size and cost constraints, are limited to small batteries (e.g., coin cell batteries). These energy sources have substantially less capacity and peak power ratings than traditional batteries (e.g., size AA or AAA). This trend calls for an amendment that aims for further reduction in energy consumption and peak power. It is expected that this amendment could also benefit the traditional markets, which have already been successfully addressed by IEEE Std 802.15.4.

This amendment specifies two alternative physical layers (PHYs), TASK and RS-GFSK, in addition to the PHYs of IEEE Std 802.15.4-2015. The amendment also defines the medium access control (MAC) modifications needed to support the implementation of the TASK and RS-GFSK PHYs. Both PHYs are specified for 2.4 GHz and several sub-gigahertz bands using multiple data rates up to 1 Mb/s.

The TASK PHY specifies a physical layer based on amplitude shift keying with ternary amplitude sequence spreading (TASK). This PHY allows implementation of transceivers with low complexity and enables low power consumption. As an important feature, this PHY also supports communications in both coherent and noncoherent modes of reception and thereby allows tradeoff between receiver complexity and performance.

The RS-GFSK PHY specifies a physical layer based on Gaussian frequency shift keying (GFSK). This PHY provides low-power benefits by the availability of higher data rates, reduced overhead in the PHY protocol data unit (PPDU), and transmission (TX) power control. In addition, the RS-GFSK PHY provides options to interoperate with the existing SUN FSK PHY (which involves smart utility network frequency shift keying). A wide range of applications will benefit from the energy savings enabled by the RS-GFSK PHY, including electronic shelf labels, home area networks, smart irrigation systems, and smart metering.

Thejaswi et al. [B18] describe the features and benefits of TASK PHY. Details on the use and merits of the RS-GFSK PHY are provided by de Ruijter [B5a].[a]

[a]The numbers in brackets correspond to the numbers of the bibliography in Annex A.

Contents

IEEE Standard for Low-Rate Wireless Networks

Amendment 2: Ultra-Low Power Physical Layer

(This amendment is based on IEEE Std 802.15.4™-2015 as amended by IEEE Std 802.15.4n™-2016.)

NOTE—The editing instructions contained in this amendment define how to merge the material contained therein into the existing base standard and its amendments to form the comprehensive standard. The editing instructions are shown in ***bold italic***. Four editing instructions are used: change, delete, insert, and replace. ***Change*** is used to make corrections in existing text or tables. The editing instruction specifies the location of the change and describes what is being changed by using ~~strikethrough~~ (to remove old material) and underscore (to add new material). ***Delete*** removes existing material. ***Insert*** adds new material without disturbing the existing material. Deletions and insertions may require renumbering. If so, renumbering instructions are given in the editing instruction. ***Replace*** is used to make changes in figures or equations by removing the existing figure or equation and replacing it with a new one. Editing instructions, change markings, and this NOTE will not be carried over into future editions because the changes will be incorporated into the base standard.[1]

[1]Notes in text, tables, and figures are given for information only and do not contain requirements needed to implement the standard.

3. Definitions, acronyms, and abbreviations

3.2 Acronyms and abbreviations

Insert the following abbreviations in alphabetical order into 3.2:

RS-GFSK	rate switch Gaussian frequency shift keying
SiPC	single parity check
TASK	ternary amplitude shift keying

5. General description

5.6 Architecture

5.6.1 PHY

Insert in 5.6.1 the following list item at the end of the dashed list of the second paragraph:

— For TASK PHY and RS-GFSK PHY: Nair et al. [B9b].[2]

6. MAC functional description

Insert the following subclause (6.17) after 6.16:

6.17 Using Link Margin IE in an RS-GFSK PAN

A device may include an RS-GFSK Link Margin IE within an enhanced acknowledgment. The RS-GFSK Link Margin IE shall only be transmitted as part of an Enh-Ack frame.

If a device receives an Enh-Ack frame containing an RS-GFSK Link Margin IE, it may adjust its transmit power within its power control range in all following GTS transmissions directed to the originating device. The transmit power control shall ignore the RS-GFSK Link Margin IE when the device is transmitting non-GTS frames. The RS-GFSK Link Margin IE is described in 7.4.4.32.

If an acknowledgment for a transmission to a particular device is not received, the transmit power for transmissions to that device may be increased for the next transmission attempt.

The algorithm that controls the transmission of the RS-GFSK Link Margin IE and the algorithm that acts on the reception of the RS-GFSK Link Margin IE are outside the scope of this standard.

If the security level, as described in 9.4.1.1, of the incoming Enh-Ack frame containing the RS-GFSK Link Margin IE is lower than that of the frame being acknowledged, then the RS-GFSK Link Margin IE shall be ignored.

[2]The numbers in brackets correspond to the numbers of the bibliography in Annex A.

7. MAC frame formats

7.4 IEs

7.4.4 Nested IE

7.4.4.1 Format of Nested IE

Insert the following rows into Table 7-16 by Sub-ID value order, and change the reserved row as indicated:

Table 7-16—Sub-ID allocation for short format

Sub-ID value	Name	Enhanced Beacon	Enhanced ACK	Data	Multipurpose	MAC command	Format subclause	Use description	Used by	Created by
0x37	RS-GFSK Link Margin IE		X				7.4.4.32	6.17	UL, MAC	UL, MAC
0x38	RS-GFSK Device Capabilities IE	X	X	X	X		7.4.4.33	6.17, 32.3	UL, MAC	UL, MAC
~~0x37~~0x39– 0x7f	Reserved									

Insert the following subclauses and figures (7.4.4.32 and 7.4.4.33 with Figure 7-101a through Figure 7-101c) after 7.4.4.31:

7.4.4.32 RS-GFSK Link Margin IE

The RS-GFSK Link Margin IE is optional and shall only be used in Enh-Ack frames that use the RS-GFSK-PHY. The IE Content field of the RS-GFSK Link Margin IE shall be formatted as illustrated in Figure 7-101a.

Bits: 0–5	6–7
Link Margin	Reserved

Figure 7-101a—RS-GFSK Link Margin IE Content field format

The Link Margin field shall be set to the available link margin, represented as a twos-complement number, defining the link margin in decibels with a range from –31 dB to 32 dB, in steps of 1 dB. The Link Margin field shall comply with the following equation:

$$\text{Link Margin} = S_{\text{received}} - S$$

where

$S_{received}$ is the received power, in dBm, during a frame
S is the receiver sensitivity as specified in 32.4.3

$S_{received}$ shall be obtained with an accuracy of equal to or less than ± 6 dB.

For example, if the received power is –71 dBm while receiving a frame transmitted in MCS 2 with FEC disabled, then this frame may have the RS-GFSK Link Margin IE included in a subsequent Enh-Ack frame with the link margin set to 20 dB.

7.4.4.33 RS-GFSK Device Capabilities IE

The RS-GFSK Device Capabilities IE is optional and only valid for the RS-GFSK PHY. The IE Content field of RS-GFSK Device Capabilities IE shall be formatted as illustrated in Figure 7-101b.

Octets: 1	2	2
RS-GFSK Features	Frequency Bands Supported	PHY MCS Levels Supported

Figure 7-101b—RS-GFSK Device Capabilities IE Content field format

The RS-GFSK Features field shall be formatted as illustrated in Figure 7-101c.

Bits: 0	1	2	3	4–7
Rate Switch	Short PHR	FEC	Link Margin	Reserved

Figure 7-101c—RS-GFSK Features field format

The Rate Switch field shall be set to one if rate switch mode, as described in 32.3, is supported and shall be set to zero otherwise.

The Short PHR field shall be set to one if the short PHR, as defined in 32.1.4, is supported and shall be set to zero otherwise. When the short PHR is supported, the device shall be responsive to both states of the received Short PHR bit in the PHY header as described in 32.1.3 and 32.1.4. It also means that the device shall be capable of transmitting a Short PHR field as described in 32.1.4 and a Long PHR as described in 32.1.3.

The FEC field shall be set to one if FEC, as described in 32.2.7, is supported and shall be set to zero otherwise. When the FEC field is set to one, the device shall be responsive to the received SFD as described in 32.1.2 and 32.2.7 in both FEC enabled and FEC disabled cases. It also means that the device is capable of transmitting with FEC enabled as described in 32.1.2 and 32.2.7; however, it may transmit without FEC enabled.

The Link Margin field in Figure 7-101c shall be set to one if acting on the RS-GFSK Link Margin IE, as described in 6.17, is supported and shall be set to zero otherwise. When the Link Margin field is set to one, the device shall be responsive to the received RS-GFSK Link Margin IE as described in 7.4.4.32, when its control range allows.

The Frequency Bands Supported field is a bitmap in which bit *n* shall be set to one if the frequency band in Table 10-4c associated with the frequency band identifier *n* is supported and shall be set to zero otherwise. The unused bit in the Frequency Bands Supported field is reserved. The supported frequency bands shall be supported in both transmit and receive.

The PHY MCS Levels Supported field is a bitmap in which bit *n* shall be set to one if the MCS in Table 32-2 associated with the RS-GFSK MCS mode *n* is supported and shall be set to zero otherwise. The unused bits in the PHY MCS Levels Supported field are reserved. When rate switch is supported, for each of the supported 2-GFSK MCS, there shall be an operating mode from Table 32-3 that will provide double data rate, as described in 32.3. A device shall be capable of receiving the MCS as indicated in its transmitted RS-GFSK Device Capabilities IE. The device is permitted to transmit in any other MCS.

This IE is used by the higher layer and MAC and may be transmitted as part of an Enhanced Beacon frame, a Data frame, a Command frame, and a Multipurpose frame.

8. MAC services

8.3 MAC data service

8.3.1 MCPS-DATA.request

Change the following row in Table 8-75 as indicated:

Table 8-75—MCPS-DATA.request parameters

Name	Type	Valid range	Description
DataRate	Integer	0–7	Indicates the data rate. For CSS PHYs, a value of one indicates 250 kb/s while a value of two indicates 1 Mb/s. For HRP UWB PHYs, values 1–4 are valid and are defined in 16.2.6. For LRP UWB PHYs, valid values are defined in Table 19-1. For the SUN OFDM PHY, values 1–7 are valid; each data rate value corresponds to the variable MCS {DataRate-1}, as described in Table 21-9. For the SUN O-QPSK PHY with DSSS spreading, values 1-4 are valid; each data rate value corresponds to the Rate Mode plus one, as described in Table 22-1. For the SUN O-QPSK PHY with MDSSS spreading, values 5-8 are valid; each data rate value corresponds to the Rate Mode plus five, as described in Table 22-1. For MSK PHYs, valid value are defined in Table 18-1. For TASK PHY, values 0–7 are valid: each value corresponds to the MCS mode as described in 31.3 (given in Table 31-5, Table 31-6, and Table 31-7). For RS-GFSK PHY, values 0–7 are valid; each value corresponds to the MCS mode as described in 32.2 (given in Table 32-2). For all other PHYs, the parameter is set to zero.

10. General PHY requirements

10.1 General requirements and definitions

10.1.1 Operating frequency range

Insert the following paragraph and table (Table 10-4c) at the end of 10.1.1:

A TASK or RS-GFSK PHY compliant device shall be able to support transmission and reception in one or more of the frequency bands defined in Table 10-4c.

Table 10-4c—TASK and RS-GFSK PHY frequency band definitions

Frequency band identifier	Frequency band (MHz)	Band designation
0	169.400–169.475	169 MHz
1	433.050–434.790	433 MHz
2	450–470	450 MHz
3	470–510	470 MHz
4	779–787	780 MHz
5	863–876	863 MHz
6	896–901	896 MHz
7	901–902	901 MHz
8	902–928	915 MHz
9	915–921	918 MHz
10	917–923.5	917 MHz
11	928–960	928 MHz
12	1427–1518	1427 MHz
13	2400–2483.5	2450 MHz

10.1.2 Channel assignments

Insert the following subclause and tables (10.1.2.13 with Table 10-15c and Table 10-15d) after 10.1.2.12:

10.1.2.13 Channel numbering for TASK and RS-GFSK PHYs

The channel center frequency for TASK and RS-GFSK PHYs shall be derived as follows:

$$ChanCenterFreq = ChanCenterFreq_0 + NumChan \times ChanSpacing$$

where

ChanCenterFreq$_0$ is the first channel center frequency
ChanSpacing is the separation between two adjacent channels
NumChan is the channel number from 0 to *TotalNumChan*–1
TotalNumChan is the total number of channels for the available frequency band

The parameters *ChanSpacing*, *TotalNumChan*, and *ChanCenterFreq*$_0$ for different frequency bands for TASK are specified in Table 10-15c. The parameters *ChanSpacing*, *TotalNumChan*, and *ChanCenterFreq*$_0$ for different frequency bands and MCS levels for RS-GFSK are specified in Table 10-15d. The MCS levels for RS-GFSK PHY are numbered as described in Table 32-2 and Table 32-3.

For specifics of the MCS modes as shown in Table 10-15d, see Table 32-2 and Table 32-3.

Table 10-15c—Total number of channels and first channel center frequencies for TASK PHYs

Frequency band identifier	*ChanSpacing* (MHz)	*TotalNumChan*	$ChanCenterFreq_0$ (MHz)
1	0.4	4	433.3
3	0.8	50	470.4
4	2	4	780
5	2	6	864
8	2	10	906
13	5	16	2405

Table 10-15d—Total number of channels and first channel center frequencies for RS-GFSK PHYs

Frequency band (MHz)	MCS mode	*ChanSpacing* (MHz)	*TotalNumChan*	$ChanCenterFreq_0$ (MHz)
169.400–169.475	0, 0a	0.0125	6	169.40625
	1, 1a	0.025	3	169.4125
433.050–434.790	0, 0a	0.0125	139	433.0625
	1, 1a	0.025	69	433.075
	2, 2a	0.2	8	433.25
450–470	0, 0a	0.0125	1600	450.00625
	1, 1a	0.025	800	450.0125
	2, 2a	0.2	100	450.100
	3, 3a	0.4	50	450.200
	4, 4a, 6	1.0	20	450.500
	5	0.5	40	450.250
	7	2.0	10	451.000
470–510	1, 1a	0.025	1600	470.025
	2, 2a	0.2	200	470.2
	3, 3a	0.4	100	470.4
	4, 4a, 6	1.0	40	471.0
	5	0.5	80	470.5
	7	2.0	20	472.0

Table 10-15d—Total number of channels and first channel center frequencies for RS-GFSK PHYs *(continued)*

Frequency band (MHz)	MCS mode	*ChanSpacing* (MHz)	*TotalNumChan*	$ChanCenterFreq_0$ (MHz)
779–787	2, 2a	0.2	40	779.2
	3, 3a	0.4	20	779.4
	4, 4a, 6	1.0	8	780.0
	5	0.5	16	779.5
863–876	2, 2a	0.2	65	863.125
	3, 3a	0.4	32	863.225
	4, 4a, 6	1.0	13	864.0
	5	0.5	26	863.5
	7	2.0	6	865.0
896–901	0, 0a	0.0125	400	896.0125
	1, 1a	0.025	200	896.025
	5	0.5	10	896.5
901–902	0, 0a	0.0125	80	901.0125
	1, 1a	0.025	20	901.025
902–928	2, 2a	0.2	130	902.2
	3, 3a	0.4	65	902.4
	4, 4a, 6	1.0	26	903.0
	5	0.5	52	902.5
	7	2.0	13	904.0
916–928	2, 2a, 3, 3a, 4, 4a, 5, 6, 7	0.1	121	916.0
917–923.5	2, 2a	0.2	33	917.1
	3, 3a	0.4	16	917.3
	5	0.5	13	917.5
928–960	0, 0a, 1, 1a	0.2	160	928.0125
1427–1518	0, 0a, 1, 1a	0.2	455	1427.0125
2400–2483.5	2, 2a	0.2	417	2400.2
	3, 3a	0.4	208	2400.4
	4, 4a, 6	1.0	83	2401.0
	5	0.5	167	2400.5
	7	2.0	41	2402.0

11. PHY services

11.2 PHY constants

Change the following row in Table 11-1 as indicated:

Table 11-1—PHY constants

Attribute	Description	Value
aTurnaroundTime	RX-to-TX or TX-to-RX turnaround time (in symbol periods), as defined in 10.2.1 and 10.2.2	For the SUN, RS-GFSK, TVWS, and LECIM FSK PHYs, the value is 1 ms expressed in symbol periods, rounded up to the next integer number of symbol periods using the ceiling() function.[a] For the LECIM DSSS PHY, the value is 1 ms expressed in modulation symbol periods, rounded up to the next integer number of symbol periods using the ceiling() function. The value is 12 for all other PHYs.

[a]The function ceiling() returns the smallest integer value greater than or equal to its argument value.

11.3 PHY PIB attributes

Change the phyFskFecEnabled row as indicated, and insert the following rows at the end of Table 11-2:

Table 11-2—PHY PIB attributes

Attribute	Type	Valid range	Description
phyFskFecEnabled	Boolean	TRUE, FALSE	A value of TRUE indicates that FEC is turned on. A value of FALSE indicates that FEC is turned off. This attribute is only valid for the SUN FSK, ~~and~~ TVWS FSK PHY, and RS-GFSK PHY.
...			
phyRsGfskShortPhrEnabled	Boolean	TRUE, FALSE	This attribute is only valid for the RS-GFSK PHY. It indicates whether the device is using Short PHR in its transmission as described in 32.1.4. If TRUE, the device is using Short PHR. If FALSE, it is using a Long PHR.
phyRsGfskPreambleLength	Integer	2-15	This attribute is only valid for the RS-GFSK PHY. It is the number of repetitions of 1-octet patterns, as described in 32.1.1, in the preamble of an RS-GFSK PHY.
phyRsGfskPrecode	Boolean	TRUE, FALSE	This attribute is only valid for the RS-GFSK PHY. If TRUE, differential precoding, as described in 32.2.2, is employed for the RS-GFSK PHY. If FALSE, it is not.
phyRsGfskSfd	Integer	0, 1	This attribute is only valid for the RS-GFSK PHY. It determines which group of SFDs is used, as described in Table 32-1.

Insert new Clause 31 and Clause 32 after Clause 30:

31. TASK PHY

31.1 General

The ternary amplitude shift keying (TASK) PHY employs ternary sequence spreading followed by ASK modulation.

For TASK PHY, the symbol duration parameters for MAC and PHY timing shall be set as given in Table 31-1 for different bands of operations. Symbol period is defined as the value of one symbol duration.

Table 31-1—TASK symbol duration used for MAC and PHY timing parameters

Frequency band (MHz)	Chip rate (Mchip/s)	Symbol duration (µs)
433.050–434.790	0.25	64
470–510	0.25	64
779–787	0.6	26.667
863–876	0.6	26.667
902–928	0.6	26.667
2400–2483.5	1	16

31.2 PPDU

The PPDU structure is presented so that the leftmost field of the PPDU shall be transmitted or received first. For all multi-octet fields, the leftmost octet represents the least significant octet, and for each octet, the leftmost bit represents the LSB. Unless otherwise stated, all multi-octet fields shall be transmitted or received least significant octet first, and each octet shall be transmitted or received LSB first.

31.2.1 PPDU format

The format for the PPDU shall be formatted as illustrated in Figure 12-1 (in 12.1).

31.2.1.1 SHR field

31.2.1.1.1 Structure of the SHR field

The SHR field shall have the Preamble field followed by the SFD field as illustrated in Figure 12-2 (in 12.1.1). The formats of the individual Preamble and SFD fields are explained in the following subclauses.

31.2.1.1.2 Preamble field

The Preamble field shall have a unique ternary base sequence of length 32 chips repeated 8 times. This 32-chip base sequence is given by [1 0 –1 0 0 –1 0 –1 1 0 1 0 0 –1 0 1 1 0 1 0 0 –1 0 1 –1 0 1 0 0 1 0 1].

In the coherent reception mode, the preamble is equivalent to a string of 8 bits spread by a sequence with a spreading factor of 32, and in the noncoherent reception mode, the preamble is equivalent to a string of 32 bits spread by a sequence with a spreading factor of 8.

31.2.1.1.3 SFD field

The SFD field indicates the end of SHR field. The SFD field shall consist of a pattern of 8 bits, [0 1 0 1 1 0 0 1]. The bits in this field are mapped onto a ternary spreading code comprising two orthogonal ternary sequences. The bit-to-sequence mapping shall be as given in Table 31-2.

Table 31-2—Spreading of the SFD field

SFD bit	Bit-to-sequence mapping
0	[0 –1 0 1 1 0 –1 0]
1	[1 0 –1 0 0 –1 0 1]

31.2.1.2 PHR Field

31.2.1.2.1 Structure of the PHR field

The PHR shall be constructed as shown in Figure 31-1.

Bits: 0–6	7	8–10	11	12–15
Length	Reserved	MCS	Reserved	HCS

Figure 31-1—Format of the PHR field

31.2.1.2.2 Length field

The Length field specifies the total number of octets contained in the PSDU.

31.2.1.2.3 MCS field

The MCS field specifies the modulation format and the FEC to be applied on the PSDU. Four modulation formats and two FECs are provided. Valid values of the MCS field and the corresponding mapping of the modulation format and the FECs are given in Table 31-3.

Table 31-3—Mapping of the MCS field

MCS field (b8, b9, b10)	Modulation format	FEC
(0, 0, 0)	1/1-TASK	Bose Chaudhuri Hocquenghem (BCH)
(1, 0, 0)	2/4-TASK	BCH with interleaving
(0, 1, 0)	3/8-TASK	BCH with interleaving
(1, 1, 0)	5/32-TASK	BCH with interleaving

Table 31-3—Mapping of the MCS field *(continued)*

MCS field (b8, b9, b10)	Modulation format	FEC
(0, 0, 1)	1/1-TASK	BCH+SiPC
(1, 0, 1)	2/4-TASK	BCH with interleaving + SiPC
(0, 1, 1)	3/8-TASK	BCH with interleaving + SiPC
(1, 1, 1)	5/32-TASK	BCH with interleaving + SiPC
NOTE—"BCH + SiPC" indicates the concatenated code generated by BCH code as the outer code and the SiPC as the inner code. "BCH with interleaving + SiPC" indicates concatenated code generated by BCH with interleaving as the outer code and the SiPC as the inner code.		

31.2.1.2.4 HCS field

The PHY header shall be protected with a 4-bit HCS. The HCS shall be generated by taking one's complement of the remainder obtained from the modulo-2 division of bits b0–b11 of the PHY header by the following polynomial:

$$g(x) = 1 + x + x^4$$

The HCS field shall be generated by processing the bits b0–b11 in the transmit order. In the HCS field, the LSB of the HCS, b12, shall be transmitted first. This is illustrated in Figure 31-2. The registers shall be initialized to all ones.

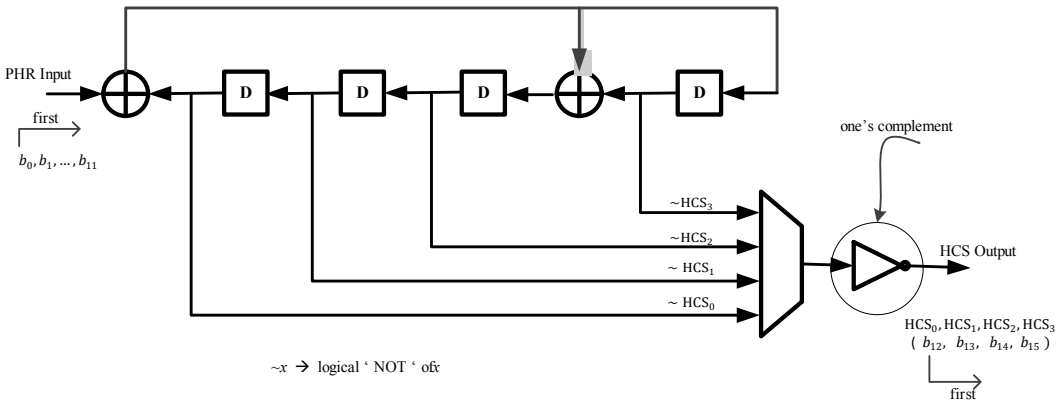

Figure 31-2—Generation of the HCS field

31.2.1.2.5 Spreading of PHR field

Similar to the spreading performed on the SFD field, bits in the PHR field are also mapped onto a ternary spreading code comprising two orthogonal ternary sequences. The bit-to-sequence mapping shall be as given in Table 31-4.

Table 31-4—Spreading of the PHR field

PHR bit	Bit-to-sequence mapping
0	[0 –1 0 1 1 0 –1 0]
1	[1 0 –1 0 0 –1 0 1]

31.2.1.3 PSDU field

A PSDU field carries the payload of a PPDU.

31.2.2 Generation of PPDU signal

For a given MCS, the PPDU signal shall be generated by the following procedure:

a) Construct the Preamble field (31.2.1.1.2), the SFD field (31.2.1.1.3), and the PHR field (31.2.1.2).
b) Apply the modulation format and FEC on the PSDU as determined by the MCS of the PHR field. Perform pseudo-random chip inversion on the resultant chips to obtain the DATA field. This process is described in 31.4.
c) Concatenate the Preamble field, the spread SFD field, the PHR field, and the DATA field, according to the order given in 31.2.1, to generate the PPDU.
d) Pass the resultant chip sequence of the PPDU through the modulation block as described in 31.5, followed by the Gaussian pulse shaping filter as described in 31.6.

The reference modulator diagram for generating a PPDU signal for TASK PHY is as depicted in Figure 31-3.

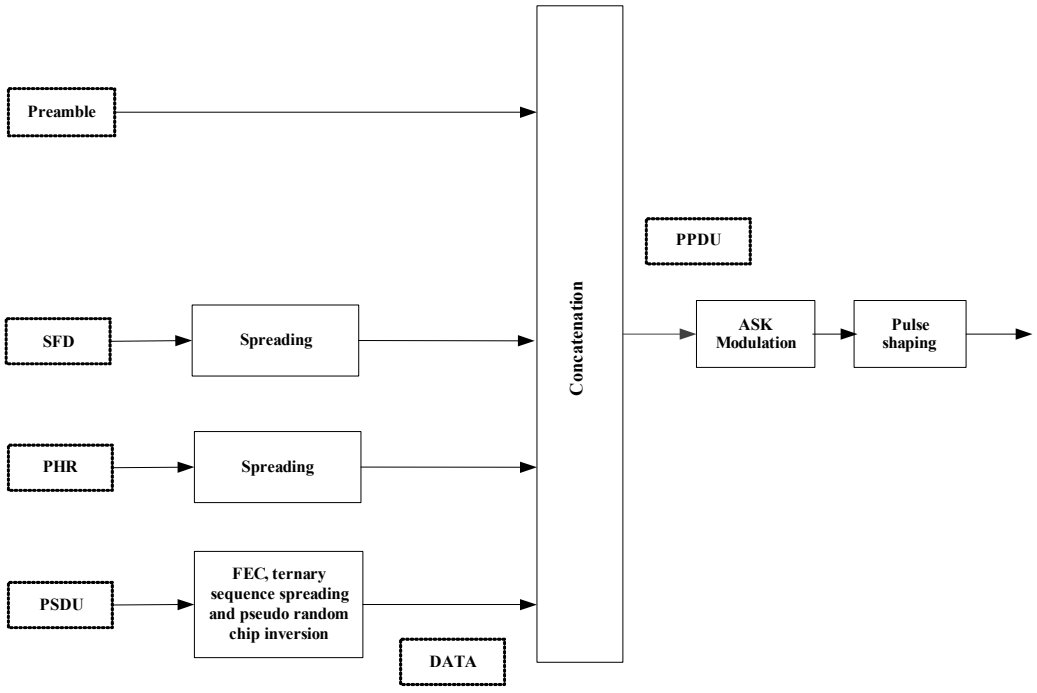

Figure 31-3—Reference modulator diagram—generation of PPDU signal

31.3 MCS mode, MCS, data rates, and related parameters

31.3.1 MCS mode

The MCS used for the PSDU in a frame is determined by the MAC in an implementation-dependent manner. The MCS mode specifies modulation and coding schemes to be applied on the PSDU. In any given frequency band of operation, eight MCS modes (0–7) are defined based on the data rates. The MCS mode and the corresponding data rates for different frequency bands are provided in Table 31-5, Table 31-6, and Table 31-7. The values presented in the data rate column of each of these tables correspond to the DataRate parameter as used in MCPS-DATA.request primitive as described in 8.3.1. Also, for each MCS, the parameters such as modulation order (*M*) and spreading sequence length (*L*) are given in these tables.

31.3.2 Data rates in the 2450 MHz band

The supported data rates and related parameters for 2450 MHz band are given in Table 31-5.

Table 31-5—PSDU modulation and coding formats and the supported data rates in 2450 MHz band

MCS mode	Modulation format	Coding format	Chip rate (Mchip/s)	*M* (Bits/data symbol)	*L* (Chips/ data symbol)	Code rate	Data rate (kb/s)
0	1/1-TASK	BCH	1	1	1	51/63	809.52
1	2/4-TASK	BCH with interleaving	1	2	4	51/63	404.76
2	3/8-TASK	BCH with interleaving	1	3	8	51/63	303.57
3	5/32-TASK	BCH with interleaving	1	5	32	51/63	126.48
4 (Optional)	1/1-TASK	BCH+SiPC	1	1	1	408/567	719.57
5 (Optional)	2/4-TASK	BCH with interleaving +SiPC	1	2	4	408/567	359.78
6 (Optional)	3/8-TASK	BCH with interleaving +SiPC	1	3	8	408/567	269.84
7 (Optional)	5/32-TASK	BCH with interleaving +SiPC	1	5	32	408/567	112.43

31.3.3 Data rates in the 780 MHz, 863 MHz, and 915 MHz bands

The supported data rates and related parameters are given in Table 31-6.

Table 31-6—PSDU modulation and coding formats and the supported data rates in 780 MHz, 863 MHz, and 915 MHz bands

MCS mode	Modulation format	Coding format	Chip rate (Mchip/s)	*M* (Bits/data symbol)	*L* (Chips/ data symbol)	Code rate	Data rate (kb/s)
0	1/1-TASK	BCH	0.6	1	1	51/63	485.71
1	2/4-TASK	BCH with interleaving	0.6	2	4	51/63	242.85
2	3/8-TASK	BCH with interleaving	0.6	3	8	51/63	182.14
3	5/32-TASK	BCH with interleaving	0.6	5	32	51/63	75.89
4 (Optional)	1/1-TASK	BCH+SiPC	0.6	1	1	408/567	431.74
5 (Optional)	2/4-TASK	BCH with interleaving +SiPC	0.6	2	4	408/567	215.87
6 (Optional)	3/8-TASK	BCH with interleaving +SiPC	0.6	3	8	408/567	161.90
7 (Optional)	5/32-TASK	BCH with interleaving +SiPC	0.6	5	32	408/567	67.46

31.3.4 Data rates in the 433 MHz and 470 MHz bands

Available data rates when operating in the 433 MHz and 470 MHz bands are shown in Table 31-7.

Table 31-7—PSDU modulation and coding formats and the supported data rates in 433 MHz and 470 MHz bands

MCS mode	Modulation format	Coding Format	Chip rate (Mchip/s)	*M* (Bits/data symbol)	*L* (Chips/ data symbol)	Code rate	Data rate (kb/s)
0	1/1-TASK	BCH	0.25	1	1	51/63	202.38
1	2/4-TASK	BCH with interleaving	0.25	2	4	51/63	101.19
2	3/8-TASK	BCH with interleaving	0.25	3	8	51/63	75.89

Table 31-7—PSDU modulation and coding formats and the supported data rates in 433 MHz and 470 MHz bands *(continued)*

MCS mode	Modulation format	Coding Format	Chip rate (Mchip/s)	*M* (Bits/data symbol)	*L* (Chips/ data symbol)	Code rate	Data rate (kb/s)
3	5/32-TASK	BCH with interleaving	0.25	5	32	51/63	31.62
4 (Optional)	1/1-TASK	BCH+SiPC	0.25	1	1	408/567	179.89
5 (Optional)	2/4-TASK	BCH with interleaving +SiPC	0.25	2	4	408/567	89.94
6 (Optional)	3/8-TASK	BCH with interleaving +SiPC	0.25	3	8	408/567	67.46
7 (Optional)	5/32-TASK	BCH with interleaving +SiPC	0.25	5	32	408/567	28.10

31.4 FEC, ternary sequence spreading, and pseudo-random chip inversion

Functional block diagrams in Figure 31-4 and Figure 31-5 provide a reference for specifying the TASK PHY modulation and coding functionalities for the PSDU. Two modes of operation are based on the FEC mechanisms:

— Mandatory mode: (MCS mode 0, 1, 2, or 3) BCH with interleaving shall be used for the FEC. The reference diagram for this mode is provided in Figure 31-4.

— Optional mode: (MCS mode 4, 5, 6, or 7) Concatenation of BCH with interleaving and SiPC shall be used for the FEC. The reference diagram for this mode is provided in Figure 31-5.

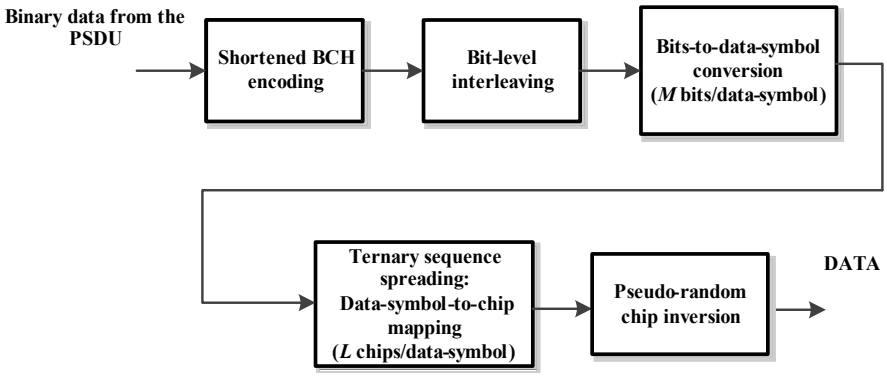

Figure 31-4—FEC, ternary sequence spreading, and pseudo-random chip inversion: mandatory mode

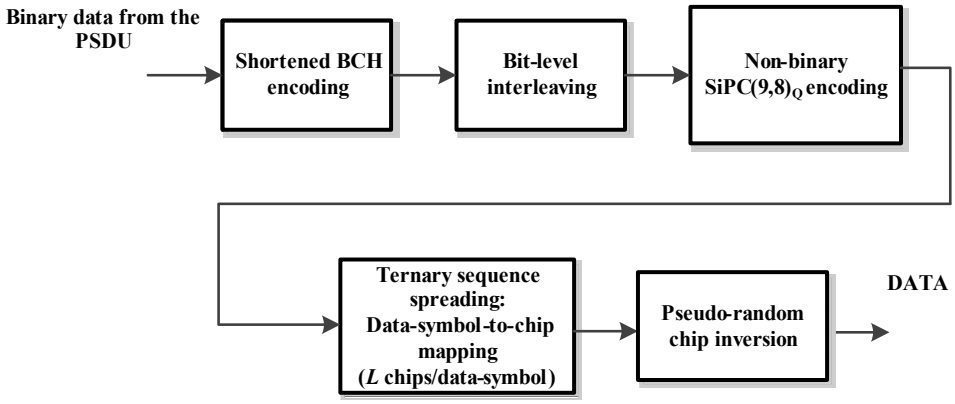

Figure 31-5—FEC, ternary sequence spreading, and pseudo-random chip inversion: optional mode

31.4.1 FEC codes

31.4.1.1 Shortened BCH codes with bit-level interleaving

31.4.1.1.1 Calculation of the BCH-related parameters

Parameters for shortened BCH (63, 51) encoding shall be calculated using the following procedure:

a) Compute the number of bits in the PSDU, N_{PSDU}:

$$N_{\text{PSDU}} = \text{Length} \times 8$$

b) Compute the total number of message blocks to be encoded, M_{B}:

$$M_{\text{B}} = \left\lceil \frac{N_{\text{PSDU}}}{51} \right\rceil$$

where $\lceil x \rceil$ denotes the smallest integer greater than or equal to x.

c) Compute the length of the shortened message block, K_{short}:

$$K_{\text{short}} = \left\lceil \frac{N_{\text{PSDU}}}{M_{\text{B}}} \right\rceil$$

d) Compute the shortening length of the code, l:

$$l = 51 - K_{\text{short}}$$

e) Compute the length of the shortened BCH code, N_{short}:

$$N_{\text{short}} = 63 - l$$

f) Compute the number of zero pad bits, Z, to be appended to the uncoded PSDU block:

$$Z = M_{\text{B}} K_{\text{short}} - N_{\text{PSDU}}$$

where it can be shown that $Z \leq M_{\text{B}}$.

g) Compute the length of the encoded PSDU, N_{coded}:

$$N_{coded} = M_B N_{short}$$

31.4.1.1.2 Zero padding

Zero pad bits are added to the uncoded PSDU to ensure uniformity in the length of message blocks before encoding, i.e., to create M_B message blocks of block length K_{short} bits. First, the uncoded PSDU of length N_{PSDU} bits should be packed as follows:

— Create Z message blocks of length $(K_{short} - 1)$ bits from the first $(K_{short} - 1)Z$ bits of the PSDU.
— Create $(M_B - Z)$ message blocks of length K_{short} bits, using the remaining $(M_B - Z)K_{short}$ bits.

The zero padding is performed by appending one zero bit at the end of each of the first Z message blocks.

31.4.1.1.3 BCH encoding

The generator polynomial for the BCH (63, 51) codes, with error correcting capability, $t = 2$, is as follows:

$$g(x) = 1 + x^3 + x^4 + x^5 + x^8 + x^{10} + x^{12}$$

Shortened BCH codes, denoted by BCH ($63 - l$, $51 - l$), can be obtained from the BCH (63, 51) code for any given shortening length, l, $1 \leq l < 51$.

For a given message block of length, K_{short}, the message polynomial is represented as follows:

$$m(x) = \sum_{i=0}^{K_{short}-1} m_i x^i$$

where $m_0, \ldots, m_{K_{short}-1}$ are the message bits and are the elements of GF(2).

For a given message polynomial, $m(x)$, the parity polynomial, $p(x)$, is computed as follows:

$$p(x) = \sum_{k=0}^{11} p_i x^i = \mathrm{mod}(x^{12} m(x), g(x))$$

where $p_0, \ldots, p_{11}$ are the parity bits.

The order of the message and parity bits shall be as follows:

— For the message bits, $m_{K_{short}-1}$ shall be the first bit to be transmitted in the message block, and m_0 shall be the last bit to be transmitted.
— For parity bits, p_{11} is the first parity bit to be transmitted, and p_0 is the last parity bit to be transmitted.

In generating the codeword, parity bits shall be appended to the right of the message block so that the message bits are transmitted first and then followed by the parity bits. This procedure is illustrated in Figure 31-6.

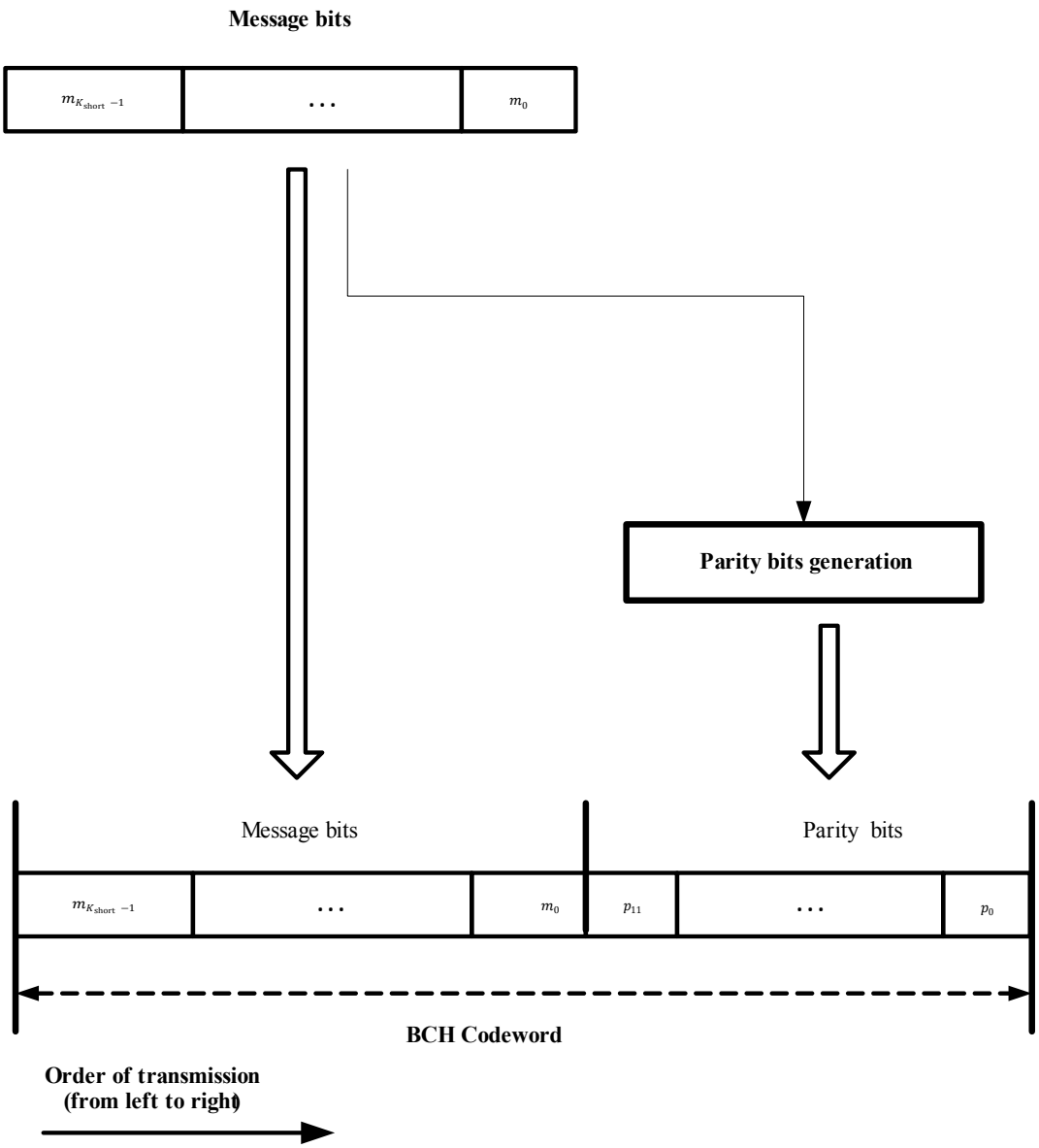

Figure 31-6—Generation of the BCH codeword for a given message block

31.4.1.1.4 Bit-level interleaving

Bit-level interleaving shall be used in conjunction with the shortened BCH codes to make encoded data resilient to bit errors in the event of data symbol errors. For a given codeword length N_{short} and an interleaving depth d, the following procedure is followed:

a) Collect d blocks of codewords.
b) Write them row-wise in a $d \times N_{\text{short}}$ dimensional array.
c) Read the array column-wise, and output the data sequentially.

The pictorial representation of the interleaving procedure is illustrated in Figure 31-7. Here, $b_{i,j}$ denotes the j-th transmitted bit of the i-th BCH codeword. That is, $b_{i,1}$ and $b_{i,N_{\text{short}}}$ denote $m_{K_{\text{short}}}$ and p_0 of the i-th BCH codeword, respectively.

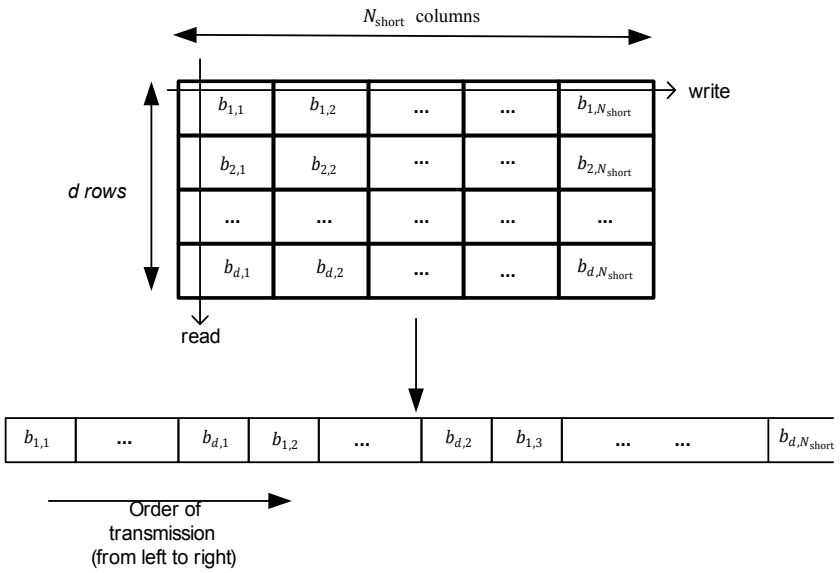

Figure 31-7—Depth–*d* interleaving for *d* codewords of length N_{short}

Parameters for bit-level interleaving shall be calculated using the following procedure:

a) For a given MCS, with a modulation order M, choose the initial interleaving depth, $d = M$.

b) Calculate the residual interleaving depth, d_{R}:

$$d_{\text{R}} = \text{mod}(M_{\text{B}}, d)$$

c) Calculate the number of interleaving blocks, N_{I}:

$$N_{\text{I}} = \frac{M_{\text{B}}}{d}$$

The bit-level interleaving for the encoded PSDU shall be performed by following the steps outlined in Table 31-8. The maximum interleaving depth, d_{max}, supported by the device shall be defined as $d_{\text{max}} = 5$.

Table 31-8—Interleaving depth vector and corresponding number of interleaving blocks

Condition			Interleaving depth vector
$d_{\text{R}} = 0$			Apply depth-d interleaving for N_{I} blocks.
$d_{\text{R}} \neq 0$	$M_{\text{B}} < d$		Apply depth-d_{R} interleaving for N_{I} blocks.
	$M_{\text{B}} > d$	$d + d_{\text{R}} \leq d_{\text{max}}$	Apply depth-d interleaving for $(N_{\text{I}} - 2)$ blocks and depth-$(d + d_{\text{R}})$ interleaving on the remaining $(d + d_{\text{R}})$ codewords for the $(N_{\text{I}} - 1)$-th and N_{I}-th blocks.
		$d + d_{\text{R}} > d_{\text{max}}$	Apply depth-d interleaving for $(N_{\text{I}} - 2)$ blocks, depth-$\lceil (d + d_{\text{R}})/2 \rceil$ interleaving for the $(N_{\text{I}} - 1)$-th block, and depth-$\lfloor (d + d_{\text{R}})/2 \rfloor$ interleaving for N_{I}-th block.

31.4.1.1.5 Bits-to-data-symbol conversion

Prior to the bits-to-data-symbol conversion, the encoded and interleaved PSDU data shall be padded with zeros to align the symbol boundary. The required number of zero padding bits, M_{zero}, shall be determined as follows:

$$M_{\text{zero}} = M\left\lceil \frac{N_{\text{coded}}}{M} \right\rceil - N_{\text{coded}}$$

where M is the modulation order (bits per data-symbol) of the given modulation format as given in Table 31-5, Table 31-6, and Table 31-7.

These M_{zero} bits are appended to the end of PSDU after BCH encoding and bit-level interleaving and then transmitted last.

The bits-to-data-symbol conversion shall be performed by converting the input bit stream into a sequence of M-tuples, where M-tuple is a block of M consecutive bits. The data symbols shall be generated by mapping each M-tuple to a unique element in the Q-ary alphabet $A = \{0, 1, 2, \ldots, Q-1\}$, where Q is the constellation size.

31.4.1.2 Single parity check (SiPC) codes

Nonbinary SiPC $(k+1, k)_Q$ code is defined as follows: SiPC $(k+1, k)_Q$ is a $(k+1)$-length block code over GF(Q), with single-symbol error correcting capability, consisting of k message symbols and one parity-check symbol. For MCS modes 4, 5, 6, and 7, FEC shall be the concatenation of BCH with interleaving as the outer code and SiPC (9, 8) code as the inner code. These modes are optional. SiPC (9, 8) encoding on the data-symbols shall be performed as described in 31.4.1.2.1.

31.4.1.2.1 SiPC encoding procedure

First, bits from the interleaving block are packed into a sequence of M-tuples. These M-tuples are then converted into message symbols by uniquely mapping them onto the elements of GF(Q). Then these message symbols are segregated into M_{B} message blocks, each consisting of 8 message symbols (over GF(Q)). SiPC encoder encodes each message block as follows:

a) Given message block of message symbols, $u_0, \ldots, u_7 \in \text{GF}(Q)$, the encoder generates the parity-check symbol, w:

$$w = \sum_{n=0}^{7} u_n$$

where the summation is taken over GF(Q).

b) The SiPC codeword is generated by appending the parity check symbol to the end of the message block.

Once the codewords are generated, the coded symbols, which are the elements of GF(Q), are converted into data symbols by uniquely mapping them onto the Q-ary alphabet $A = \{0, 1, 2, \ldots, Q-1\}$.

The order of transmission shall be such that the message symbols are transmitted first and then followed by the parity symbol. This transmission order is illustrated in Figure 31-8.

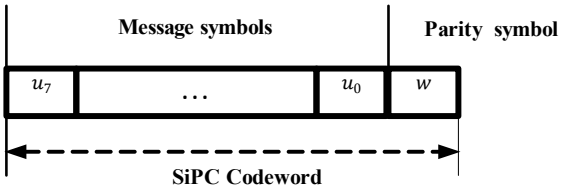

Figure 31-8—Generation of SiPC codeword for a given message block

31.4.2 Ternary sequence spreading: Data-symbol-to-chip conversion

Ternary sequence spreading is performed by a process of mapping each data symbol to a unique sequence of chips. The mapping is determined by the modulation format specified by the MCS field. The parameters for different modulation formats are given in 31.4. For a modulation format with the constellation size, Q, and the spreading sequence length, L, this stage maps data symbols from $A = \{0, 1, \ldots, Q-1\}$ to a set of L-length ternary sequences, C. Subclauses 31.4.2.1 through 31.4.2.4 outline the data-symbol-to-chip mapping for different modulation formats.

Chip transmission order is as follows: For an L-length chip-sequence, $\boldsymbol{c}_m = [c_m(0), \ldots, c_m(L-1)]$, $c_m(0)$ shall be transmitted first, and $c_m(L-1)$ shall be transmitted last.

31.4.2.1 1/1-TASK

The data-symbol-to-chip mapping for 1/1-TASK shall be performed as given in Table 31-9.

Table 31-9—Data-symbol-to-chip mapping for 1/1-TASK

1-tuple	Data symbol $m \in A$	Sequence $\boldsymbol{c}_m \in C$
0	0	0
1	1	1

31.4.2.2 2/4-TASK

The data-symbol-to-chip mapping for 2/4-TASK shall be performed as given in Table 31-10.

Table 31-10—Data-symbol-to-chip mapping for 2/4-TASK

2-tuple	Data symbol $m \in A$	Sequence $\boldsymbol{c}_m \in C$
00	0	[1 0 0 0]
10	1	[0 –1 0 0]
01	2	[0 0 0 1]
11	3	[0 0 –1 0]

31.4.2.3 3/8-TASK

The data-symbol-to-chip mapping for 3/8-TASK shall be performed as given in Table 31-11. The ternary sequences for mapping shall be obtained as follows:

$\boldsymbol{c}_0$ = [0 0 0 1 –1 0 1 1]

$\boldsymbol{c}_m$ = cyclic shifted $\boldsymbol{c}_0$ by m locations to the right, for m = 1, ... , 7

Table 31-11—Data-symbol-to-chip mapping for 3/8-TASK

3-tuple	Data symbol $m \in A$	Ternary sequence $\boldsymbol{c}_m \in C$
000	0	$\boldsymbol{c}_0$
100	1	$\boldsymbol{c}_1$
110	2	$\boldsymbol{c}_2$
010	3	$\boldsymbol{c}_3$
011	4	$\boldsymbol{c}_4$
111	5	$\boldsymbol{c}_5$
101	6	$\boldsymbol{c}_6$
001	7	$\boldsymbol{c}_7$

31.4.2.4 5/32-TASK

The data-symbol-to-chip mapping for 5/32-TASK shall be performed as given in Table 31-12. The ternary sequences for mapping shall be obtained as follows:

$\boldsymbol{c}_0$ = [–1 0 0 1 0 1 –1 0 –1 –1 1 –1 0 1 0 1 0 0 0 1 0 0 1 1 –1 0 0 0 0 0 1 1]

$\boldsymbol{c}_m$ = cyclic shifted $\boldsymbol{c}_0$ by m locations to the right, for m = 1, ... , 31

Table 31-12—Data symbol to chip mapping for 5/32-TASK

5-tuple	Data symbol $m \in A$	Ternary sequence $\boldsymbol{c}_m \in C$
00000	0	$\boldsymbol{c}_0$
10000	1	$\boldsymbol{c}_1$
11000	2	$\boldsymbol{c}_2$
01000	3	$\boldsymbol{c}_3$
01100	4	$\boldsymbol{c}_4$
11100	5	$\boldsymbol{c}_5$

Table 31-12—Data symbol to chip mapping for 5/32-TASK *(continued)*

5-tuple	Data symbol $m \in A$	Ternary sequence $\boldsymbol{c}_m \in C$
10100	6	$\boldsymbol{c}_6$
00100	7	c_7
00110	8	$\boldsymbol{c}_8$
10110	9	$\boldsymbol{c}_9$
11110	10	$\boldsymbol{c}_{10}$
01110	11	$\boldsymbol{c}_{11}$
01010	12	$\boldsymbol{c}_{12}$
11010	13	$\boldsymbol{c}_{13}$
10010	14	$\boldsymbol{c}_{14}$
00010	15	$\boldsymbol{c}_{15}$
00011	16	$\boldsymbol{c}_{16}$
10011	17	$\boldsymbol{c}_{17}$
11011	18	$\boldsymbol{c}_{18}$
01011	19	$\boldsymbol{c}_{19}$
01111	20	$\boldsymbol{c}_{20}$
11111	21	$\boldsymbol{c}_{21}$
10111	22	$\boldsymbol{c}_{22}$
00111	23	$\boldsymbol{c}_{23}$
00101	24	$\boldsymbol{c}_{24}$
10101	25	$\boldsymbol{c}_{25}$
11101	26	$\boldsymbol{c}_{26}$
01101	27	$\boldsymbol{c}_{27}$
01001	28	$\boldsymbol{c}_{28}$
11001	29	$\boldsymbol{c}_{29}$
10001	30	$\boldsymbol{c}_{30}$
00001	31	$\boldsymbol{c}_{31}$

31.4.3 Pseudo-random chip inversion

The pseudo-random chip inversion shall be performed only on the chips composing the Data field of the PSDU. The operation shall be clocked at the chip rate. This block consists of three main steps as illustrated in Figure 31-9.

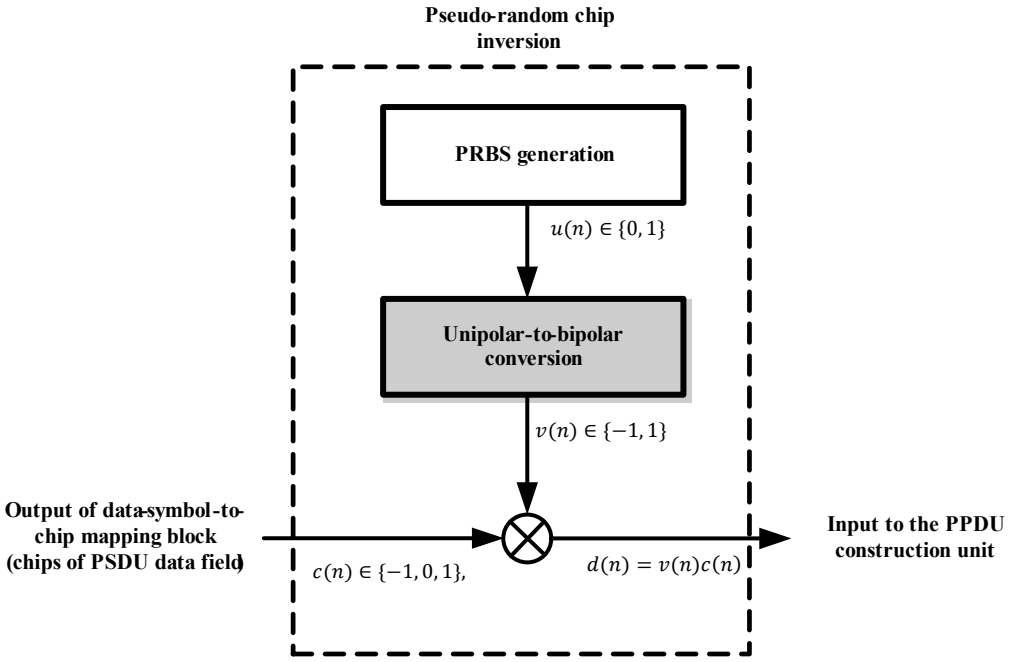

Figure 31-9—Schematic of the pseudo-random chip inversion stage

31.4.3.1 PRBS generation

The pseudo-random binary sequence generated by the PRBS generator shall be equivalent to the output of a 16-bit scrambler, with the generator polynomial (see 16.3.2).

$$G(x) = 1 + x^{14} + x^{15}$$

A reference shift register implementation of the PRBS generator is illustrated in Figure 31-10.

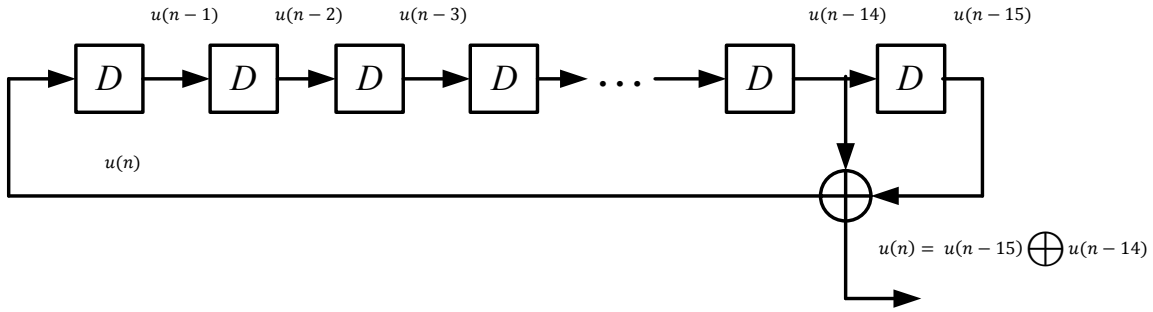

Figure 31-10—Linear feedback shift-register-based implementation of the PRBS generator

The PRBS output is generated recursively as follows:

$$u(n) = u(n-14) \oplus u(n-15), \qquad n = 0, 1, 2, \ldots$$

where $\oplus$ is the modulo-2 addition operator.

The initialization vector of the PRBS is denoted as follows:

$\boldsymbol{u}_{\text{init}} = [u(-15), u(-14), \ldots, u(-1)]$

The PRBS generator shall be initialized with the following vector:

$\boldsymbol{u}_{\text{init}} = [1\ 1\ 1\ 0\ 0\ 0\ 1\ 0\ 1\ 1\ 0\ 1\ 1\ 0\ 1]$

31.4.3.2 Unipolar-to-bipolar conversion

The output of the PRBS generator $u(n)$, which is a unipolar binary sequence, shall be converted to bipolar binary sequence, $v(n)$, through the following operation:

$$v(n) = 2u(n) - 1$$

where

$$v(n) = \begin{cases} 1 & \text{if } u(n) = 1 \\ -1 & \text{if } u(n) = 0 \end{cases}$$

31.4.3.3 Chip inversion

The polarities of the chips shall be inverted as follows:

$$d(n) = v(n)c(n), \quad c(n) \in \{-1, 0, 1\}, \quad n = 0, 1, 2, \ldots$$

where $\{c(n), n = 0, 1, 2, \ldots\}$ is the chip sequence.

At the coherent receiver, to recover the polarity of chips, the PRBS generator shall be initialized with the same initialization vector. On the other hand, the noncoherent receiver does not need to be equipped with the PRBS generator.

31.5 Modulation

The sequence of chips composing the PPDU is modulated using ASK with binary phase shifts. Specifically, the modulation is performed by the following mapping:

$$A_n = \begin{cases} +A & \text{when } d(n) = +1 \\ 0 & \text{when } d(n) = 0 \\ -A & \text{when } d(n) = -1 \end{cases}$$

where

$\{d(n)\}$ is the chip sequence of the PPDU
A_n is the amplitude of the n-th chip
A is the transmit voltage level

The ASK modulation is followed by Gaussian pulse shaping. The chips are generated at the rate of 1 Mchip/s for 2450 MHz band; 600 kchip/s for 780 MHz, 863 MHz, and 915 MHz bands; and 250 kchip/s for 433 MHz and 470 MHz bands.

31.6 Pulse shaping

The modulated signal shall be filtered to meet the transmit PSD masks, as defined in 31.8.1, and the EVM, as defined in 31.8.6. Each baseband chip is represented by a Gaussian pulse, with a bandwidth-time product of $BT_{\text{chip}} = 0.3\sim0.5$, where T_{chip} is the chip duration (T_{chip} = 1/chip rate). The impulse response of the filter is given as follows:

$$g(t) = B\sqrt{\frac{2\pi}{ln(2)}}e^{-\left(\frac{2\pi^2 B^2 t^2}{ln(2)}\right)}$$

31.7 Representation of the modulated waveforms

The modulated PPDU signal is represented as follows:

$$x_{\text{PB}}(t) = \left[A\sum_{n=1}^{N_{\text{PPDU}}} d(n)g(t - nT_{\text{chip}})\right]\cos(\omega_c t + \phi)$$

where

$d(n) \in \{-1, 0, 1\}$	are the chips of the PPDU
T_{chip}	is the chip duration
N_{PPDU}	is the number of chips in the processed PPDU
$g(t)$	is the output of the pulse shaping described in 31.6
ω_c	is the angular frequency of the carrier
$\phi \in [0, 2\pi]$	is the random phase

31.8 RF requirements

31.8.1 Transmit PSD mask

When operating in the 2450 MHz band, transmit spectral components shall conform to the limits specified in Table 31-13, when measured using a 100 kHz resolution bandwidth.

Table 31-13—Transmit PSD limits in 2450 MHz band

Frequency range	Relative limit	Absolute limit
$\lvert f - f_c \rvert > 3.5$ MHz	–20 dB	–30 dBm

For the relative limit, the reference level shall be the highest average spectral power measured within ± 1 Hz of the carrier frequency.

When operating in 780 MHz, 863 MHz, and 915 MHz bands, transmit spectral components shall conform to the limits specified in Table 31-14, measured using a 100 kHz resolution bandwidth.

Table 31-14—Transmit PSD limits in 780 MHz, 863 MHz, and 915 MHz bands

Frequency range	Relative limit	Absolute limit
$\lvert f - f_c \rvert > 1.2$ MHz	–20 dB	–20 dBm

For the relative limit, the reference level shall be the highest average spectral power measured within ± 600 kHz of the carrier frequency.

When operating in 433 MHz and 470 MHz bands, transmit spectral components shall conform to the limits specified in Table 31-15, measured using a 100 kHz resolution bandwidth.

Table 31-15—Transmit PSD limits in 433 MHz and 470 MHz bands

Frequency range	Relative limit	Absolute limit
$\lvert f - f_c \rvert > 1.25$ MHz	–20 dB	–20 dBm

For the relative limit, the reference level shall be the highest average spectral power measured within ± 600 kHz of the carrier frequency.

31.8.2 Receiver sensitivity

Under the conditions specified in 10.1.7, a compliant device shall be capable of achieving a receiver sensitivity of –85 dBm or better for the modulation format corresponding to the lowest data rate in the given operating band.

31.8.3 Interference rejection capability

The receiver interference rejection capability of TASK PHY shall be measured as described in 12.3.5. The values for adjacent channel rejection capability and alternate channel rejection capability shall conform to the limits specified in Table 31-16.

Table 31-16—Receiver interference rejection requirements in all the operating bands

Adjacent channel rejection	Alternate channel rejection
0 dB	20 dB

The adjacent channel rejection shall be measured as follows: The desired signal shall be a compliant TASK PHY signal that consists of pseudo-random bits, modulated by any one of the modulation formats defined in Table 31-9, Table 31-10, Table 31-11, and Table 31-12. Either in the adjacent channel or in the alternate channel, the interfering signal shall be generated by a compliant TASK PHY signal employing the same modulation format as that of the desired signal.

The desired signal is input to the receiver at a level of 3 dB greater than the maximum allowed receiver sensitivity specified in 31.8.2. The interfering signal is generated at a level as specified in Table 31-16 relative to the desired signal power. The test shall be performed for only one interfering signal at a time.

The receiver shall meet the PER criterion of 1% at 20 octets of PSDU.

31.8.4 TX-to-RX turnaround time

The TASK PHY shall have a TX-to-RX turnaround time as defined in 10.2.1.

31.8.5 RX-to-TX turnaround time

The TASK PHY shall have a RX-to-TX turnaround time as defined in 10.2.2.

31.8.6 EVM

EVM shall be measured as described in 10.2.3. The TASK PHY shall have EVM values of less than 35%.

31.8.7 Transmit power

The TASK PHY compliant transmitter shall be able to transmit at a power level of at least –13 dBm.

31.8.8 Transmit center frequency tolerance

The TASK PHY transmit center frequency tolerance shall be $\pm 40 \times 10^{-6}$ maximum.

31.8.9 Receiver maximum input level of desired signal

The receiver maximum input level is the maximum power level of the desired signal present at the input of receiver for which the error criterion of 1% PER at 20 octets of PSDU is met. The TASK PHY shall have a receiver maximum input level greater than or equal to –20 dBm.

31.8.10 Receiver ED

The TASK PHY shall provide the ED measurement as described in 10.2.5. The ED measurement time, to average over, shall be equal to 128 chip durations.

31.8.11 SNR measurement

The minimum and maximum SNR values (0x00 and 0xff) should be associated with the lowest and highest quality compliant signals detectable by the receivers, respectively. SNR values in between should be uniformly distributed between these two limits.

31.8.12 CCA

The TASK PHY shall use one of CCA mode 1, CCA mode 2, or CCA mode 3, as described in 10.2.7.

32. RS-GFSK PHY

32.1 PPDU format

The SHR, PHR, and PHY payload components are treated as bit strings of length *n*, numbered b0 on the left and b(n – 1) on the right. When transmitted, they are processed b0 first to b(n – 1) last, regardless of their content or structure.

The RS-GFSK PPDU shall be formatted as illustrated in Figure 12-1 for transmissions using the SFD for uncoded or the SFD for FEC coded, as described in 32.1.2.

32.1.1 Preamble field

The Preamble field shall contain *phyRsGfskPreambleLength* (as defined in 11.3) multiples of the 8-bit sequence “01010101”.

32.1.2 SFD

The SFD shall be selected from the list of values shown in Table 32-1. Devices that do not support any FEC shall support the SFD associated with uncoded (PHR + PSDU). Devices that support the convolutional FEC shall support the SFD for FEC coded (PHR + PSDU) in addition to the SFD for uncoded (PHR + PSDU). If interoperation with SUN FSK PHY is desired, a value of zero for the PIB attribute *phyRsGfskSfd* may be used. If interoperation with SUN FSK PHY is not desired, a value of one for the PIB attribute *phyRsGfskSfd* may be used.

Table 32-1—RS-GFSK PHY SFD values for 2-GFSK

	SFD for coded (b0–b15)	SFD for uncoded (b0–b15)
phyRsGfskSfd = 0	0110 1111 0100 1110	1001 0000 0100 1110
phyRsGfskSfd = 1	0011 0101 1100 0110	1001 1010 1111 0000

NOTE—When transmission is in MCS modes 5, 6, and 7 with differential encoding described in 32.2.2, the expected pattern for the SFD on the receiver side will differ from the values shown in Table 32-1.

32.1.3 Long PHR

All RS-GFSK devices shall support the long PHR. The format of the long PHR is shown in Figure 32-1.

Bits: 0	1	2	3	4	5–15
Reserved	Rate Switch	Short PHR	FCS Type	Data Whitening	Frame Length

Figure 32-1—Format of the long PHR for RS-GFSK

Bit 0 is reserved.

The Rate Switch field indicates if rate switch is enabled or disabled. The Rate Switch field shall be set to one when rate switch is enabled and shall be set to zero otherwise. The rate switch mode is described in 32.3. The rate switch shall be disabled when FEC is used.

The Short PHR field shall be set to zero to indicate the use of the long PHR.

The FCS Type field indicates the length of the FCS field described in 7.2.10 that is included in the MPDU. The transmitted FCS Type field shall be set to zero for a 4-octet FCS and shall be set to 1 for a 2-octet FCS. When FEC is being used, the transmitted FCS Type field shall be set to zero, and a 4-octet FCS shall be used.

The Data Whitening field indicates whether data whitening is used during transmission. An RS-GFSK device shall have data whitening enabled for all frame transmissions with the Data Whitening field in the PHR set to one.

NOTE—This requirement allows for compatibility with the SUN FSK PHY.

The Frame Length field is an unsigned integer that shall be set to the total number of octets contained in the PSDU (prior to FEC encoding, if enabled). The Frame Length field shall be transmitted MSB first.

32.1.4 Short PHR

Support for the Short PHR is optional. The format of the short PHR is shown in Figure 32-2.

Bits: 0	1	2	3–7
Reserved	Rate Switch	Short PHR	Frame Length

Figure 32-2—Format of the short PHR for RS-GFSK

Bit 0 is reserved.

The Rate Switch field indicates if rate switch is enabled or disabled. The Rate Switch field shall be set to one when rate switch is enabled and shall be set to zero otherwise. The rate switch mode is described in 32.3.

The Short PHR field shall be set to one to indicate the use of the short PHR. The short PHR format shall not be used when FEC is used.

When the short PHR is used, the length of the FCS field described in 7.2.10 shall be 2 octets.

The Frame Length field is an unsigned integer that shall be set to the total number of octets contained in the PSDU. The Frame Length field shall be transmitted MSB first.

The short PHR may be enabled from a higher layer using the PHY PIB attribute *phyRsGfskShortPhrEnabled*. When this attribute is TRUE, the PSDU length shall be 31 octets or less, and FEC shall be disabled.

NOTE—When the short PHR is used, the maximum PSDU size is limited to 31 octets.

32.2 Modulation and coding

The modulation for the RS-GFSK is either a 2-level or a 4-level GFSK with a BT value of 0.5.

The symbol rate and the outer deviation shall be the same across the entire PPDU. When the Rate Switch bit is set to zero, the entire PPDU shall be transmitted using 2-GFSK modulation, i.e., one of the operating modes in Table 32-2. In addition, when the Rate Switch bit is set to zero, the outer deviation shall be determined by the multiplication of the modulation index, as specified in Table 32-2, by half the symbol rate.

Table 32-2—RS-GFSK 2-GFSK MCS

RS-GFSK MCS mode	Data rate (kb/s)	Symbol rate (kb/s)	Channel spacing (kHz)	Modulation index
0	4.8	4.8	12.5	0.76
1	9.6	9.6	25	0.76
2	50	50	200	0.76
3	150	150	400	0.76
4	500	500	1000	0.76
5	250	250	500	0.5
6	500	500	1000	0.5
7	1000	1000	2000	0.5

When the Rate Switch bit is set to one, the SHR and PHR shall be transmitted in 2-GFSK, and the PSDU shall be transmitted in 4-GFSK, i.e., one of the operating modes in Table 32-3. In addition, when the Rate Switch bit is set to one, the outer deviation across the entire PPDU shall be equal to the modulation index, as specified in Table 32-3, multiplied by 1.5 times the symbol rate. In 2-GFSK mode, the symbol rate is equal to the data rate. In 4-GFSK mode, the symbol rate is equal to the data rate divided by 2.

Table 32-3—RS-GFSK 4-GFSK MCS

RS-GFSK operating mode	Data rate (kb/s)	Symbol rate (kb/s)	Channel spacing (kHz)	Modulation index
0a	9.6	4.8	12.5	0.3
1a	19.2	9.6	25	0.3
2a	100	50	200	0.3
3a	300	150	400	0.3
4a	1000	500	1000	0.3

Table 32-2 shows the primary modulation and channel parameters for the RS-GFSK PHY MCSs. The values presented in RS-GFSK MCS mode column correspond to the DataRate as used in MCPS-DATA primitive as described in 8.3.1. When FEC is enabled, the effective data rate is half of the value that is shown in Table 32-2, due to the rate 1/2 convolutional coding as described in 32.2.7.

Table 32-3 shows the rate switch modulation and channel parameters, which are used in rate switch mode for transmitting the PSDU. The symbol period is defined as the reciprocal value of the symbol rate. If MCS levels with different symbol periods are employed for uplink and downlink, all calculations depending on symbol period shall use the longer symbol period.

32.2.1 Reference modulator diagram

The functional block diagram in Figure 32-3 is provided as a reference for specifying the RS-GFSK PHY data flow processing functions. Each bit shall be processed using the bit order rules defined in 32.1.

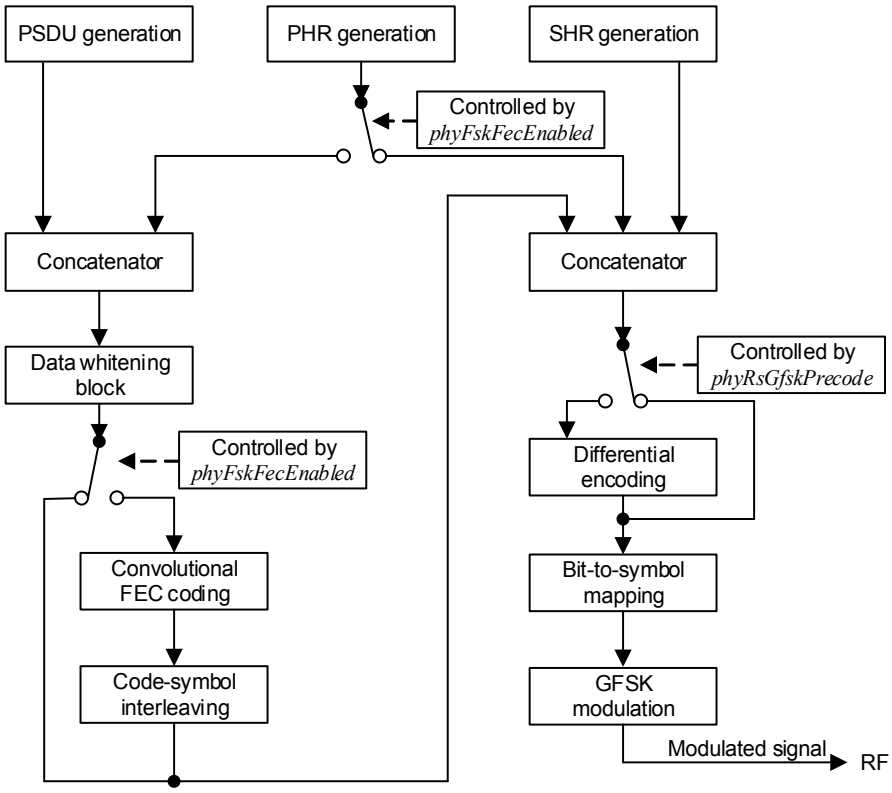

Figure 32-3—RS-GFSK reference modulator diagram

When FEC is enabled, the PHR and PSDU shall be processed for coding, as described in 32.2.7. Differential encoding shall be applied to PHR and PSDU as described in 32.2.2 when MCS mode 5, 6, or 7 is used.

When FEC is not used, data whitening shall be applied over the PSDU, as described in 32.2.9. When FEC is used, data whitening shall be applied over the PHR and the PSDU.

When differential encoding is enabled, the PPDU shall be processed as described in 32.2.2.

32.2.2 Differential encoding

Differential encoding shall be applied for MCS modes 5, 6, and 7 when *phyFskFecEnabled* is TRUE and shall be disabled otherwise.

The procedure of differential encoding shall be employed as described in 13.2.3.

32.2.3 Bit-to-symbol mapping

Bit-to-symbol mapping shall be applied as described in 20.3.2.

32.2.4 Modulation quality

Modulation quality shall be measured by observing the frequency deviation tolerance and the zero crossing tolerance of the eye diagram caused by a PN9 sequence of length 511 bits.

32.2.5 Frequency deviation tolerance

The frequency deviation tolerance for 2-GFSK shall be as given in 20.3.3.1. The frequency deviation tolerance for 4-GFSK shall be as given in Figure 32-4.

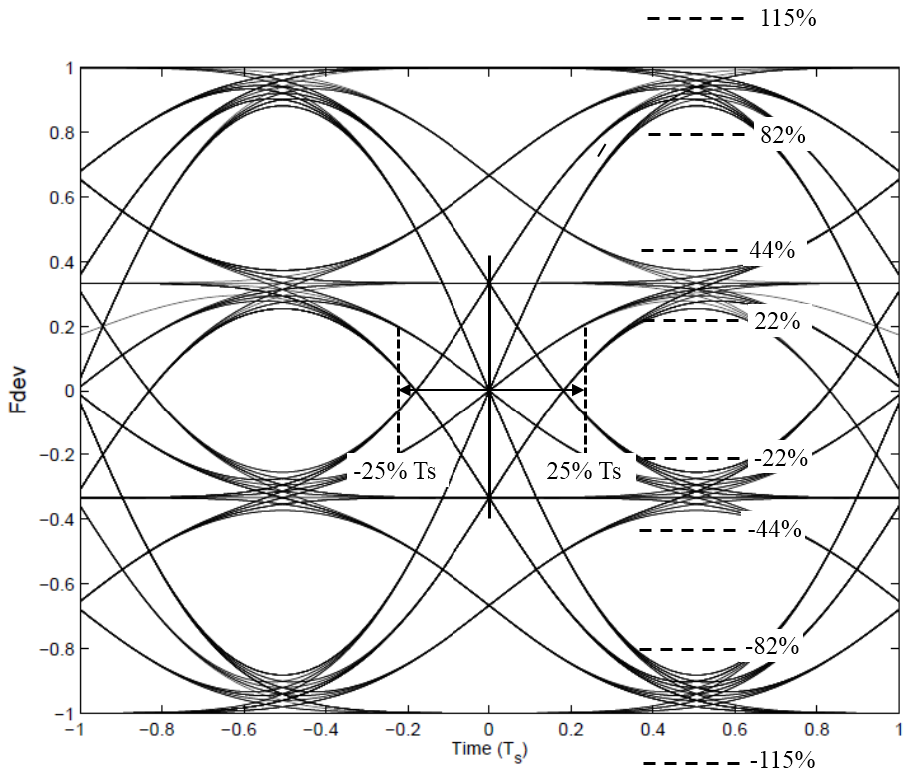

Figure 32-4—Eye diagram of 4GFSK modulation

F_{dev} is the normalized frequency deviation.

$$F_{dev} = \frac{2F(t)}{3h \times R_s}$$

where

$F(t)$ is the measured frequency
h is the modulation index
R_S is the symbol rate as defined in Table 32-3

The outer deviation equals where F_{dev} is one. The frequency $F(t)$ shall be measured in a bandwidth equal to twice the symbol rate centered around the transmit carrier frequency.

The symbol timing accuracy shall be the same or better than the radio frequency tolerance as specified in 32.4.1.

32.2.6 Zero crossing tolerance

The zero crossing tolerance for 2-GFSK shall be as given in 20.3.3.2. The frequency crossing tolerance for 4-GFSK shall be set as in Figure 32-4.

32.2.7 FEC

FEC is optional. If *phyFskFecEnabled* indicates the usage of convolutional FEC code, it shall be applied as described in 24.3.4 with the following changes:

Prior to the convolutional encoding of the PHR and PSDU bits, the initial encoder state at $k = 0$ shall be set as follows:

$$(u_{-1}, u_{-2}, \ldots, u_{-6}) = (0, 0, 0, 0, 0, 0)$$

The pad bits shall be set to zero; and the number of pad bits, N_{PAD}, is computed from the number of blocks, N_{B}, and the total number of uncoded bits, N_{D}, as follows:

$$N_{\mathrm{B}} = \mathrm{ceiling}((8 \times \mathrm{LENGTH} + 6) / 16)$$

$$N_{\mathrm{D}} = N_{\mathrm{B}} \times 16$$

$$N_{\mathrm{PAD}} = N_{\mathrm{D}} - (8 \times \mathrm{LENGTH} + 6)$$

Instead of using the sequence shown in Figure 24-6, the sequence shown in Figure 32-5 shall be passed to the convolutional encoder.

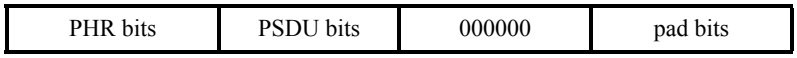

Figure 32-5—PSDU extension prior to encoding

32.2.8 Code-symbol interleaving

When FEC is used, interleaving of code-bits shall be employed, as described in 20.3.5. No interleaving shall be employed if FEC is not enabled.

32.2.9 Data whitening for RS-GFSK

Data whitening is mandatory for all frame transmissions.

The procedure of data whitening shall be employed as described in 17.2.3.

32.3 Rate switch RS-GFSK

The Rate Switch field in the PHR shall be set to one when rate switch is enabled and shall be set to zero otherwise. Enabling rate switch is optional. When rate switch is enabled, the SHR and the PHR shall be transmitted using any 2-GFSK MCS with modulation index 0.9, and the PSDU shall be transmitted using the same symbol rate as used during the SHR and PHR, but employing a 4-GFSK operation mode with modulation index 0.3. When rate switch is disabled, a single MCS is used during the transmission of the PPDU. The capability of receiving and transmitting frames with rate switch enabled may be communicated by setting the Rate Switch field in the RS-GFSK Device Capabilities IE to one. Then, the device shall be responsive to both states of the received Rate Switch bit in the PHR. Also, the device shall be capable of transmitting frames with rate switch enabled and disabled.

32.4 RF requirements

32.4.1 RF tolerance

The single-sided clock frequency tolerance T at the transmitter, in 10^{-6}, shall be as follows:

$$T \leq \min\left(\frac{T_0 \times R \times h \times F_0}{R_0 \times h_0 \times F}, 30\right)$$

for all combinations of R, h, and F and for each mode supported by the device, where

R is the symbol rate, in ksymbol/s
h is the modulation index used for the 2GFSK part of the frame
F is the carrier frequency, in MHz
R_0 is 50 ksymbol/s
h_0 is 0.76
F_0 is 915 MHz
T_0 is 20×10^{-6} for modes in all bands, except at 2450 MHz for which the value of T_0 is 40×10^{-6}

32.4.2 Channel switch time

Channel switch time shall be less than or equal to 500 μs. The channel switch time is defined as the time elapsed at the antenna between the trailing edge of the last symbol of one PPDU to the leading edge of the first symbol of a consecutive PPDU sent on a different channel.

32.4.3 Receiver sensitivity

Under the conditions specified in 10.1.7, the RS-GFSK receiver sensitivity shall be better than S, where S is defined, in dBm, as follows:

$$S = \min\left(S_0 + 10 \log_{10}\left(\frac{R}{R_0}\right), -85\right)$$

where

S_0 is taken from Table 32-4
R_0 is 50 kb/s
R is the bit rate, in kb/s

Table 32-4—S_0 values for receiver sensitivity

	Uncoded	FEC
Without differential encoding	–91	–99
With differential encoding	N/A	–102

32.4.4 Receiver interference rejection

The receiver interference rejection shall be measured as described in 20.6.8.

32.4.5 TX-to-RX turnaround time

The RS-GFSK PHY shall have a TX-to-RX turnaround time as defined in 10.2.1.

32.4.6 RX-to-TX turnaround time

The RS-GFSK PHY shall have a RX-to-TX turnaround time as defined in 10.2.2.

32.4.7 Receiver maximum input level of desired signal

The RS-GFSK PHY shall have a receiver maximum input level greater than or equal to –20 dBm using the measurement defined in 10.2.4.

32.4.8 Receiver ED

The RS-GFSK PHY shall provide the receiver ED measurement as described in 10.2.5.

32.4.9 LQI

The RS-GFSK PHY shall provide the LQI measurement as described in 10.2.6.

32.4.10 CCA

The RS-GFSK PHY shall use one of CCA mode 1, CCA mode 2, CCA mode 3, or CCA mode 4, as described in 10.2.7.

Annex A

(informative)

Bibliography

Insert the following references into Annex A in alphanumeric order:

[B5a] de Ruijter, H., IEEE 802.15 document 15-15-0290-01-004q, 2015.

[B9b] Nair, J. P., C. Thejaswi, K. Bynam, and H. de Ruijter, IEEE 802.15 document 15-14-0709-00-004q, 2014.[3]

[B18] Thejaswi, C., K. Bynam, and J. P. Nair, IEEE 802.15 document 15-15-0120-00-004q, 2015.

[3] IEEE 802.15 documents are available at https://mentor.ieee.org/802.15/documents.

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