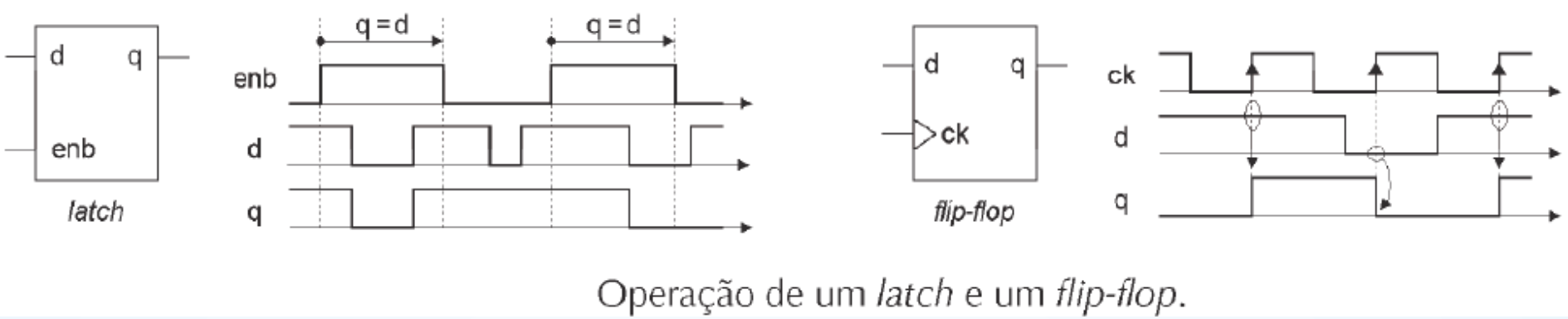
Aula 9 – Circuitos Síncronos

Tópicos da aula

- **Latch e Flip-flops**
- **Condições para transição e Inicialização**
- **Registradores**
- **Máquinas de estado**

LATCH e FLIP-FLOP

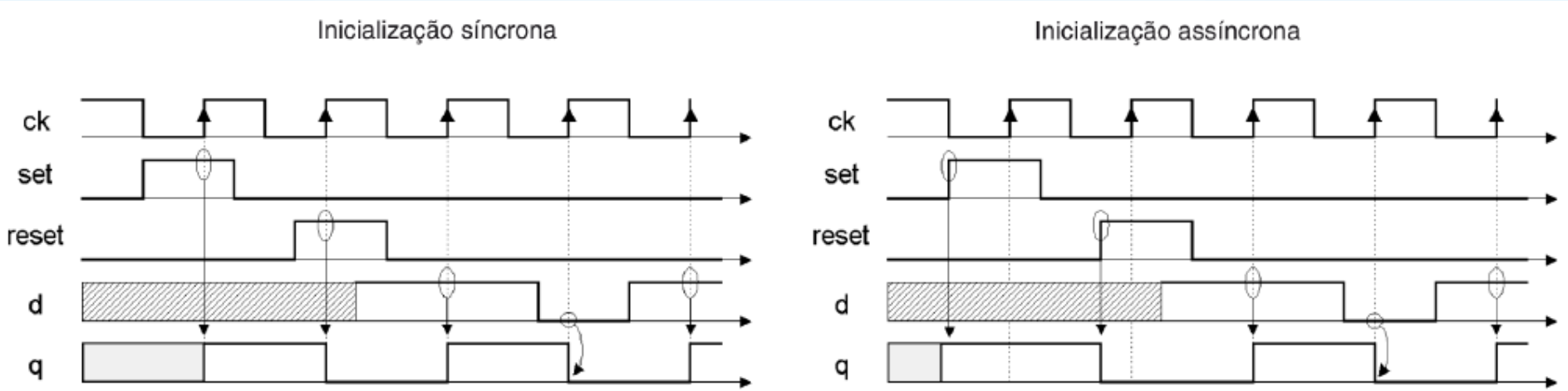


Operação de um *latch* e um *flip-flop*.

Ocorrência de bordas (subida / descida) em sinais

```
rising_edge (clock)                 -- Borda de subida.
(clock EVENT AND clock = '1')       -- Borda de subida.
falling_edge (clock)                -- Borda de descida.
(clock EVENT AND clock = '0')       -- Borda de descida.
```

Inicialização (reset)



Exemplos de operações de inicialização em *flip-flops*.

Exercícios

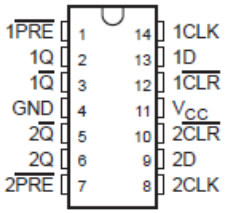
- **Implemente um Flip-flop tipo D com reset síncrono**
- **Implemente um Flip-flop tipo D com reset assíncrono**

Exercícios

74AC11074
DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH CLEAR AND PRESET
SCAS499A – DECEMBER 1986 – REVISED APRIL 1996

- Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise
- *EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic Small-Outline (D) and Thin Shrink Small-Outline (PW) Packages, and Standard Plastic 300-mil DIPs (N)

D, N, OR PW PACKAGE
(TOP VIEW)



description

This device contains two independent positive-edge-triggered D-type flip-flops. A low level at the preset ($\overline{PRE}$) or clear ($\overline{CLR}$) input sets or resets the outputs regardless of the levels of the other inputs. When $\overline{PRE}$ and $\overline{CLR}$ are inactive (high), data at the data (D) input that meets the setup-time requirements are transferred to the outputs on the low-to-high transition of the clock (CLK) pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input may be changed without affecting the levels at the outputs.

The 74AC11074 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

INPUTS				OUTPUT	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H†	H†
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

† This configuration is nonstable; that is, it does not persist when $\overline{PRE}$ or $\overline{CLR}$ returns to its inactive (high) level.

Registradores

- **Podem ser entendidos como uma sequência de flip-flops tipo D em paralelo**
- **Importantes como forma de memorização de dados**

Exercícios

- **Implemente um registrador com carregamento (LOAD) assíncrono**
- **Implemente um registrador com carregamento (LOAD) síncrono**

Máquinas de Estados

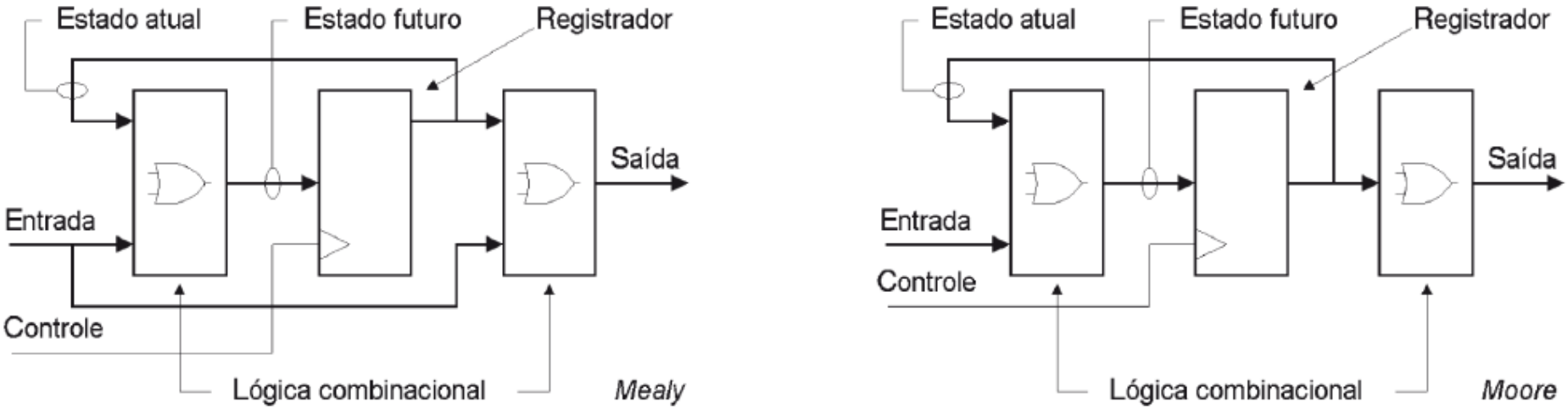
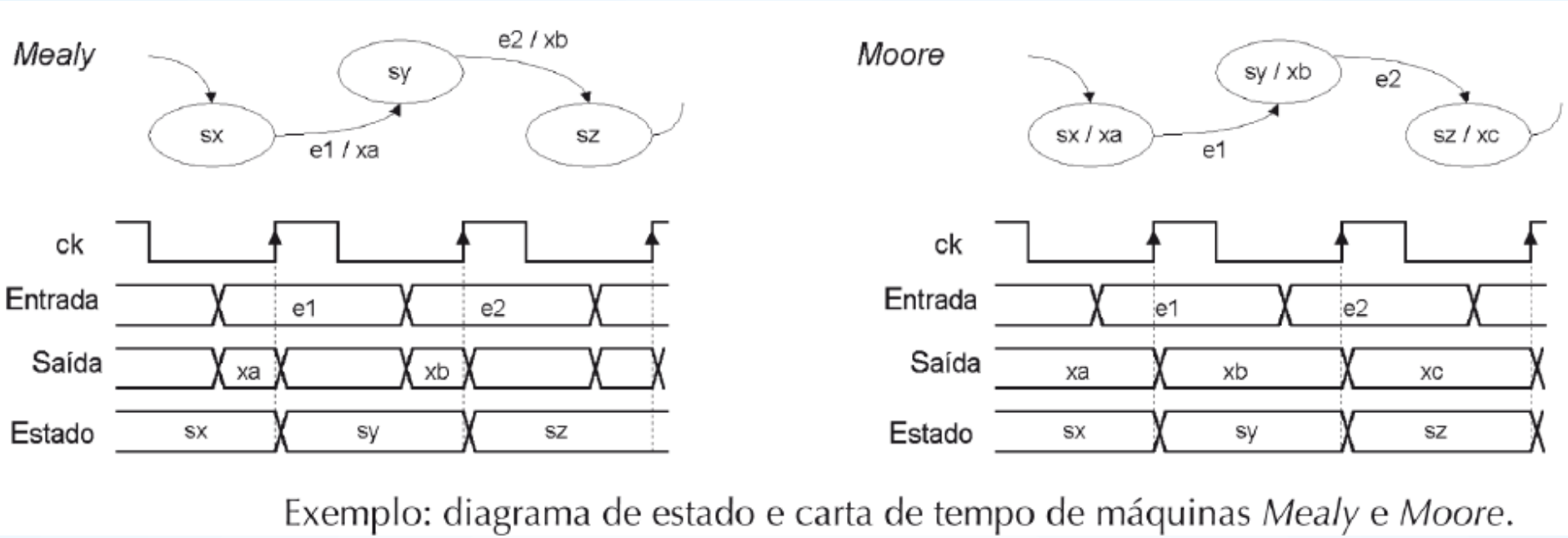


Diagrama de blocos de máquinas de estados.

Máquinas de Estados



Exemplo: diagrama de estado e carta de tempo de máquinas *Mealy* e *Moore*.

```
75      U_MACHINE : process(i_CLK, i_RST)
76      begin
77          if (i_RST = '1') then
78              w_EN        <= '0';
79              w_CLR_BUSY  <= '1';
80              w_STATE     <= st_IDLE;
81
82          elsif rising_edge (i_CLK) then
83              case w_STATE is
84                  when st_IDLE =>
85                      w_CLR_BUSY  <= '0';
86
87                      if (i_REQ = '1') then
88                          w_EN     <= '1';
89                          w_STATE  <= st_UPDATE;
90                      else
91                          w_STATE  <= st_IDLE;
92                      end if;
93                  when st_UPDATE =>
94                      w_EN  <= '0';
95                      if (w_BUSY = '1') then
96                          w_CLR_BUSY  <= '1';
97                          w_STATE <= st_IDLE;
98                      else
99                          w_STATE <= st_UPDATE;
100                     end if;
101                 when others =>
102                     w_STATE <= st_IDLE;
103             end case;
104         end if;
105     end process U_MACHINE;
```

Exercícios

- **Implemente uma máquina de estados que opere como cronômetro e apresente as seguintes funcionalidades: (1) START, (2) STOP, (3) RESTART**

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