



Write-Optimized Dynamic Hashing for Persistent Memory

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Outline

Background

- Static Hashing
- Extendible Hashing
- Persistent Memory

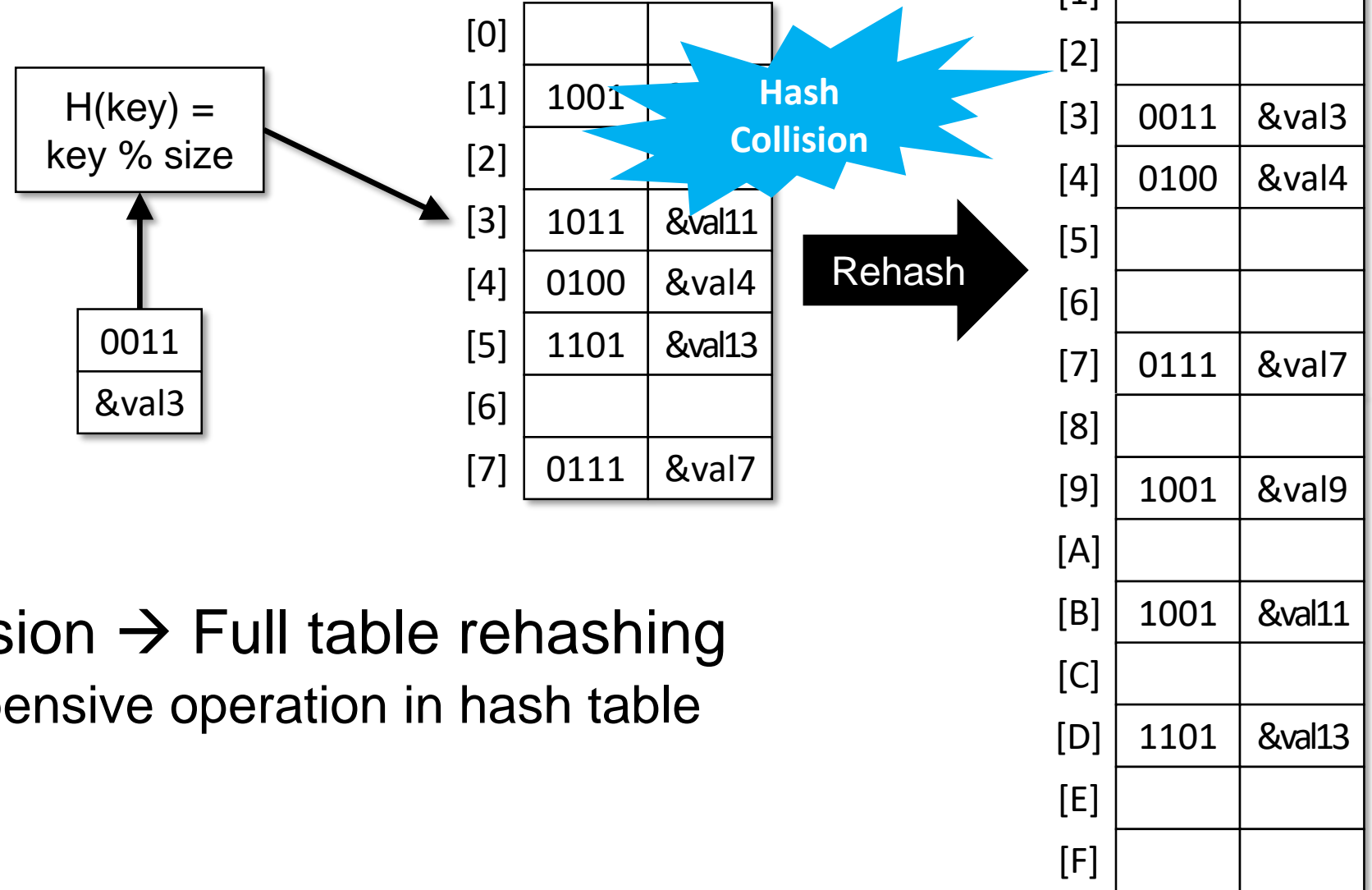
Cacheline-Conscious Extendible Hashing

- Challenges and Contributions
- 3-Level Structure of CCEH
- Failure-atomic Directory Update

Evaluation

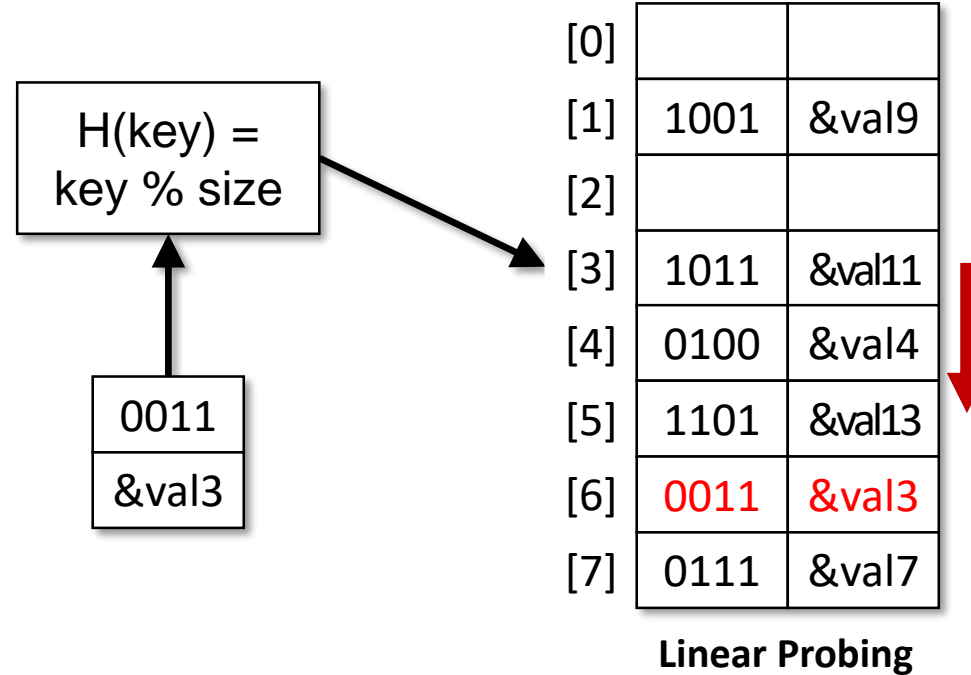
Conclusion

Background: Static Hashing



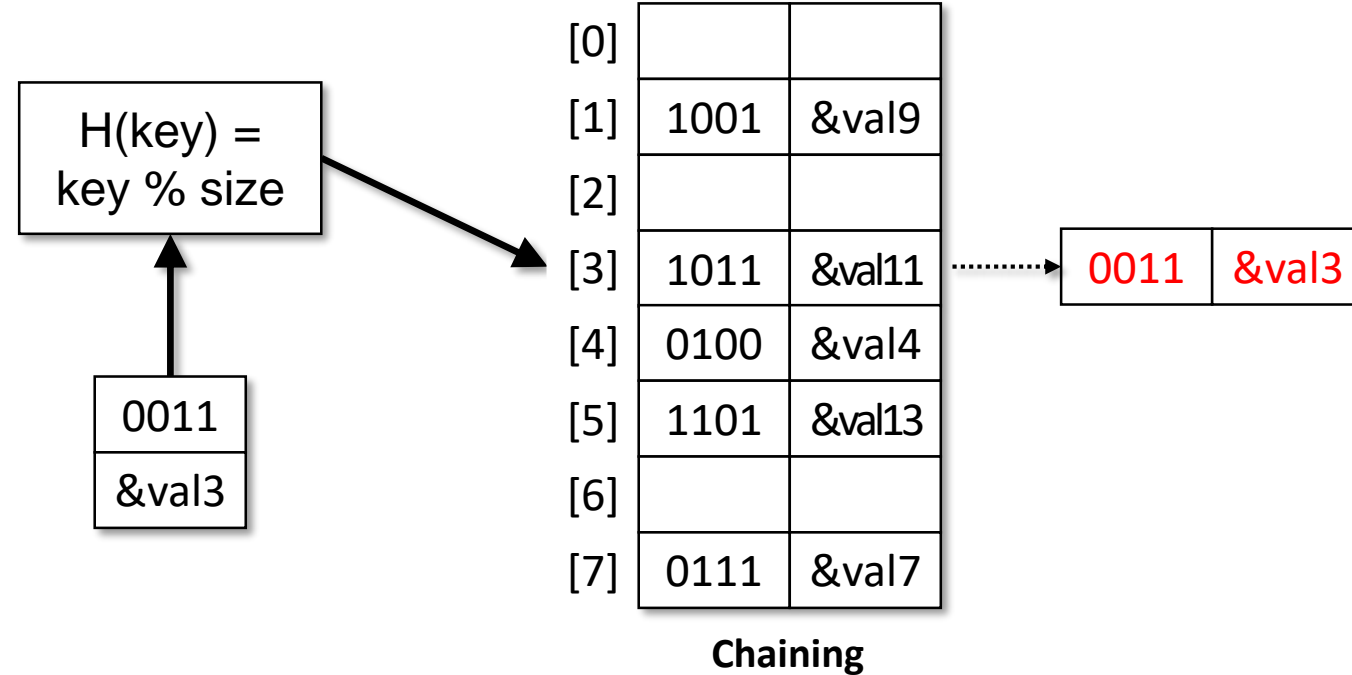
- Hash key collision → Full table rehashing
 - The most expensive operation in hash table

Background: Static Hashing



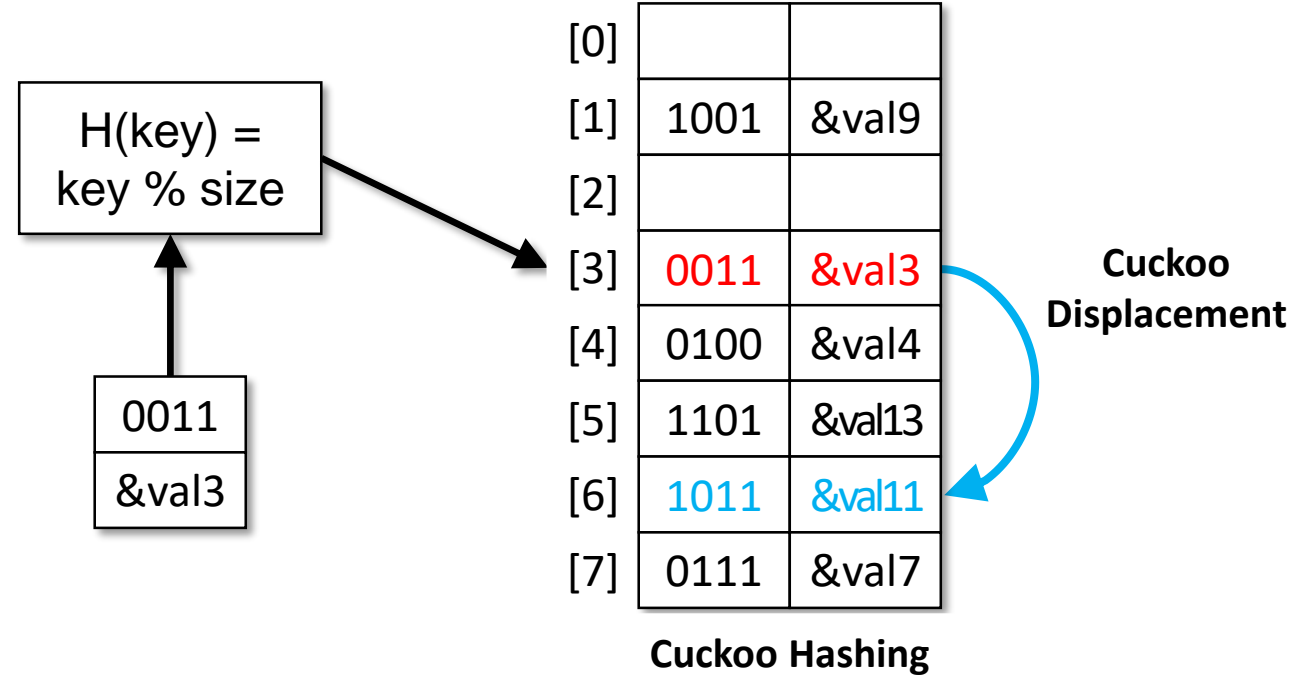
- To avoid full table rehashing:
 - Linear probing
 - Chaining
 - Double hashing such as Cuckoo hashing

Background: Static Hashing



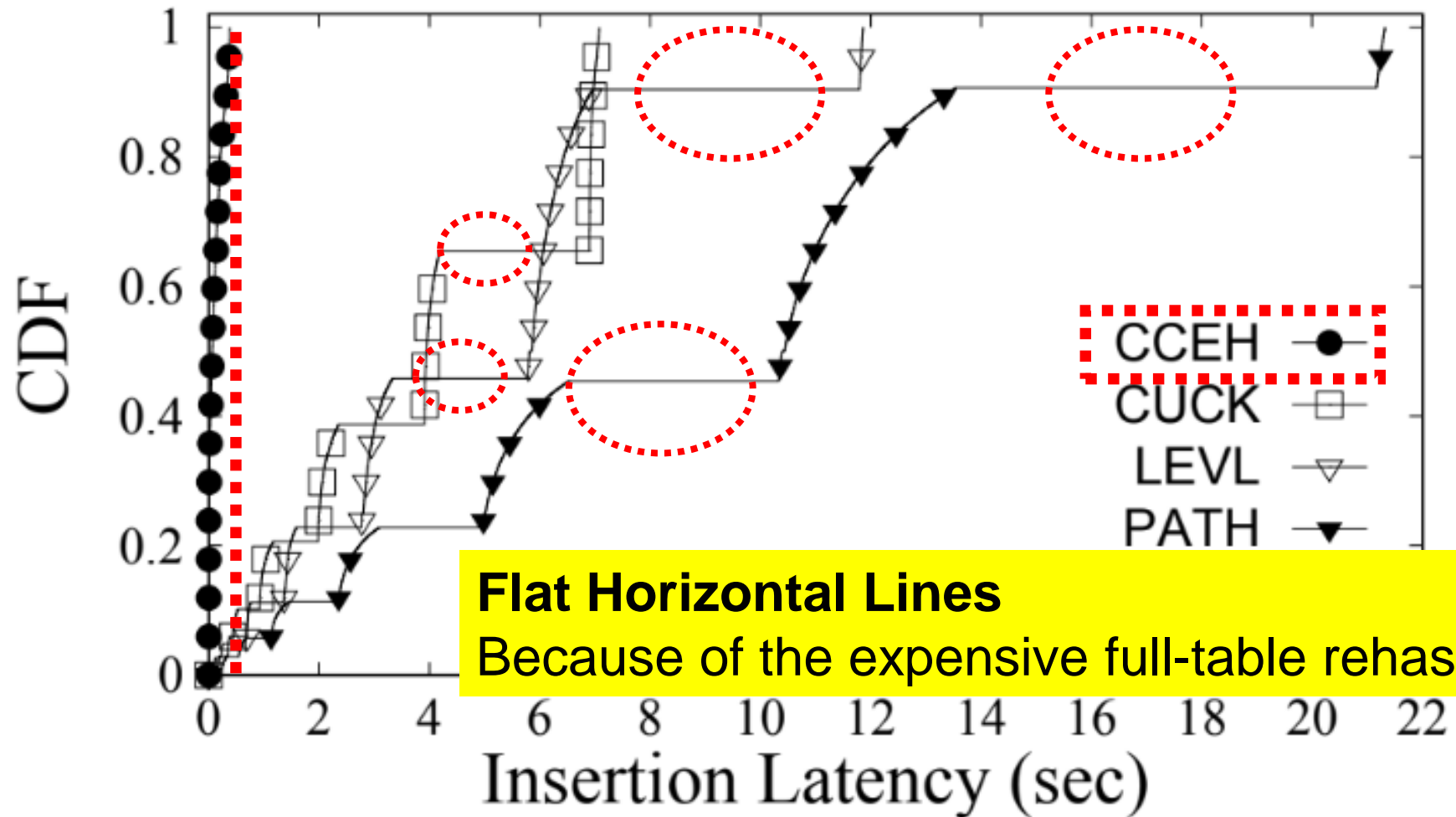
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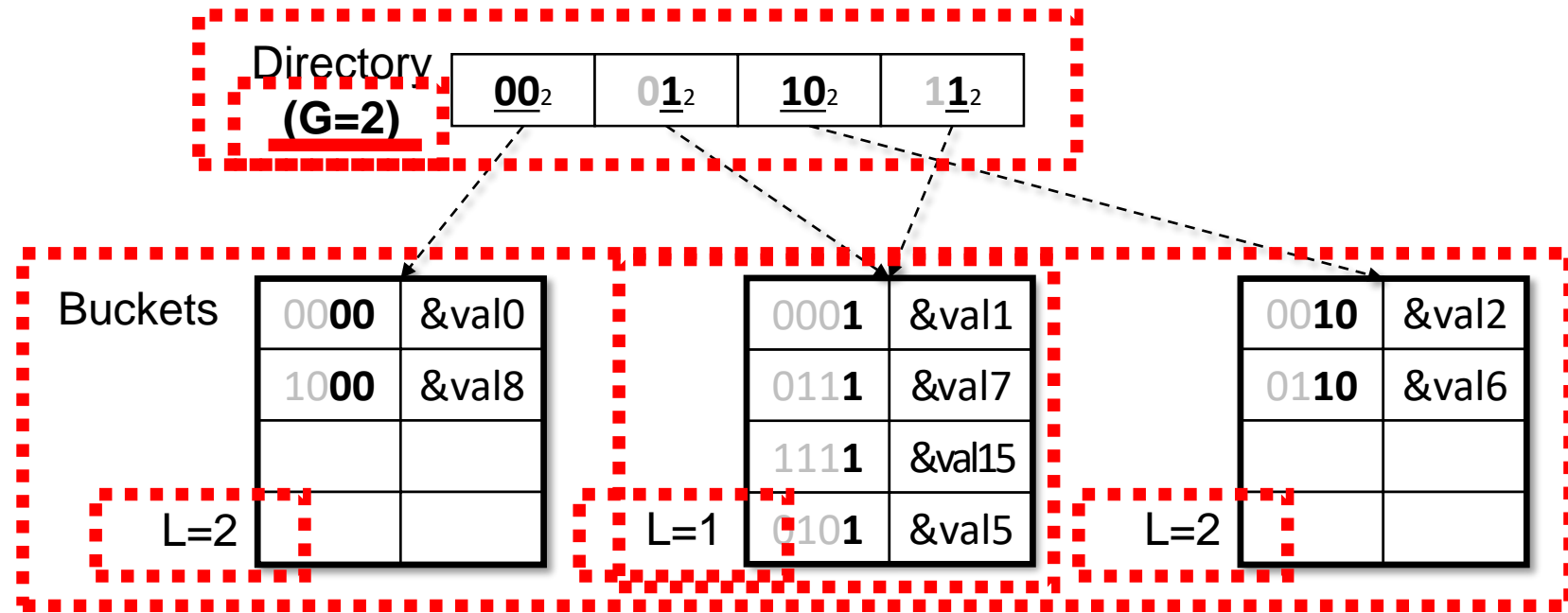
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Insertion Latency CDF



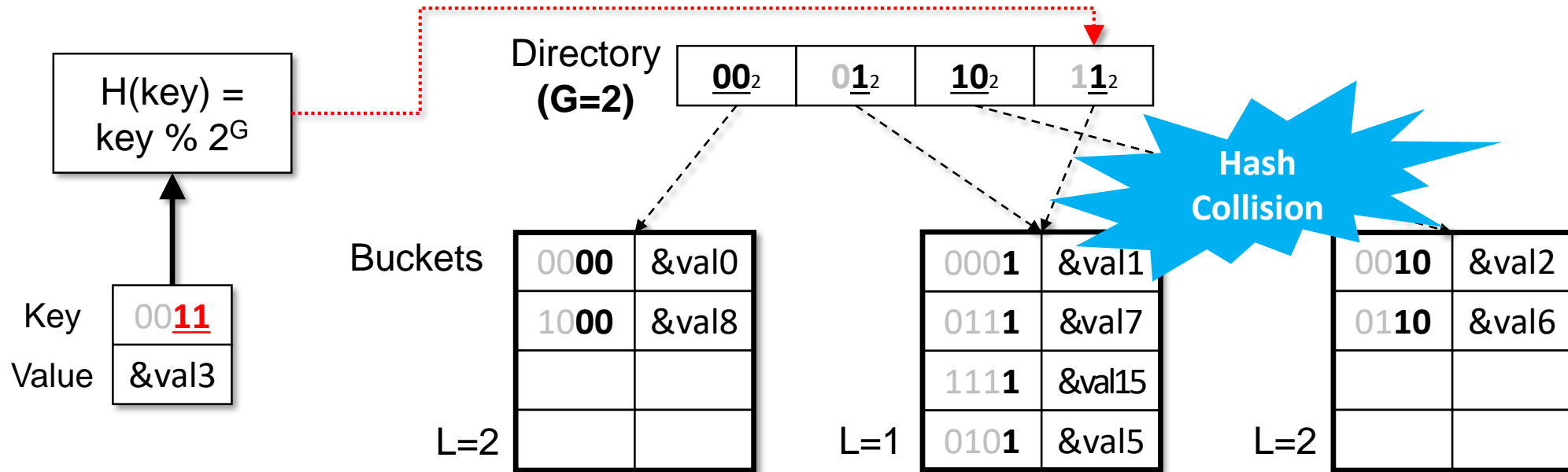
Background: Disk-based Extendible Hashing

Hash Function:
 $H(\text{key}) = \text{key} \% 2^G$

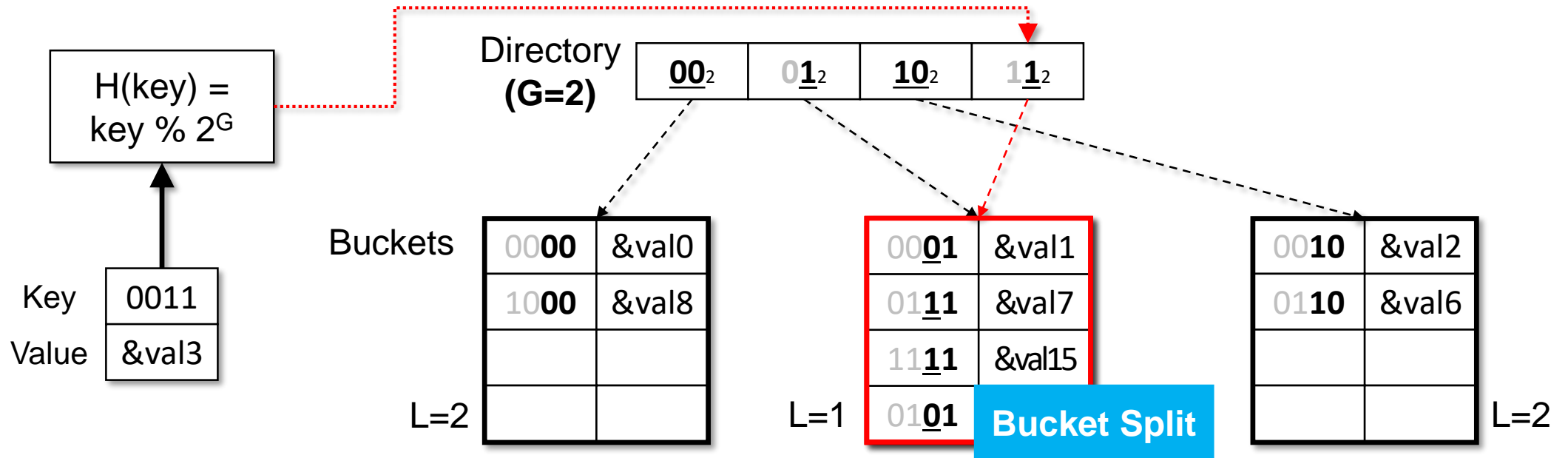


- Dynamically splits one bucket or merges two buckets at a time

Background: Extendible Hashing – Insertion

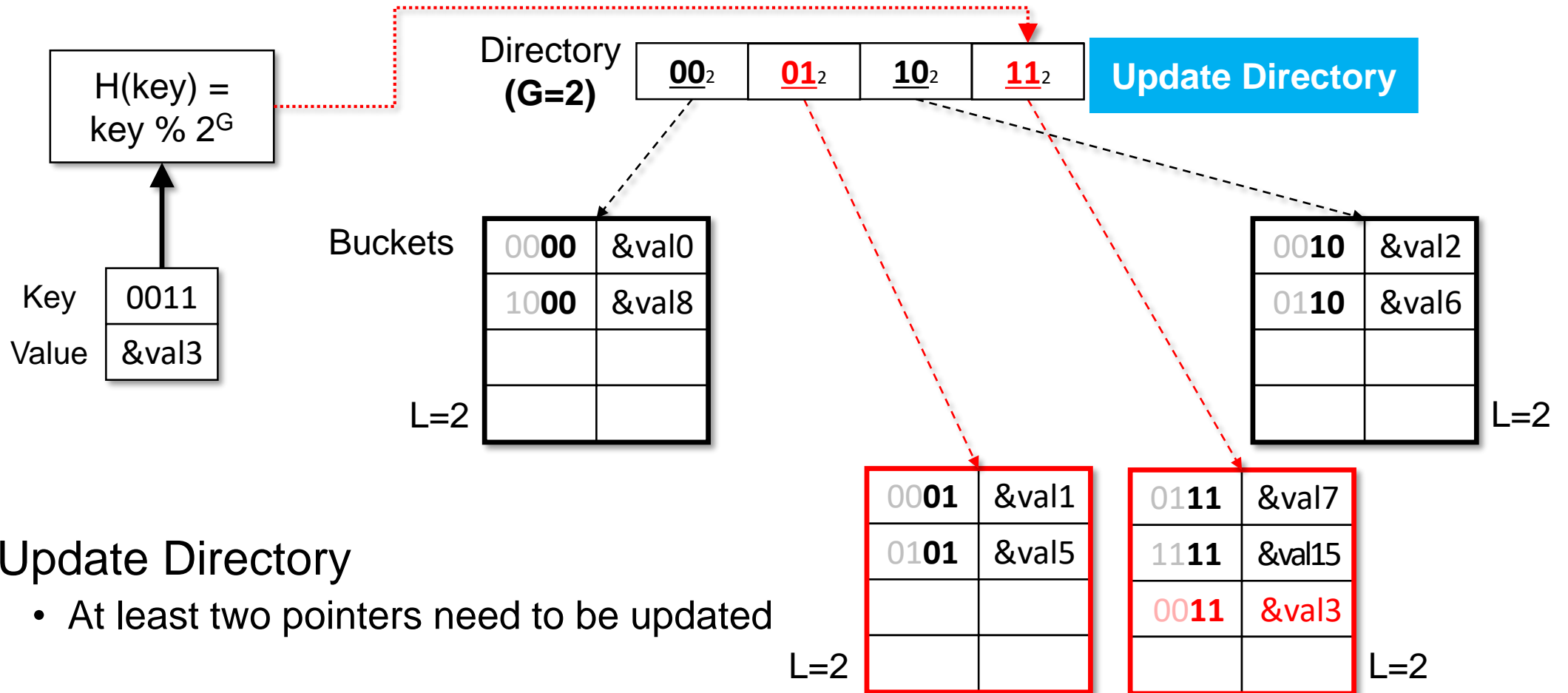


Background: Extendible Hashing – Bucket Split



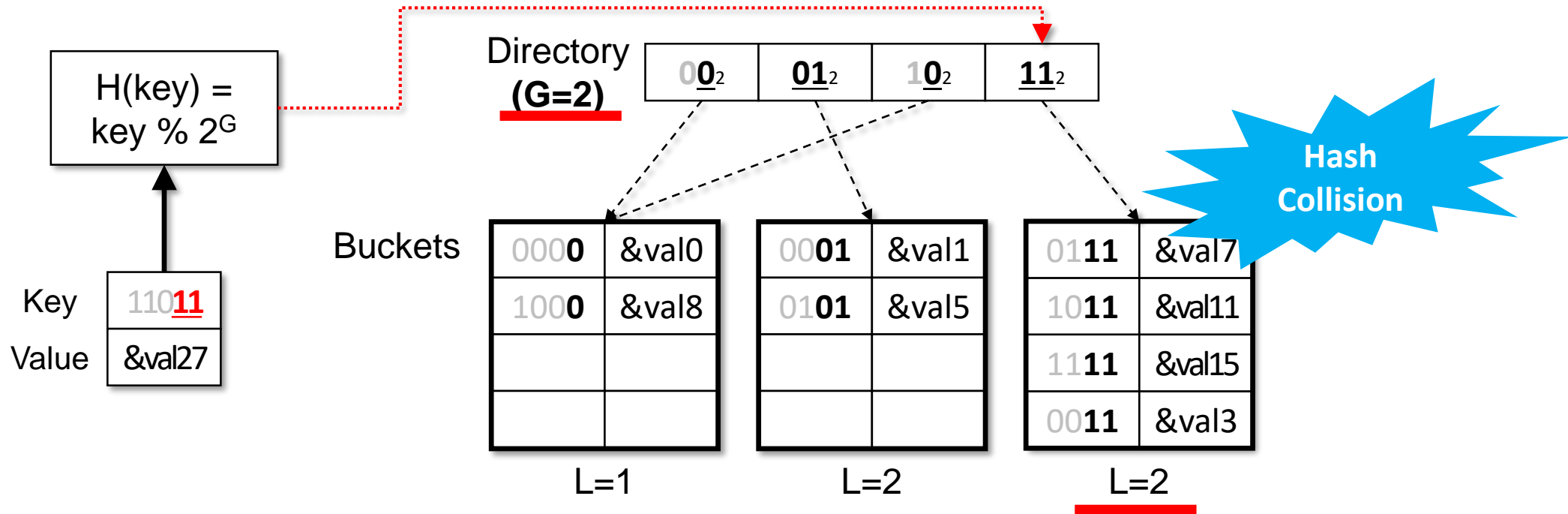
- Only overflown bucket is modified

Background: Extendible Hashing – Bucket Split



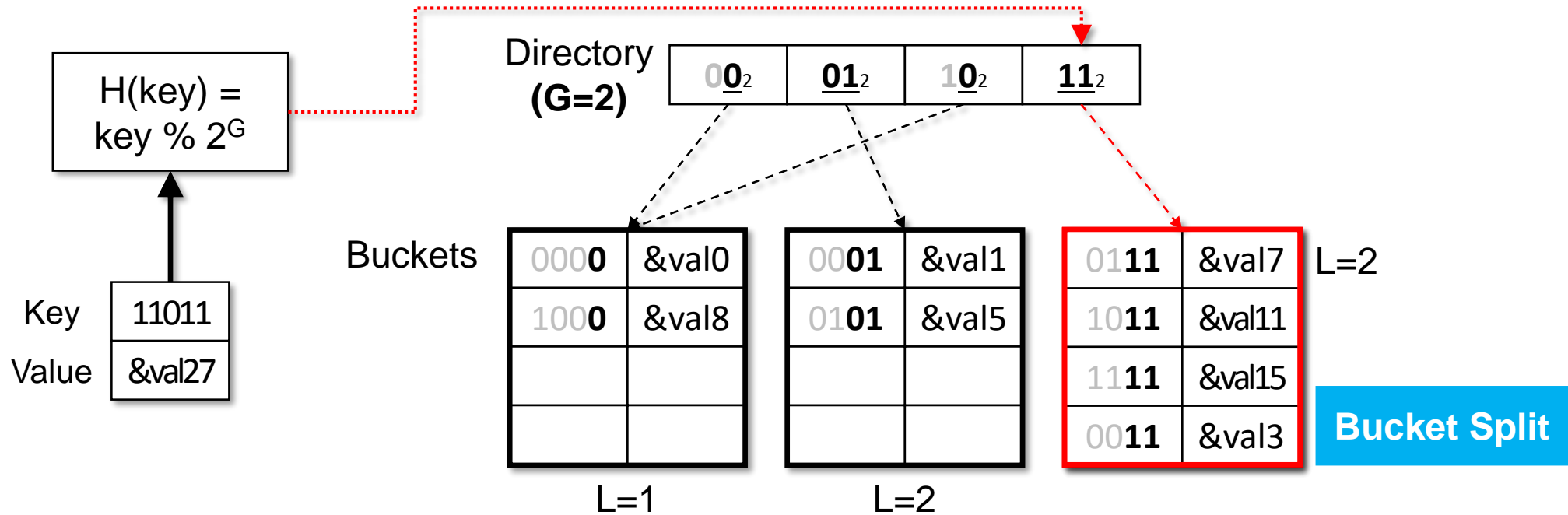
- Update Directory
 - At least two pointers need to be updated

Background: Extendible Hashing – Directory doubling



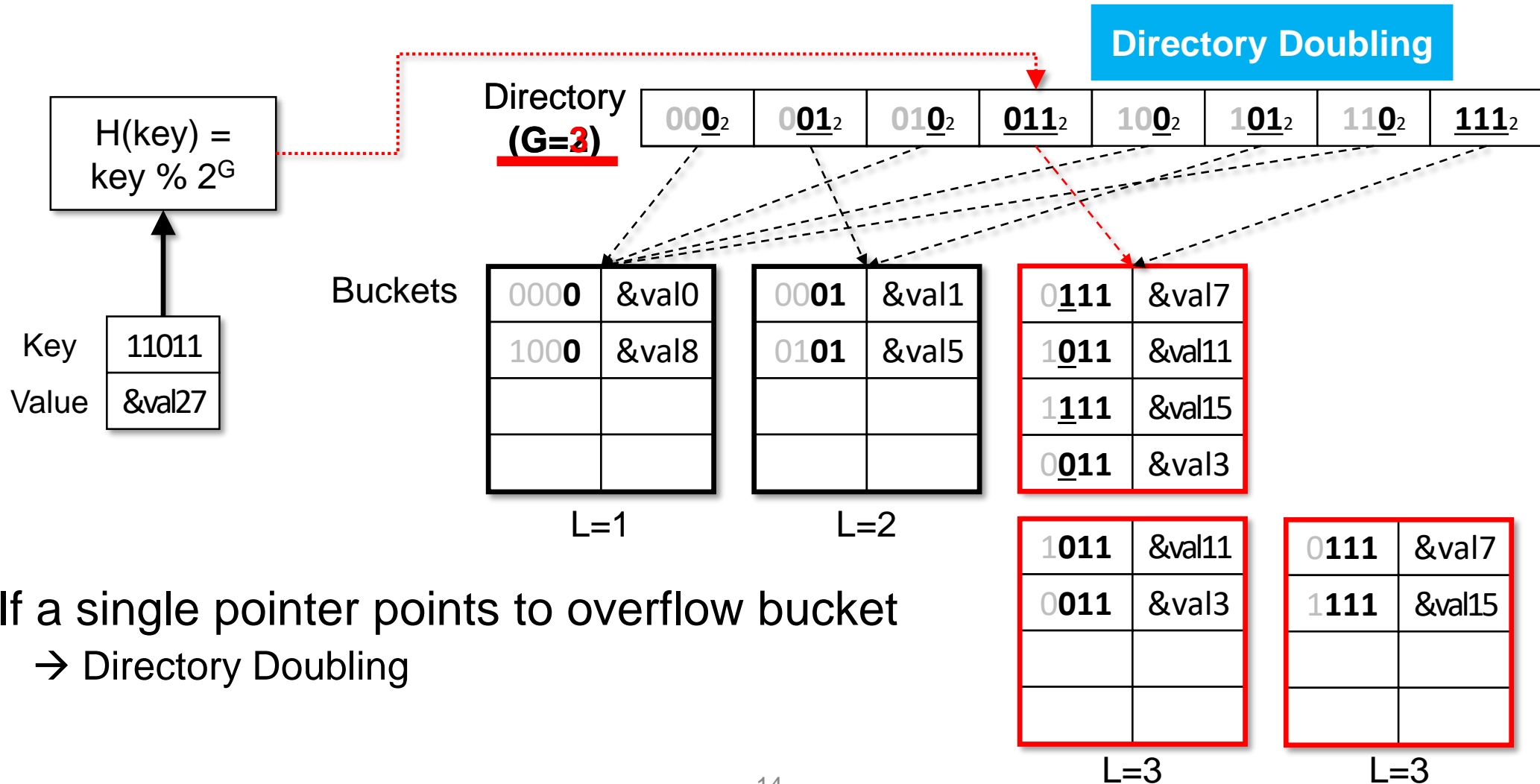
- If a single pointer points to overflow bucket
→ Directory Doubling

Background: Extendible Hashing – Directory doubling



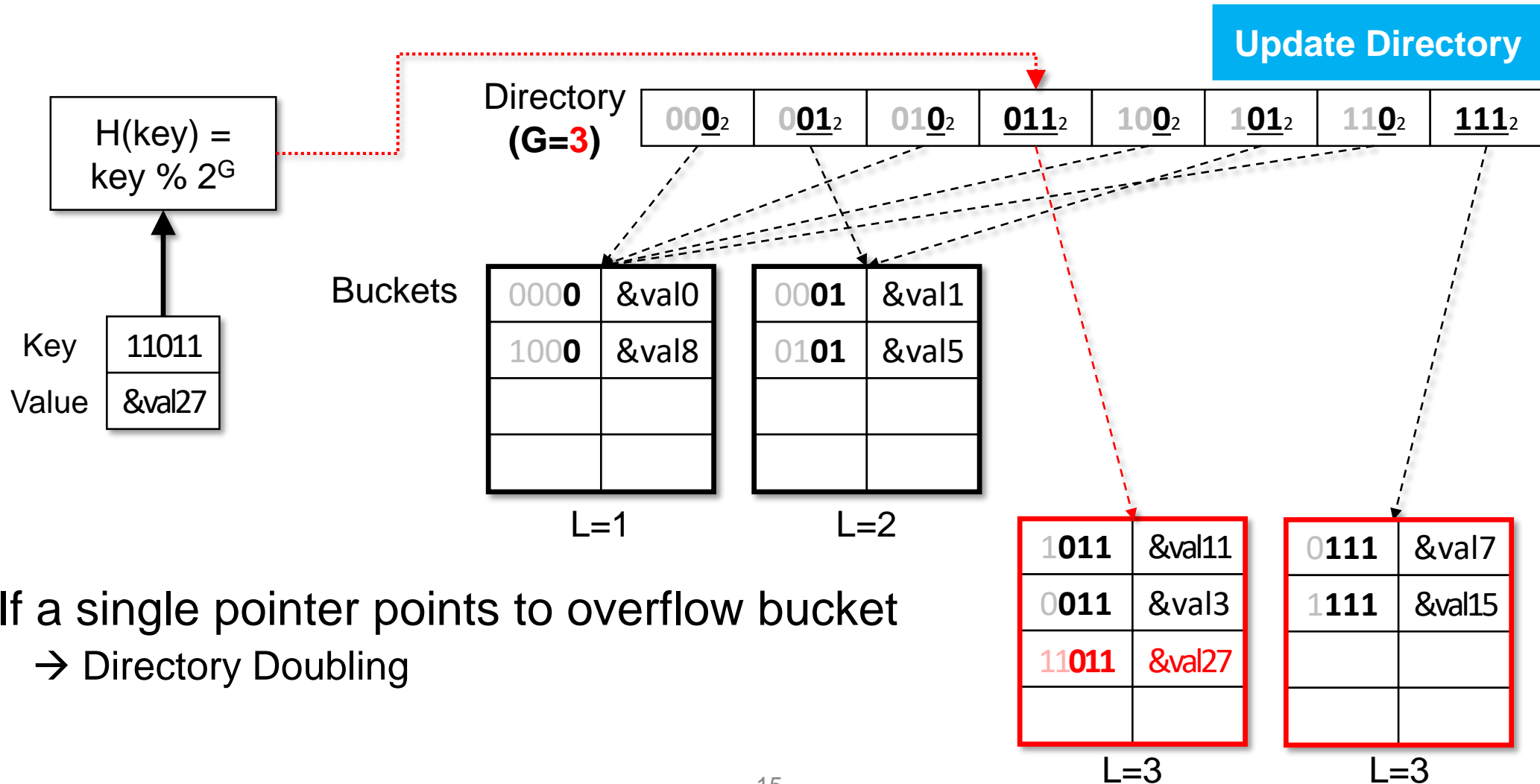
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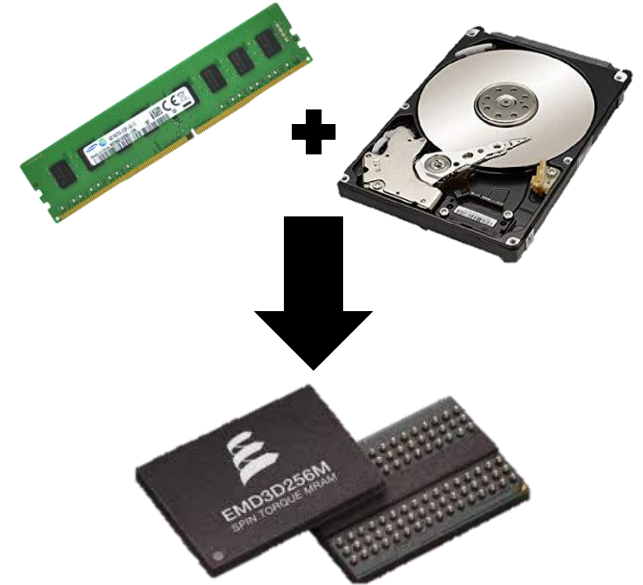
Persistent Memory

Characteristics

- High performance – Comparable to DRAM
- Byte-addressability – As DRAM
- Persistence – As storage devices (HDD/SSD)

Challenges

- Atomic unit of writes → 8-bytes
- Data transfer unit between CPU cache and PM → 64 byte cacheline
- Order of memory writes is not guaranteed



Outline

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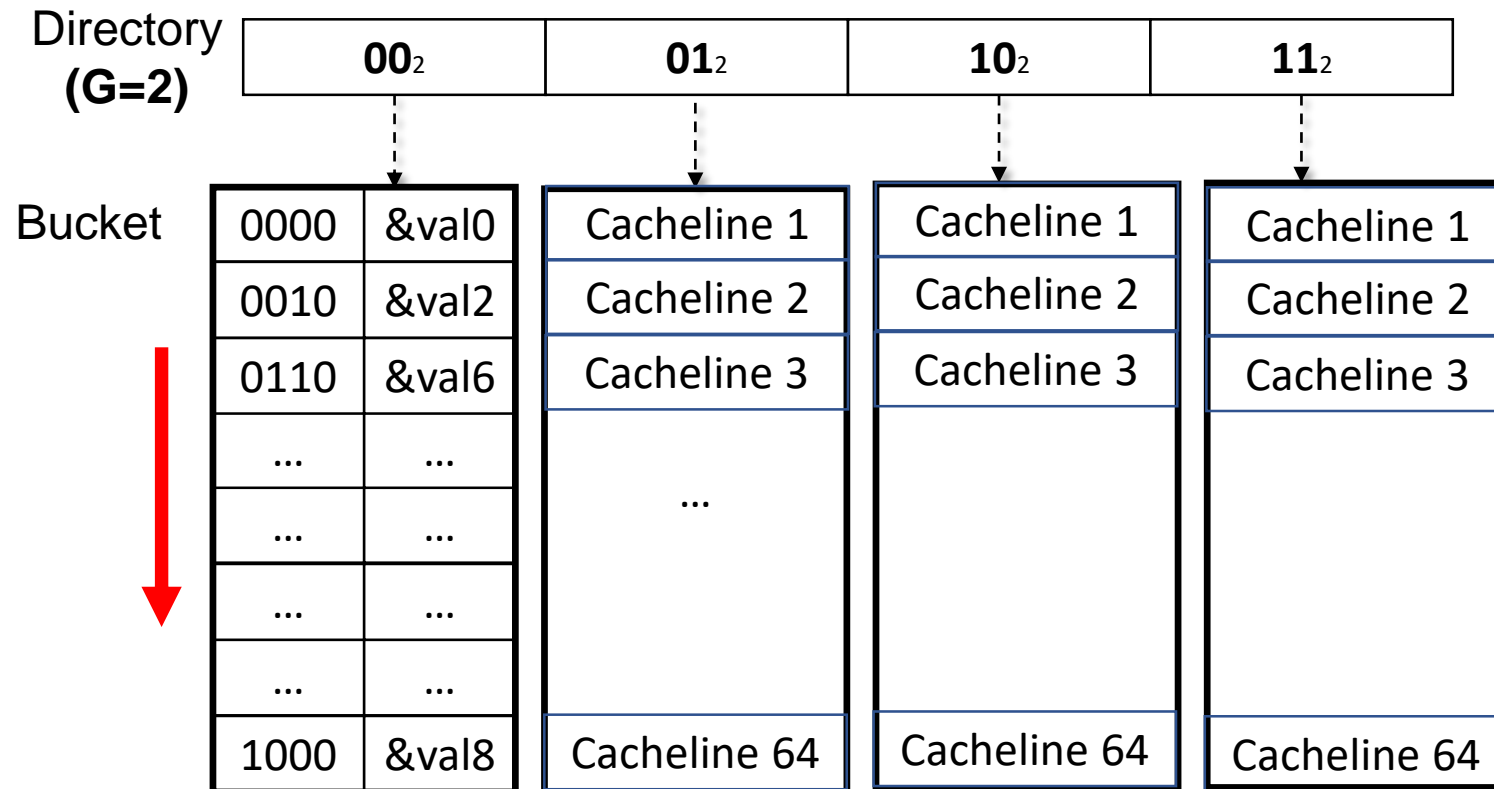
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- Failure-atomic Directory Update

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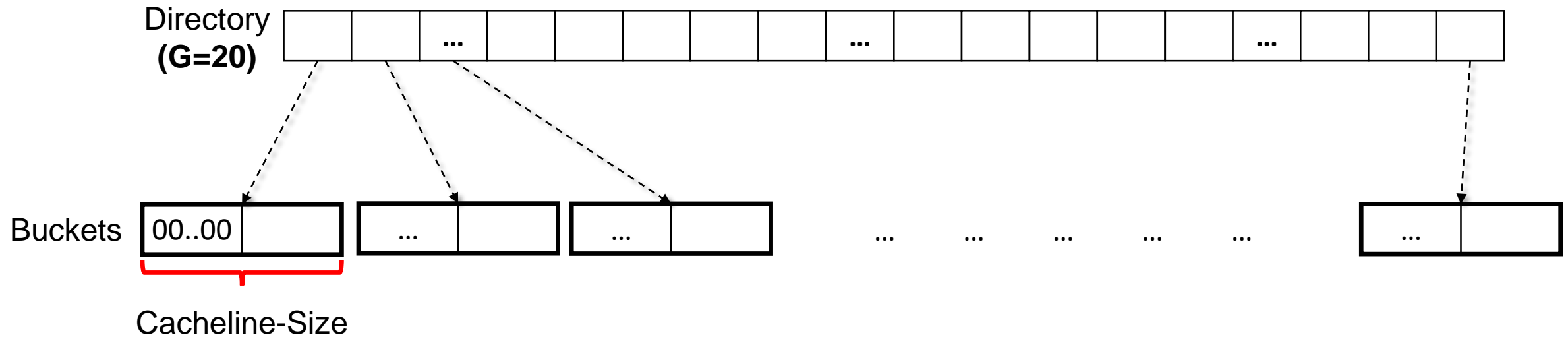
Challenge in In-Memory Extendible Hashing



Problems

- Page-sized bucket → 64 cacheline accesses per bucket

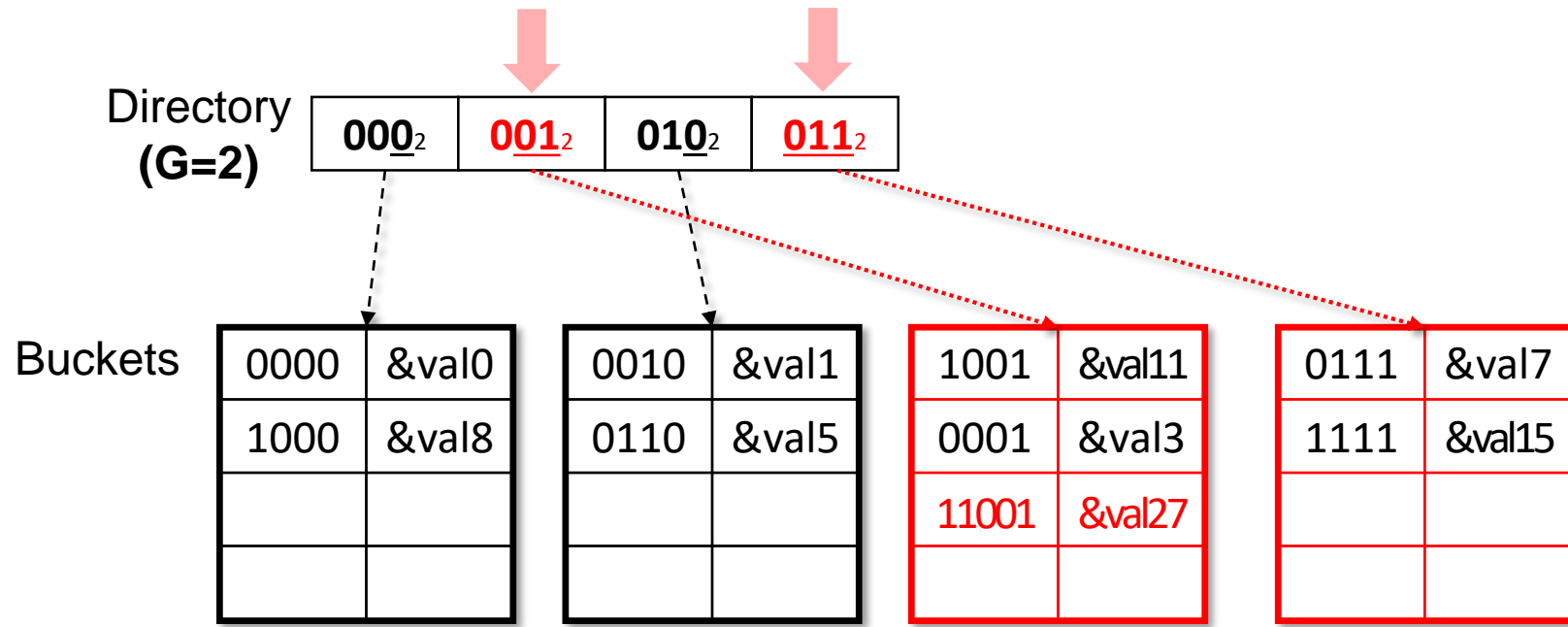
Challenge in In-Memory Extendible Hashing



Problems

Cacheline-sized small bucket → a large directory
(8 byte pointer per cacheline)

Challenge in Extendible Hashing on PM



Problems

Split operation updates multiple pointers → Not Failure-Atomic

Contributions

3-Level Structure

- Introduces an intermediate level, **Segment**
- Lookup via only **two cacheline accesses**

Failure-atomic Directory Updates

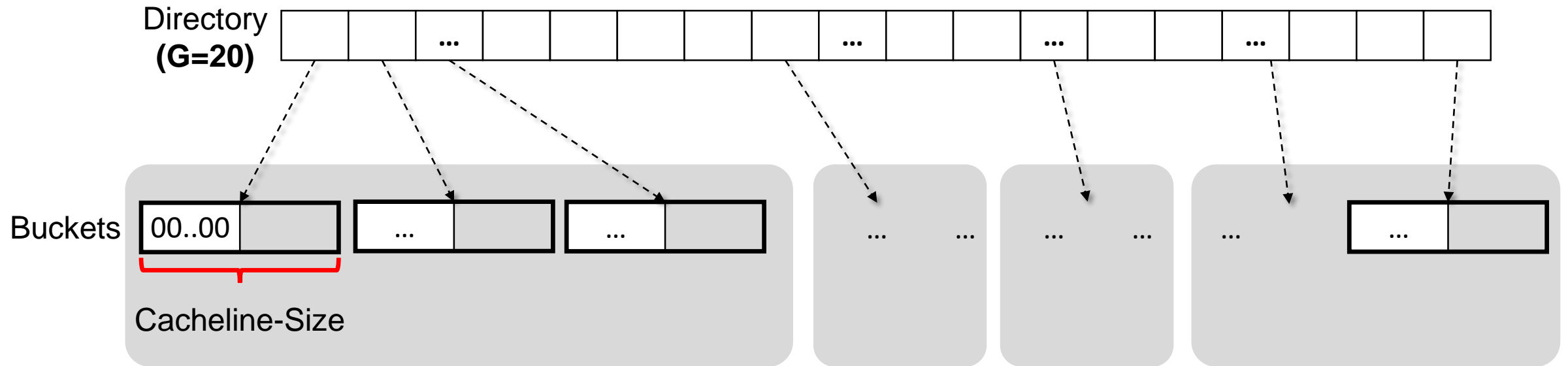
- Introduces **the split buddy tree** to manage split history

Failure-atomic Segment Split

- **Lazy deletion** scheme to minimize dirty writes

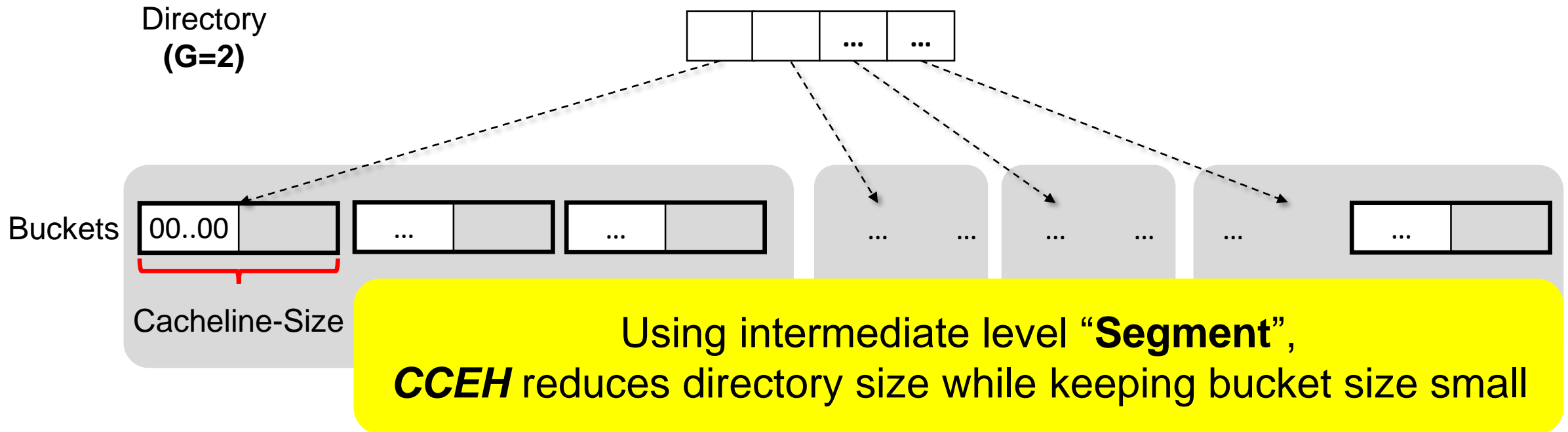


Segment: Intermediate Level



- A group of multiple cacheline-sized buckets = Segment

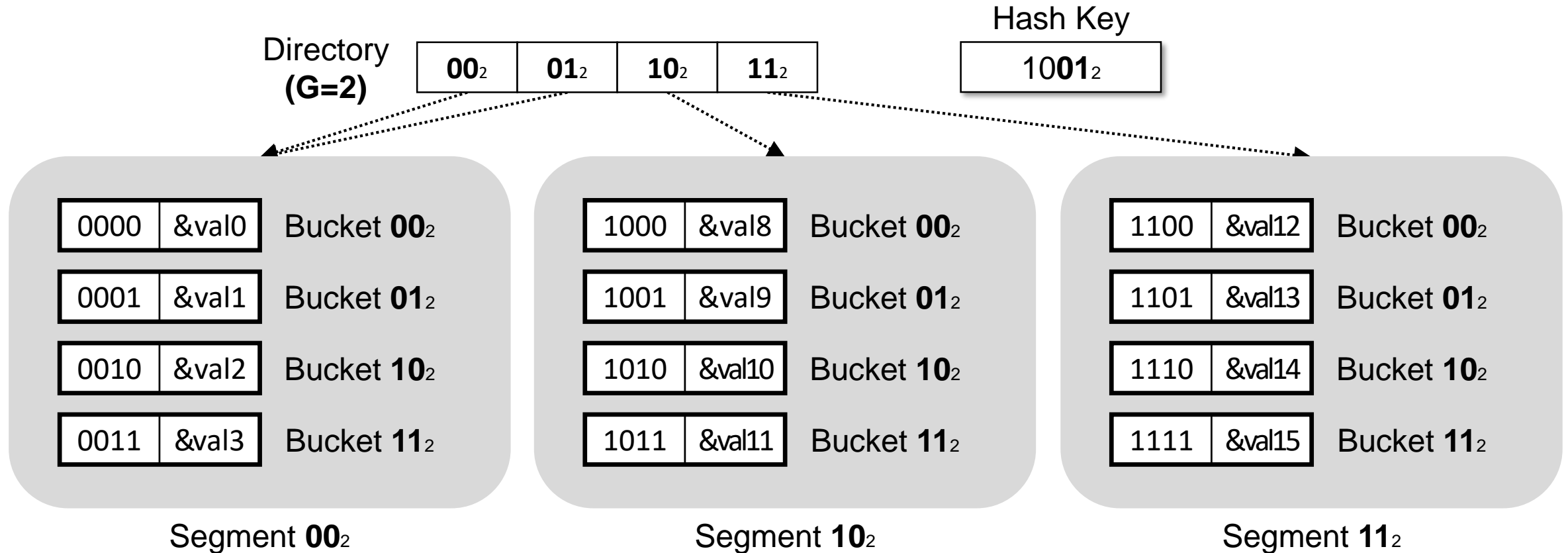
Segment: Intermediate Level



3-Level Structure

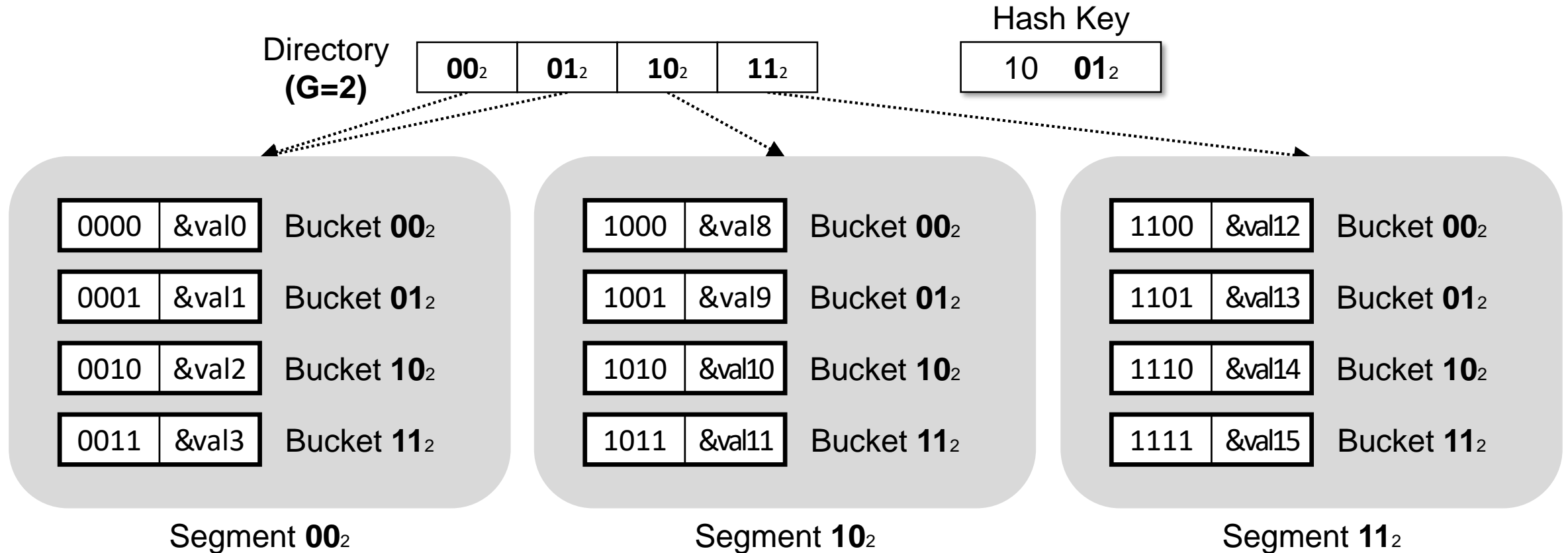
Directory → Segment → Cacheline-sized Bucket

Minimize Cacheline Accesses in Segment



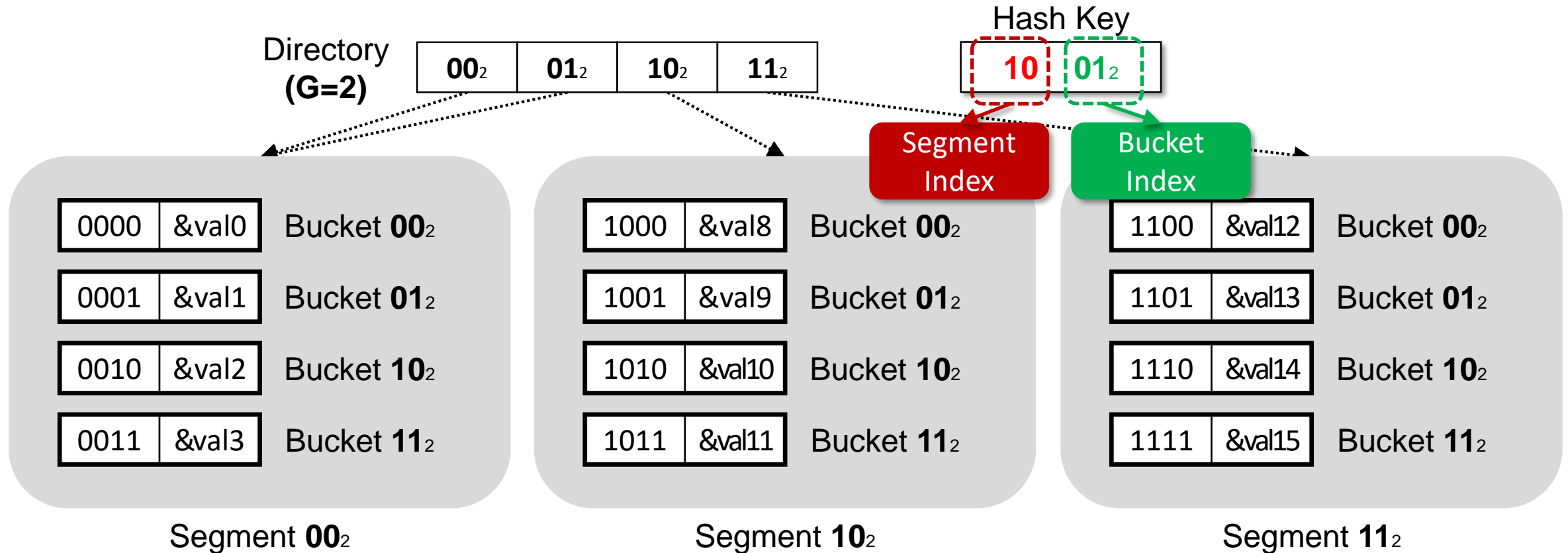
Q: With large segments, how can we minimize cacheline accesses?

Minimize Cacheline Accesses in Segment



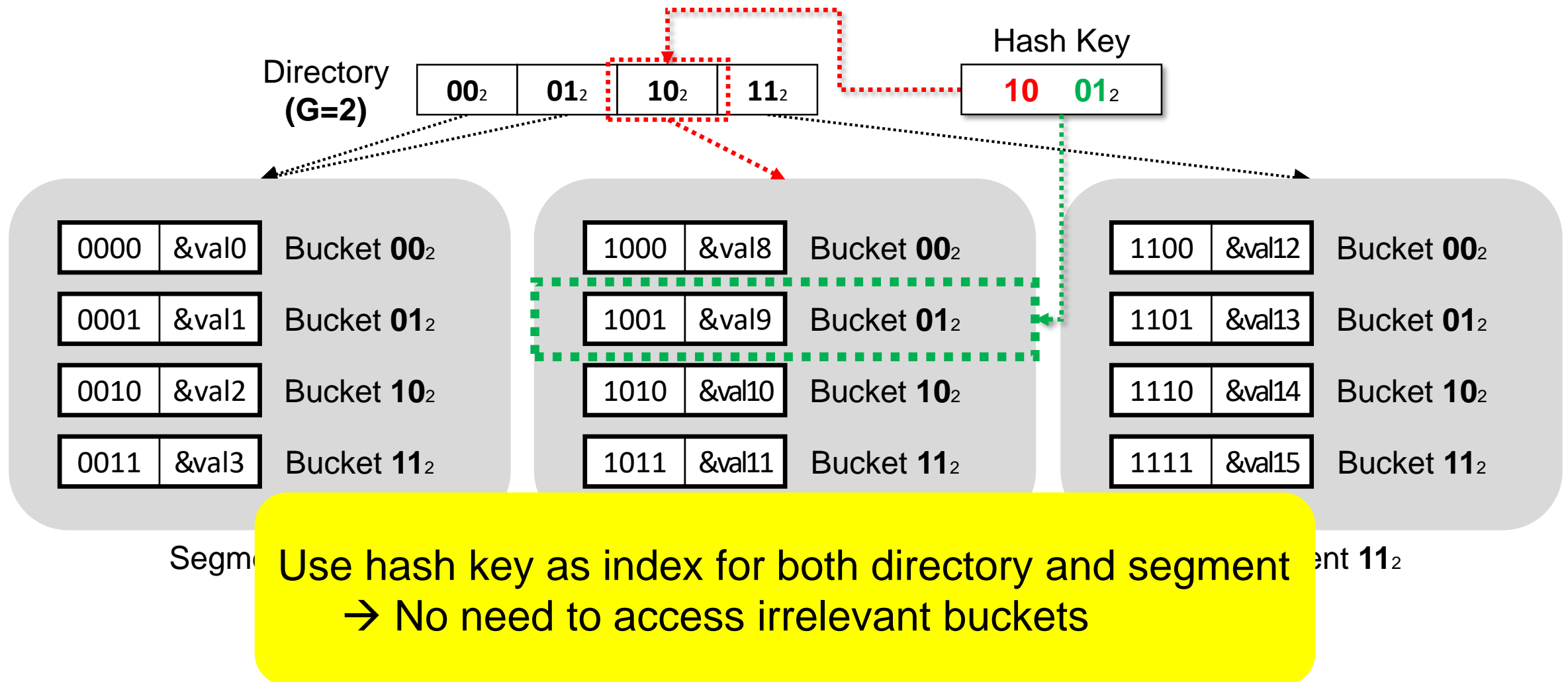
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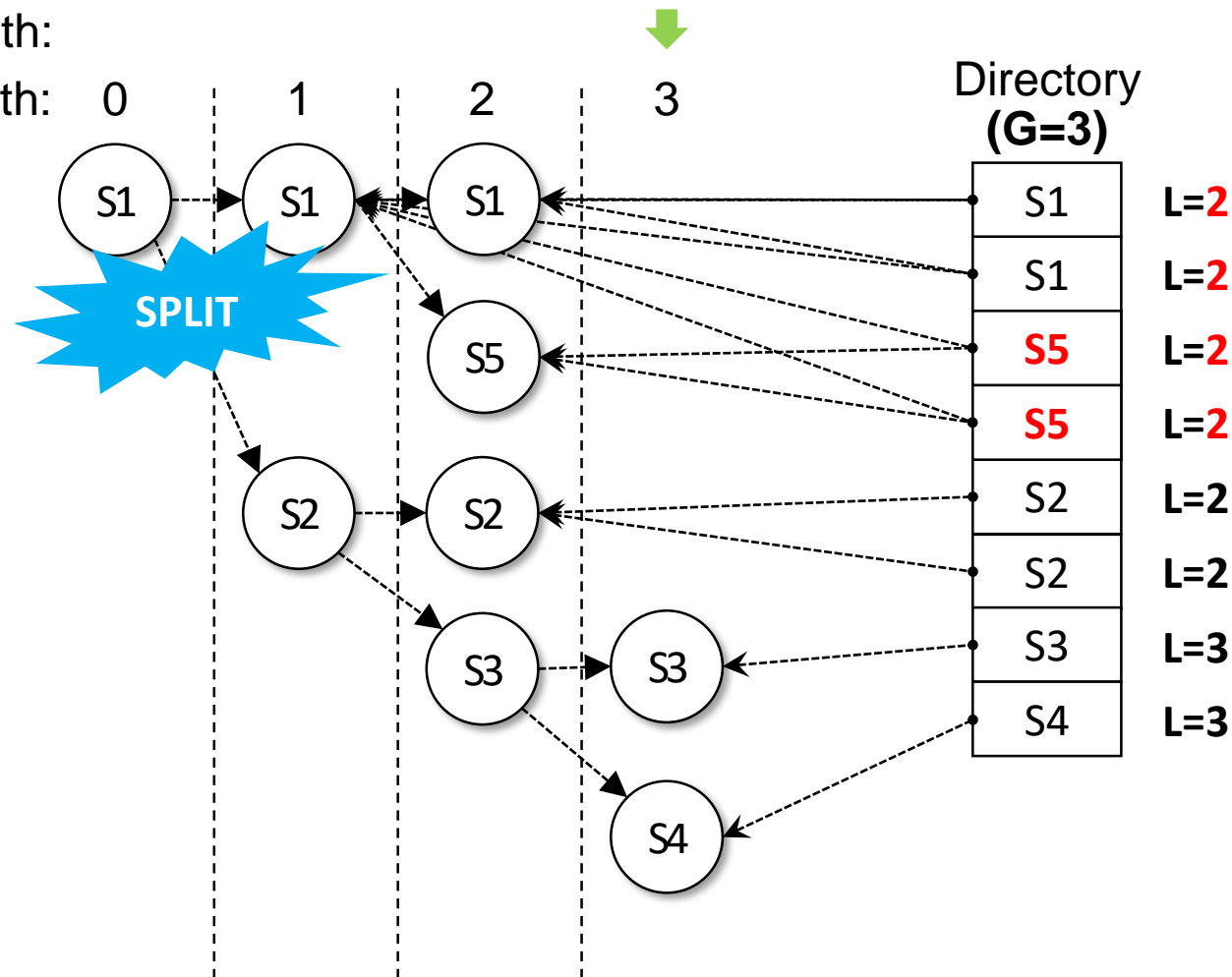
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Recovery: Split History Buddy Tree in CCEH

Global Depth:

Depth:



(3) Update local depth of S1

(2) Update a directory entry

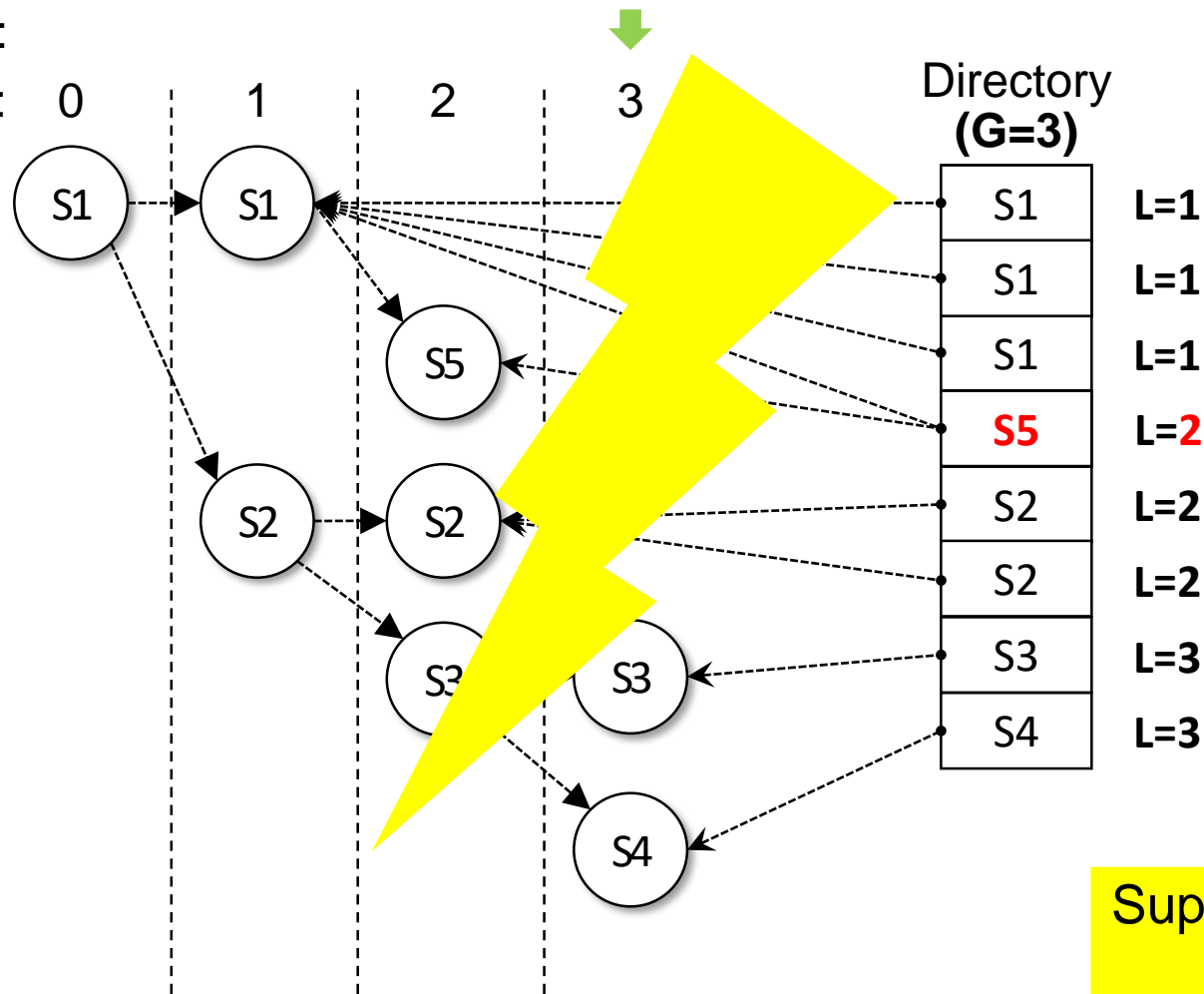
(1) Update a directory entry

Using **MSB** segment index, split segments are pointed by **adjacent directory** entries

Recovery: Split History Buddy Tree in CCEH

Global Depth:

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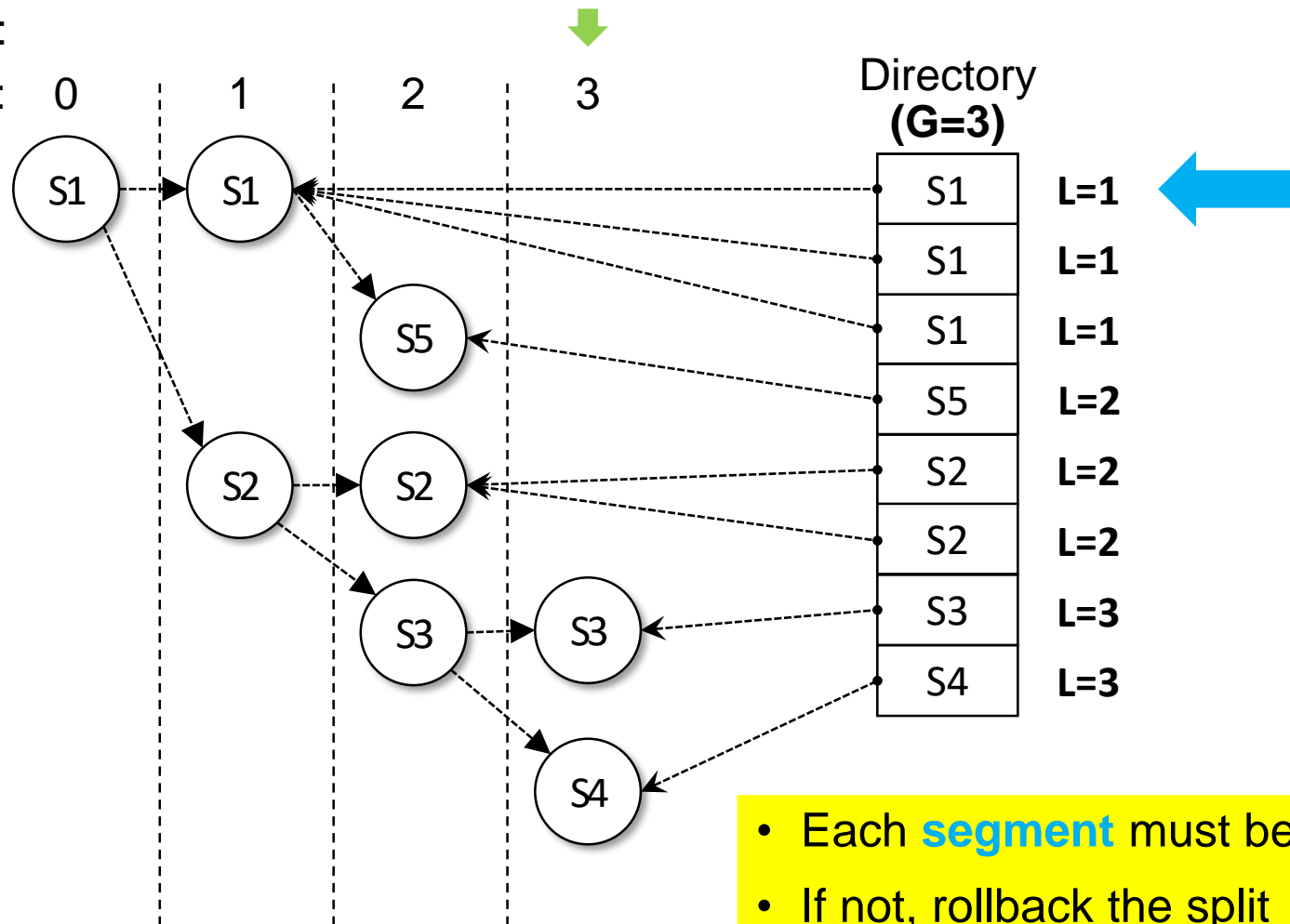


Suppose a system crashes while **S5** splits

Recovery: Split History Buddy Tree in CCEH

Global Depth:

Depth:



$$\text{Stride} = 2^{G-L}$$

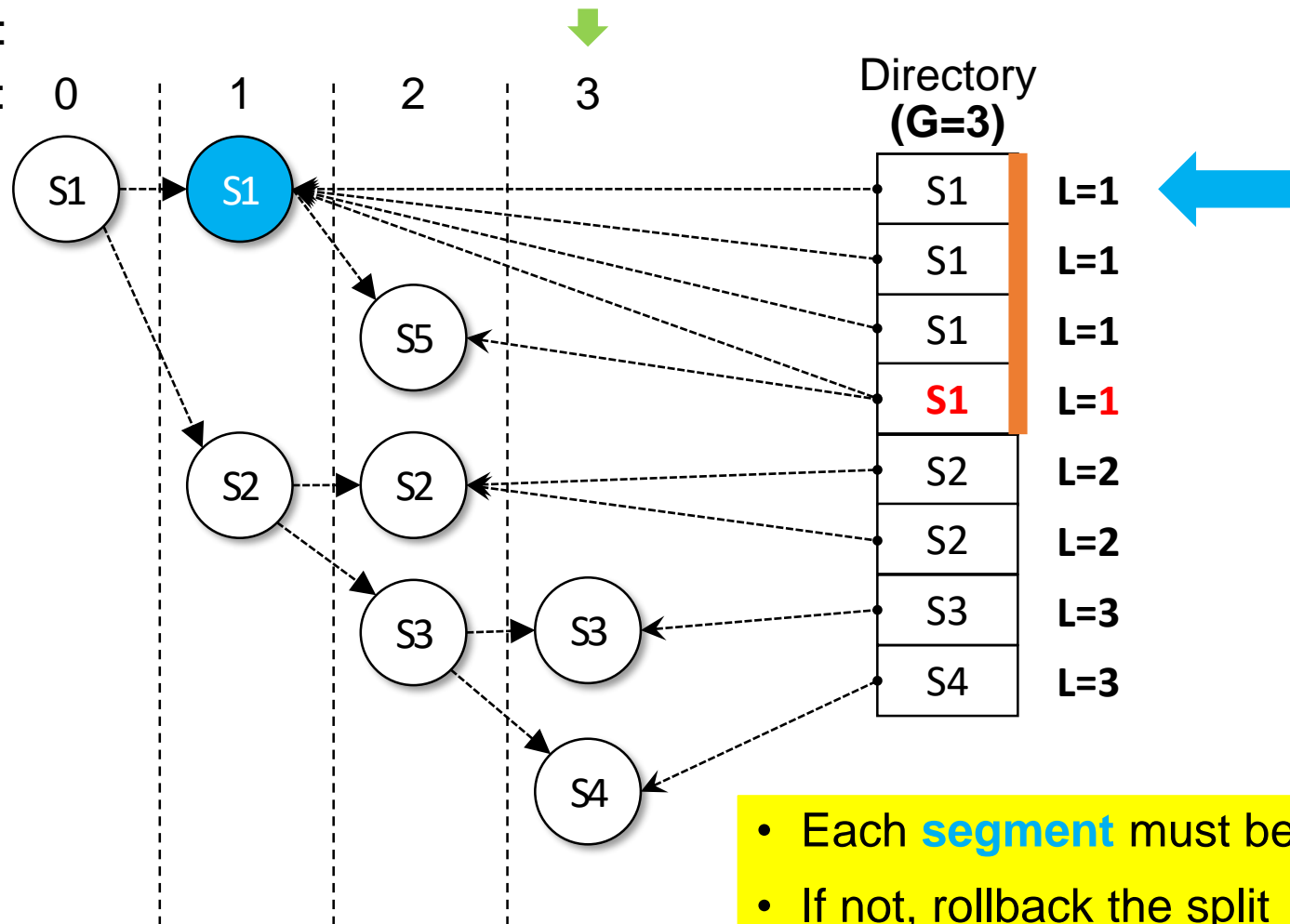
Global Depth $G = 3$
Local Depth $L = 1$
Stride = 4

- Each **segment** must be pointed by 2^{G-L} directory entries
- If not, rollback the split

Recovery: Split History Buddy Tree in CCEH

Global Depth:

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$$\text{Stride} = 2^{G-L}$$

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Failure-atomic Directory Updates

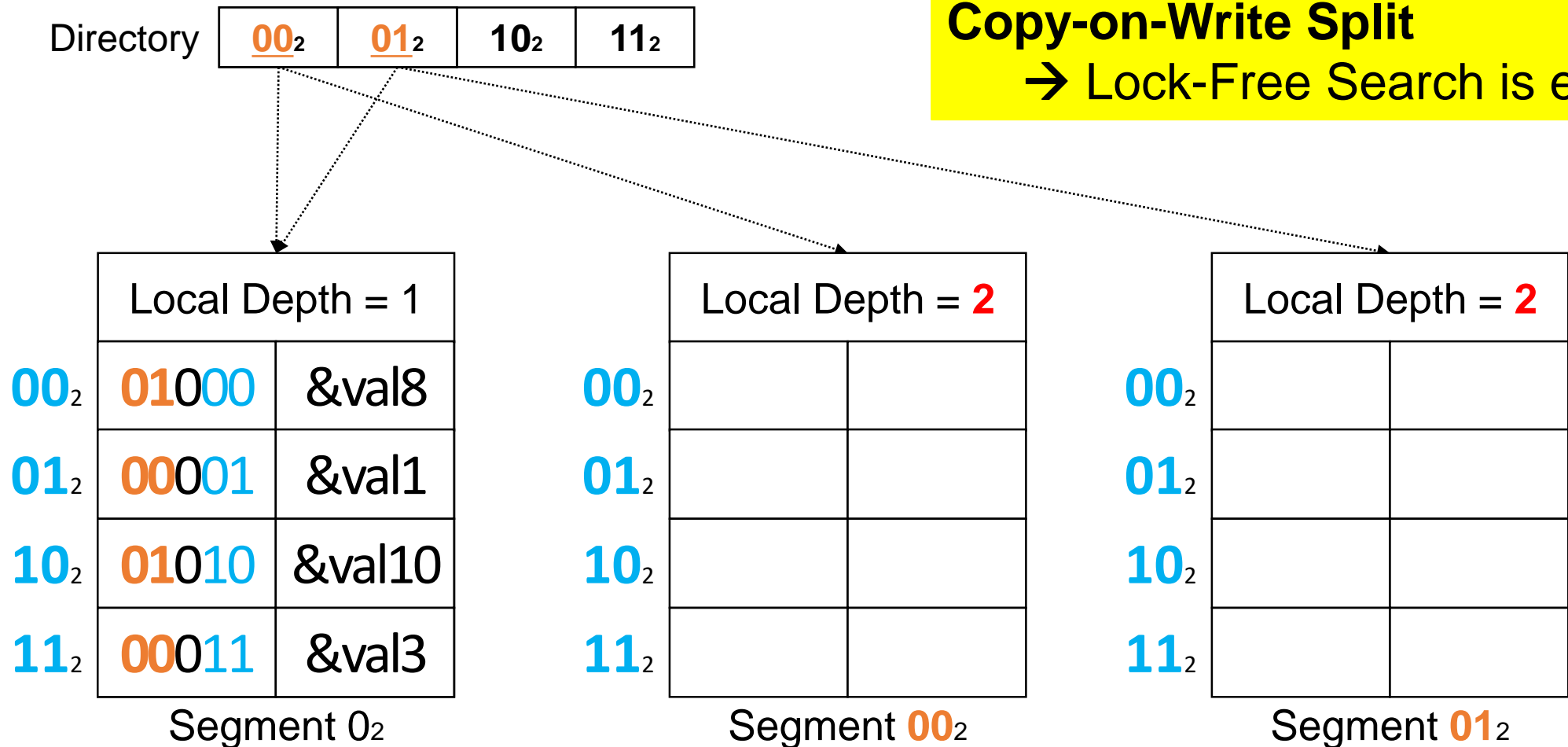
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Failure-atomic Segment Split

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Segment Split: Legacy CoW



Segment Split: Lazy Deletion

Directory

<u>00</u> ₂	<u>01</u> ₂	10 ₂	11 ₂
------------------------	------------------------	-----------------	-----------------

Lazy Deletion

→ Minimizes dirty writes

	Local Depth = 2	
00 ₂	01 000	&val8
01 ₂	00001	&val1
10 ₂	01 010	&val10
11 ₂	00011	&val3

Segment 00₂

Single
Cacheline-flush
invalidates all the
migrated data

	Local Depth = 2	
00 ₂		
01 ₂		
10 ₂		
11 ₂		

Segment 01₂

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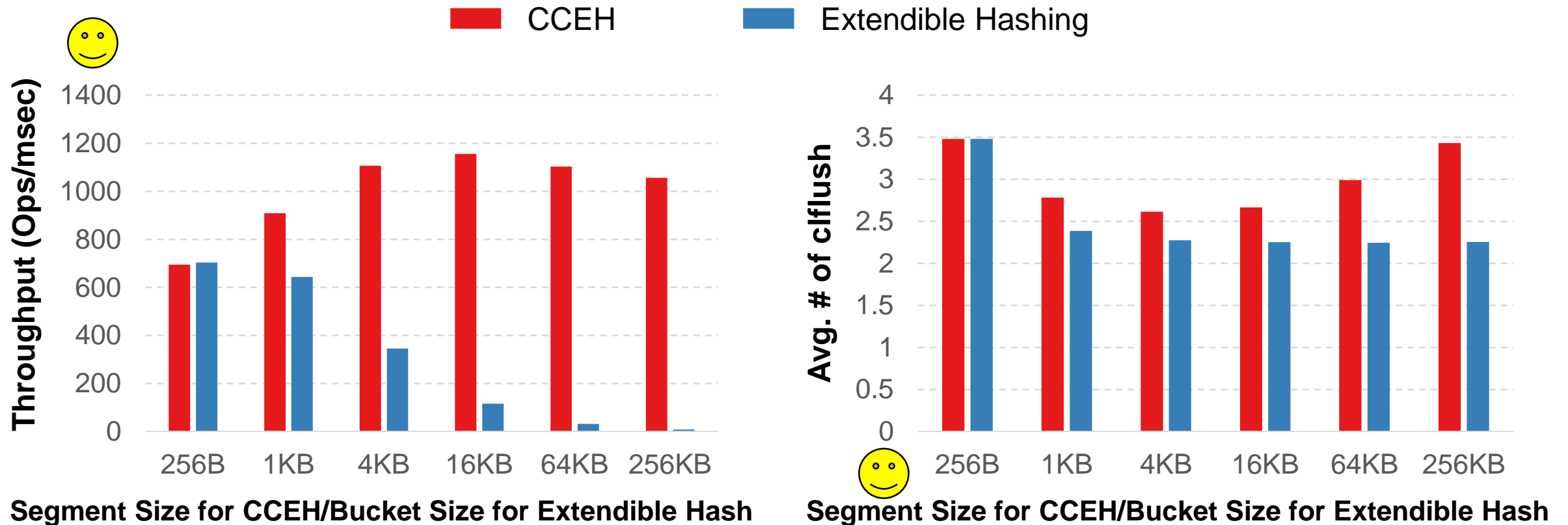
Evaluation

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Experimental Setup

CPU	2x Intel Xeon Haswell-Ex E7-4809 v3 → 8 cores, 2.0 GHz → 20MB L3 cache
Memory	64GB of DDR3 DRAM
PM	Quartz: A DRAM-based PM latency emulator * To emulate write latency, we inject stall cycle after each <i>clflush</i> instructions
Workload	160 Million random number dataset

CCEH VS Legacy Extendible Hash

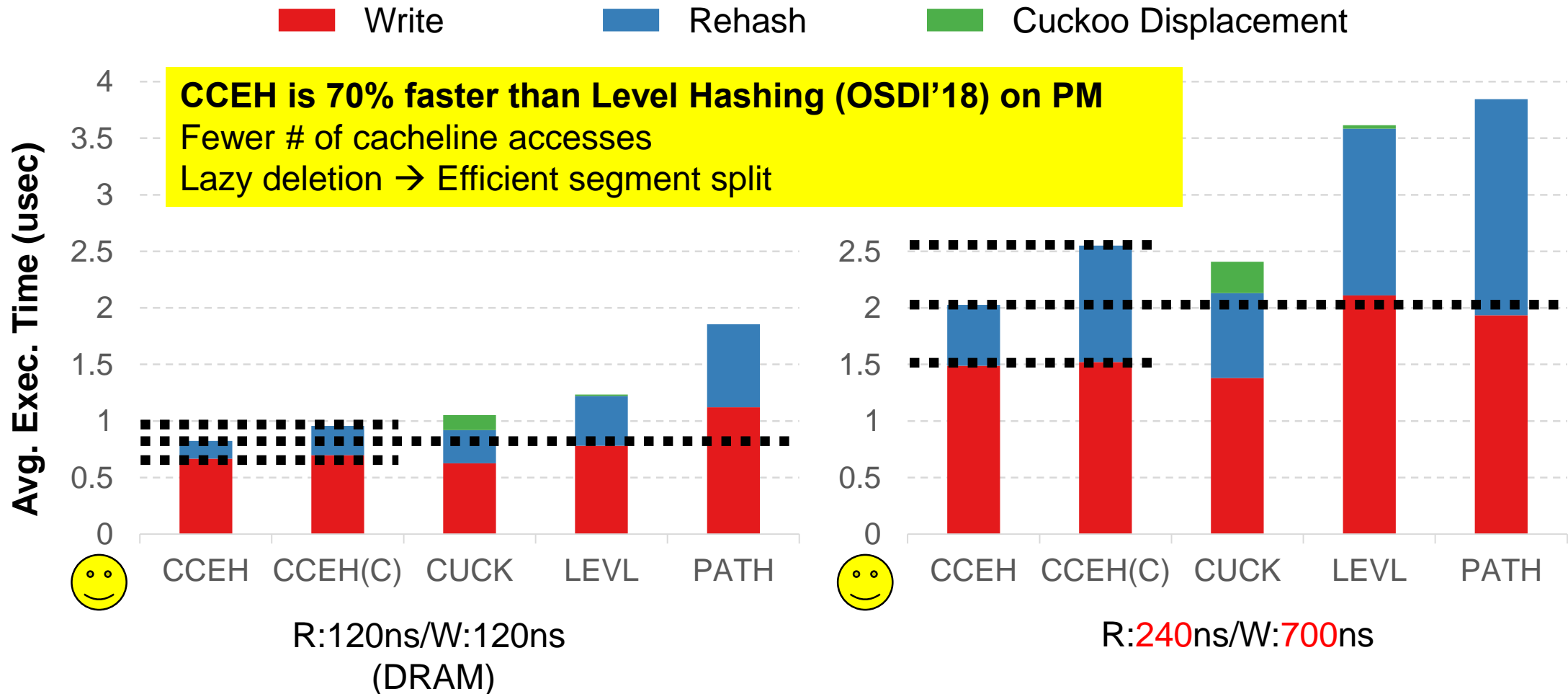


CCEH compared to legacy Extendible Hashing

Cons: Low utilization and more cacheline flushes due to hash collisions

Pros: Constant number of cacheline accesses with varying directory size

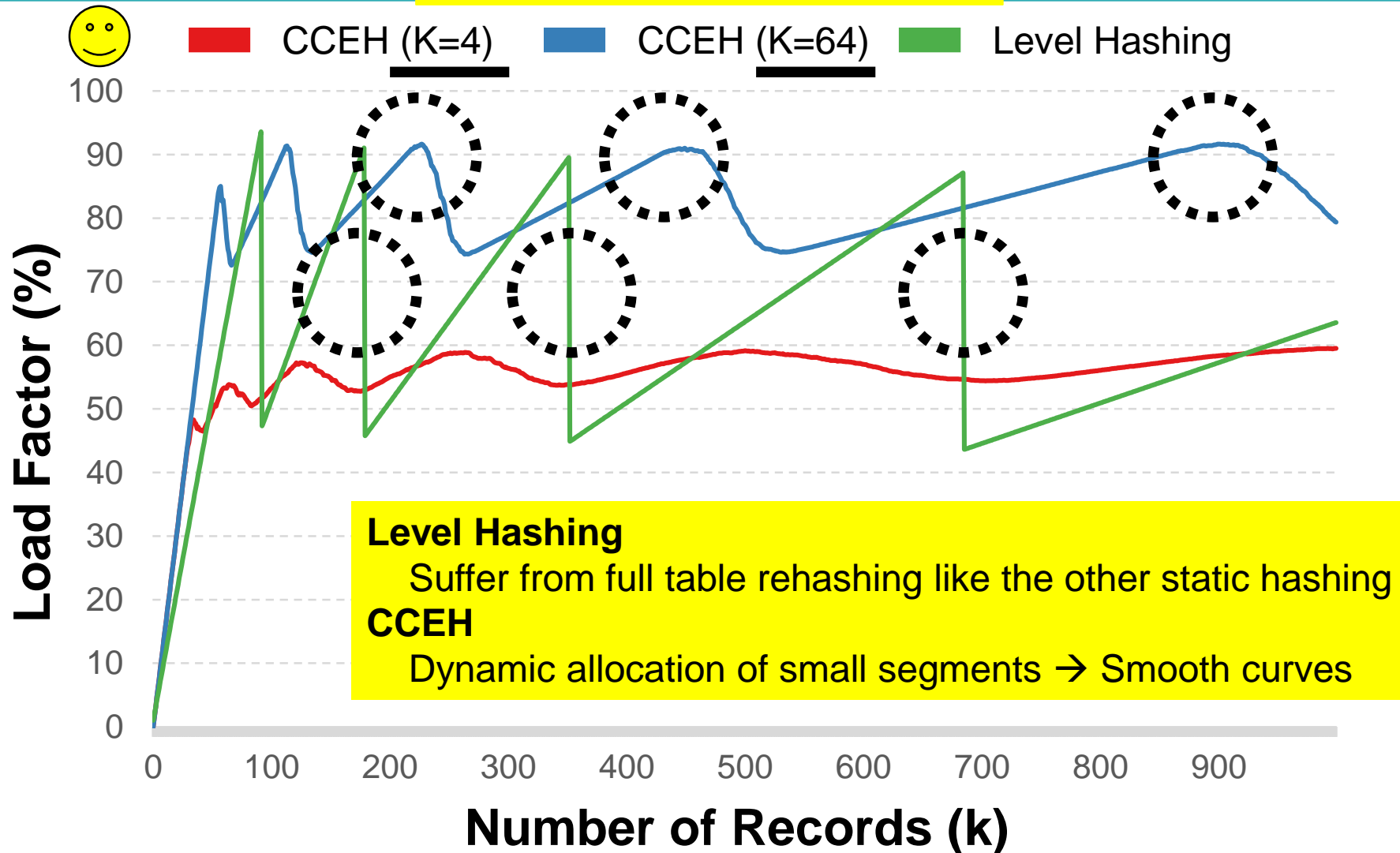
Insertion Performance Breakdown



Load Factor

CCEH (Optimization)

K = Linear probing distance in Segment



Conclusion

Cacheline-Conscious Extendible Hashing (CCEH)

- 3-Level Structure
 - Introduced an intermediate level, Segment
 - Constant Lookup: Only two cacheline accesses → Write-Optimal
- Failure-Atomic Write-Optimal Lazy Deletion → Minimize I/O
- Failure-Atomic Directory Updates → Log-less directory update

Disk-based hashing needs to be modified for PM to make effective use of cachelines.

Source Codes: <http://github.com/DICL/CCEH>

Question?

