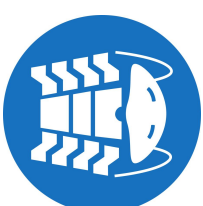
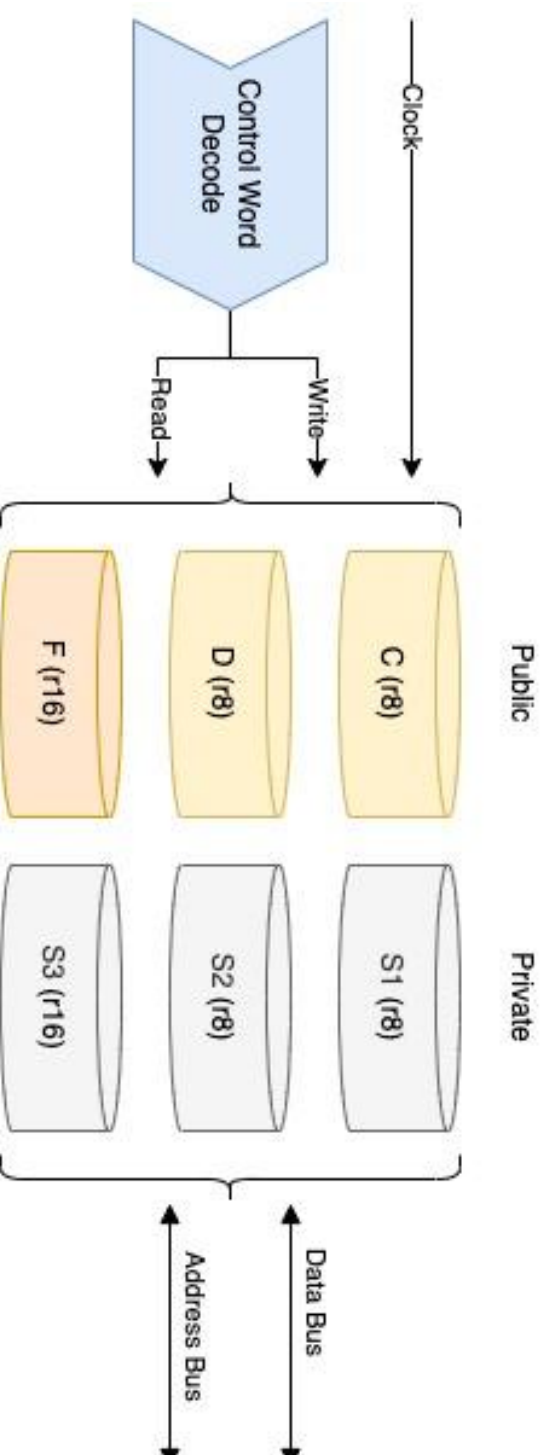


General Purpose Registers (GPR)



The Trilobyte CPU contains **two 8-bit general-purpose registers** and **one 16-bit general-purpose counter register** that is available for user control. The GPR module itself contains an additional two 8-bit scratch registers and one 16-bit scratch register.

Power: **5V Vcc**



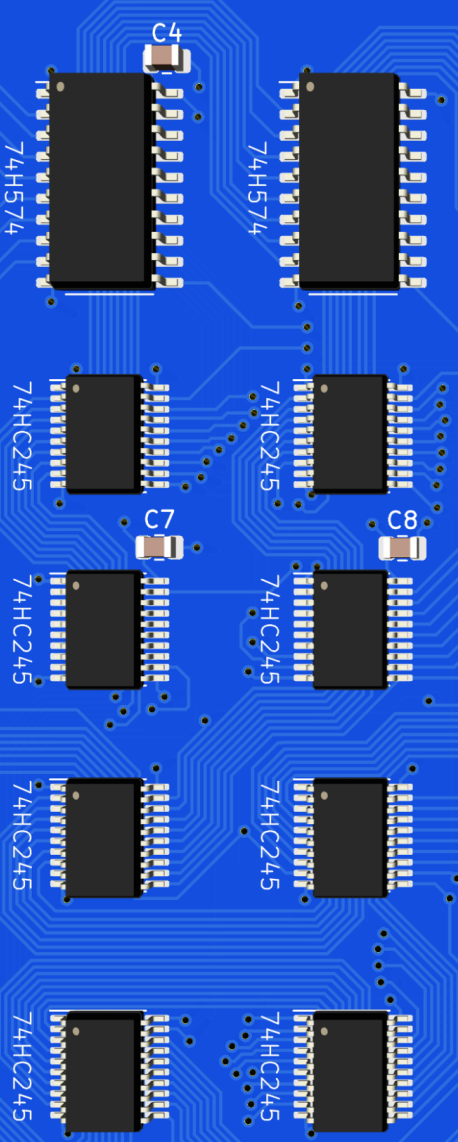
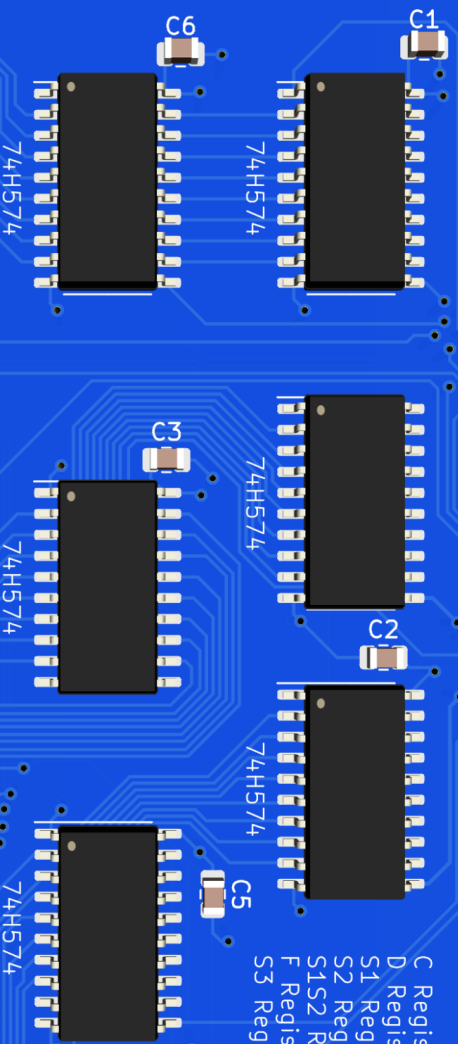
General Purpose Registers

- Vcc
- Gnd
- CP
- C7
- C6
- C5
- C4
- C3
- C2
- C1
- C0

— Read — Write —



- C Register (8)
- D Register (8)
- S1 Register (8)
- S2 Register (8)
- S1S2 Register (16)
- F Register (16)
- S3 Register (16)



- B0
- B1
- B2
- B3
- B4
- B5
- B6
- B7

- A0
- A1
- A2
- A3
- A4
- A5
- A6
- A7
- A8
- A9
- A10
- A11
- A12
- A13
- A14
- A15

Register

Name	Size	Visibility	Mnemonic
C	8-bit	PUBLIC	r, r8
D	8-bit	PUBLIC	r, r8
F	16-bit	PUBLIC	r, r16
S1	8-bit	PRIVATE	r, r8
S2	8-bit	PRIVATE	r, r8
S3	16-bit	PRIVATE	r, r16

Bus Connections

- C, D: Loads and asserts data from/to the 8-bit data bus
- F: Loads and asserts data from/to the 16-bit data bus
- S1: Loads and asserts data from/to the 8-bit data bus, as well as, asserts its data to the LSB of the 16-bit address bus.
- S2: Loads and asserts data from/to the 8-bit data bus, as well as, asserts its data to the MSB of the 16-bit address bus.
- S3: Loads and asserts data from/to the 16-bit data bus, as well as, asserts its MSB, or LSB to the 8-bit data bus.
- S1S2: Asserts register-pair to the 16-bit data bus



Control & Instructions

Description	C7	Control [0..6]	Hex Code
Reset / Load ALL	0	0000_000	0x0
Load C	1	0000_001	0x81
Load D	1	0000_010	0x82
Load S1	1	0000_011	0x83
Load S2	1	0000_100	0x84
Load F	1	0000_101	0x85
Load S3	1	0000_110	0x86
Assert C	1	0001_000	0x88
Assert D	1	0010_000	0x90
Assert S1	1	0011_000	0x98
Assert S2	1	0100_000	0xa0
Assert S1S2	1	0101_000	0xa8
Assert F	1	0110_000	0xb0



Assert S3	1	0111_000	0xb8
Assert S3L	1	1000_000	0xc0
Assert S3H	1	1001_000	0xc8
MOV C, D	1	0010_001	0x91
MOV C, S1	1	0011_001	0x99
MOV C, S2	1	0100_001	0xa1
MOV C, S3L	1	1000_001	0xc1
MOV C, S3H	1	1001_001	0xc9
MOV D, C	1	0001_010	0x8a
MOV D, S1	1	0011_010	0x9a
MOV D, S2	1	0100_010	0xa2
MOV D, S3L	1	1000_010	0xc2
MOV D, S3H	1	1001_010	0xca
MOV S1, C	1	0001_011	0x8b
MOV S1, D	1	0010_011	0x9a



MOV S1, S2	1	0100_011	0x93
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8bit & 16bit C8, D8, S18, S28, S1S216, F16, S316

Control Bus

- 11: VCC
- 10: GND
- 9: RESET
- 8: CS
- 7: ALE
- 6: PSEN
- 5: RST/WD
- 4: CS
- 3: ALE
- 2: PSEN
- 1: RST/WD

Data Bus

- 17: BUS7
- 16: BUS6
- 15: BUS5
- 14: BUS4
- 13: BUS3
- 12: BUS2
- 11: BUS1
- 10: BUS0

Address Bus

- 29: ADDR15
- 28: ADDR14
- 27: ADDR13
- 26: ADDR12
- 25: ADDR11
- 24: ADDR10
- 23: ADDR9
- 22: ADDR8
- 21: ADDR7
- 20: ADDR6
- 19: ADDR5
- 18: ADDR4
- 17: ADDR3
- 16: ADDR2
- 15: ADDR1
- 14: ADDR0

Smoothing Caps

Logic Gate Power

All Registers will reset when CONTROL goes LOW and there is a rising edge of the clock.

74HC574

74HC574

Figure 1. Schematic representation of the experimental design. The figure is divided into two main sections, (a) and (b), each showing a timeline of events for two groups: ZINC-25 and ZINC-25+.

(a) ZINC-25 and ZINC-25+ groups:

- ZINC-25 (Control):** Includes a 14-day period of 100% NDC (No Direct Contact) and a 14-day period of 100% DND (Direct Noisy Drive).
- ZINC-25+ (Intervention):** Includes a 14-day period of 100% NDC and a 14-day period of 100% DND.

(b) ZINC-25 and ZINC-25+ groups:

- ZINC-25 (Control):** Includes a 14-day period of 100% NDC and a 14-day period of 100% DND.
- ZINC-25+ (Intervention):** Includes a 14-day period of 100% NDC and a 14-day period of 100% DND.

The figure illustrates the experimental design for the ZINC-25 and ZINC-25+ groups, showing the timeline of events and the duration of the intervention.

Figure 1 illustrates the four-step synthesis of poly(arylene ether)s. The reaction involves the polycondensation of 4,4'-dichlorodiphenyl ether (1) with various diamines (2) to form poly(arylene ether)s (3). The diamines used are: (a) 4,4'-diaminodiphenyl ether, (b) 4,4'-diaminodiphenyl sulfone, (c) 4,4'-diaminodiphenyl ether, and (d) 4,4'-diaminodiphenyl ether. The resulting polymers are: (a) poly(4,4'-oxydiphenylene), (b) poly(4,4'-oxydiphenylene sulfone), (c) poly(4,4'-oxydiphenylene ether), and (d) poly(4,4'-oxydiphenylene ether). The reaction conditions are: (a) 180°C, 12h, N₂; (b) 180°C, 12h, N₂; (c) 180°C, 12h, N₂; (d) 180°C, 12h, N₂.

F Register

Pin 20: VCC

Pin 19: 74HC274

Pin 18: A0/A0B0

Pin 17: A1/A0B1

Pin 16: A2/A0B2

Pin 15: A3/A0B3

Pin 14: A4/A0B4

Pin 13: A5/A0B5

Pin 12: A6/A0B6

Pin 11: A7/A0B7

Pin 10: A8/A0B8

Pin 9: A9/A0B9

Pin 8: A10/A0B10

Pin 7: A11/A0B11

Pin 6: A12/A0B12

Pin 5: A13/A0B13

Pin 4: A14/A0B14

Pin 3: A15/A0B15

Pin 2: A16/A0B16

Pin 1: A17/A0B17

Pin 0: GND

Pin 18: VCC

Pin 17: 74HC274

Pin 16: A0/A0B0

Pin 15: A1/A0B1

Pin 14: A2/A0B2

Pin 13: A3/A0B3

Pin 12: A4/A0B4

Pin 11: A5/A0B5

Pin 10: A6/A0B6

Pin 9: A7/A0B7

Pin 8: A8/A0B8

Pin 7: A9/A0B9

Pin 6: A10/A0B10

Pin 5: A11/A0B11

Pin 4: A12/A0B12

Pin 3: A13/A0B13

Pin 2: A14/A0B14

Pin 1: A15/A0B15

Pin 0: GND

Pin 18: VCC

Pin 17: 74HC274

Pin 16: A0/A0B0

Pin 15: A1/A0B1

Pin 14: A2/A0B2

Pin 13: A3/A0B3

Pin 12: A4/A0B4

Pin 11: A5/A0B5

Pin 10: A6/A0B6

Pin 9: A7/A0B7

Pin 8: A8/A0B8

Pin 7: A9/A0B9

Pin 6: A10/A0B10

Pin 5: A11/A0B11

Pin 4: A12/A0B12

Pin 3: A13/A0B13

Pin 2: A14/A0B14

Pin 1: A15/A0B15

Pin 0: GND

[illegible]

To just ASSERT or LOAD a value to the data bus to be used with external modules, just select a single value from either READ or WRITE.

To do a GPR to GPR transfer just select a READ and WRITE control word and then OR them together.

To do a RESET, CONTROL7 is set LOW and all data buses are set to 0x0, which causes each register to load the value presented on their data bus.

MOV R, *	MOV *, R
0x81: LDC	0x80: NOP
0x82: LDD	0x86: CO
0x83: LDSI	0x90: DO
0x84: LDS2	0x98: SIOB
0x85: LDF	0xa0: S2OB
0x86: LDS3	0xa8: S1S2O
	0xb0: FO
	0xb8: S3O
	0xc0: S3LOB
	0xc8: S3HOB

MOV C, D	0x91	(b1,010,00,01)
MOV C, S1	0x99	(b1,010,00,01)
MOV C, S2	0x81	(b1,010,00,01)
MOV C, S15B	0x91	(b1,010,00,01)
MOV C, S15SB	0x99	(b1,100,00,01)
MOV D, C	0x91	(b1,100,00,01)
MOV D, C1	0x8a	(b1,001,01,01)
MOV D, S1	0x9a	(b1,001,01,01)
MOV D, S2	0x82	(b1,010,01,01)
MOV D, S15B	0x92	(b1,001,00,01)
MOV D, S15SB	0x9a	(b1,100,01,01)
MOV S1, C	0x8b	(b1,001,00,01)
MOV S1, D	0x9a	(b1,001,01,01)

MOV C, D	0x91	0b01_0010_001
MOV C, S1	0x99	0b01_0011_001
MOV C, S2	0xa1	0b01_0100_001
MOV C, S3	0xc1	0b01_1000_001
MOV C, S3	0xc1	0b01_1001_001
MOV D, C	0xb8	0b01_0001_010
MOV D, S1	0x9a	0b01_0011_010
MOV D, S2	0xa2	0b01_0100_010
MOV D, S3	0xc2	0b01_1000_010
MOV D, S3	0xc2	0b01_1001_010
MOV S1, C	0xb0	0b01_0001_011
MOV S1, D	0x9a	0b01_0010_011

[illegible]

Parts & Components List

Digital Logic, IC's

Part #	Description	Qty	Datasheet	Link
74HC574	8-Bit, Edge-Triggered, flip-flops	7	DATA	Mouser
74HC245	8-bit, Tri-State Transceiver	8	DATA	Mouser
74HC00	Quad, 2-input NAND gates	2	DATA	Mouser
74HC138	3 to 8 line, decoder	2	DATA	Mouser
-	Ceramic Capacitor	8	-	-
-	Resistor (Pull U/D)	1	-	-
-	Header Pins	-	-	-

