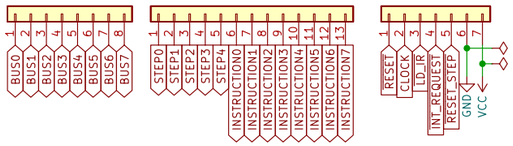
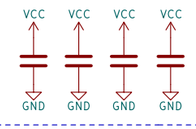
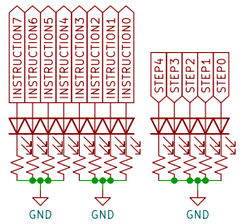
Instruction / Step Counter

CPU Connections



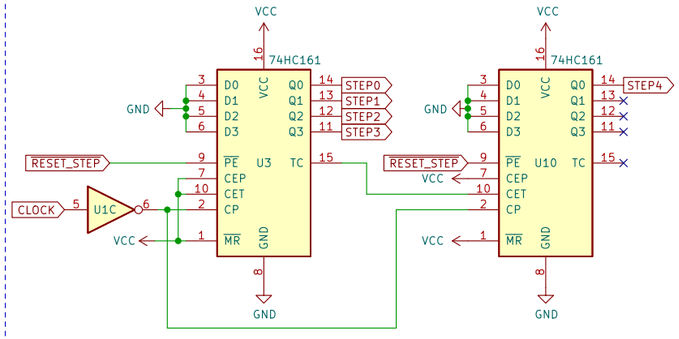
Smoothing Caps



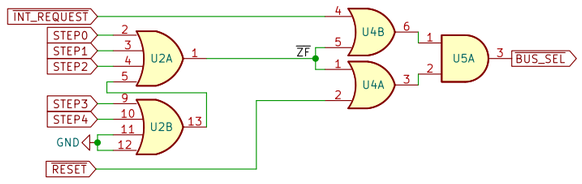


STEP COUNTER

Each instruction can have up to 32 steps

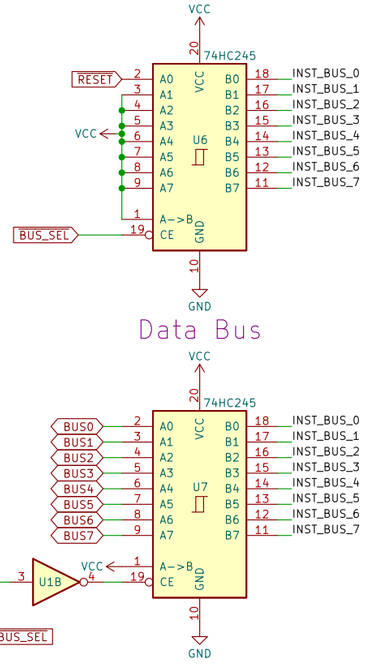


Bus Select Logic

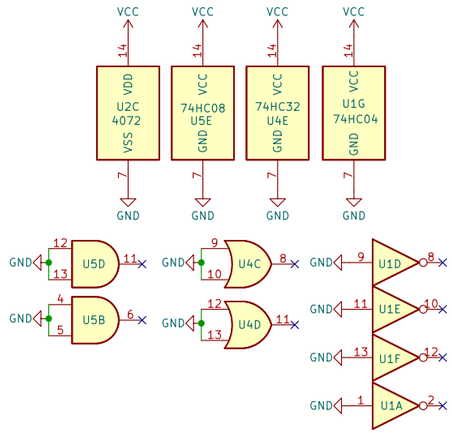


Instruction Bus

Hardwired Addresses Bus



Logic Gate Power



An instruction address can come from two places:
1. 8-bit Memory/Data Bus
2. Hardwired Address

When the Step counter is at 0x0, a $\overline{ZF}$ (zero flag) is set to active and is OR'ed with the inputs from $\overline{INT\_REQUEST}$ AND $\overline{RESET}$

If either $\overline{INT\_REQUEST}$ or $\overline{RESET}$ are `low`, and Zero Flag is LOW, then $\overline{LD\_INT\_VECTOR}$ is LOW. This causes the Instruction Source to switch to the hardwired addresses.

When a hardwired address is used, it is 0xff or 0xfe with the LSB being the current value of $\overline{RESET}$.

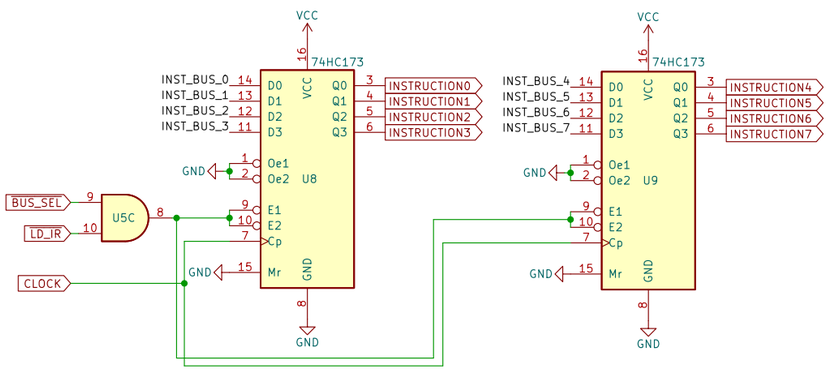
$\overline{RESET}$ Has the higher priority than $\overline{INT\_REQUEST}$ so if both are active, then reset operation is executed

0b11111111// 0xFF (Interupt Opcode)
0b11111110// 0xFE (RESET Opcode)

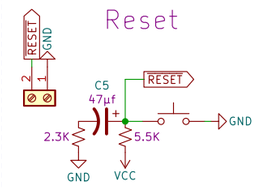
TRUTH TABLE

ZF	RESET	IRQ	SEL	DESC
1	nc	nc	1	Bus Data Asserted
0	1	1	1	Bus Data Asserted
0	0	nc	0	0xFE Asserted (Reset)
0	1	0	0	0xFF Asserted (IRQ Handler

Instruction Register



Reset



Reset RC circuit starts at logic level LOW for about a half a second. This ensures the CPU enters the reset mode on power-up

Trilobyte CPU

Sheet: /
File: inst-step-irq-decode.kicad_sch

Title: Instruction Register & Step Counter

Size: User	Date: 2022-07-20	**Rev: v1.0.0**
KiCad E.D.A. kicad (6.0.0-0)		Id: 1/1