

MEMORY MODULE w/segments

32K ROM | 2M RAM

ROM \$0000 - \$7FFF
RAM \$8000 - \$200000

Contents of this module include the following:

- 16-bit Memory Address Register (MAR)
- Memory Segments: Data, Code, Stack segments (DS, CS, SS)
- EEPROM & RAM

ROM address space is 15bits wide
RAM address space is 19bits wide

Since there is only 16bits in the MAR for addressing, the following logic explains how chip are selected:

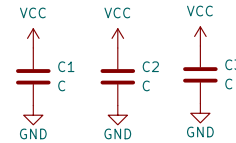
- If any segment is HIGH, or A15 is HIGH then EEPROM is disabled
- Otherwise, EEPROM is active and uses READ only
- The SEGMENT[0..2]'s are used to fill address space 16, 17, & 18
- SEGMENT[3,4] is decoded into 4 values and is used to target different RAM chips

Segment registers are loaded from the shared 8bit bus and can also be asserted back onto the BUS. A reason for asserting is so you can {push ds} onto the stack to store them during interrupts

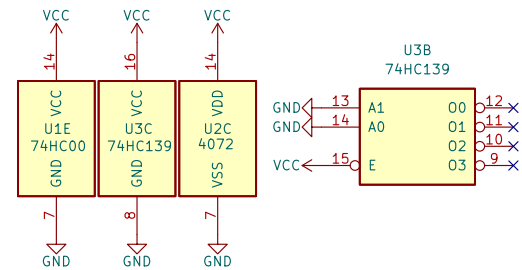
Addressing Key:
S: SEGMENT[3,4]
s: SEGMENT[0..2]
a: MAR[0..15]

0b_SS_sss_aaaa_aaaa_aaaa_aaaa

Smoothing Caps

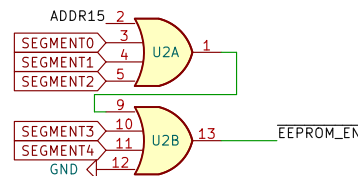


Logic Gate Power

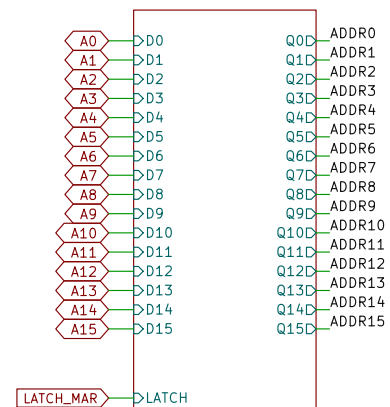


EEPROM ENABLE LOGIC

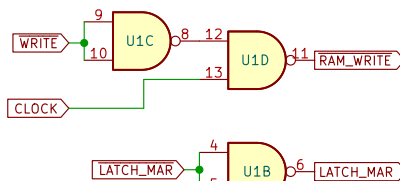
If any of the following is HIGH
segment[0..4] or A16
Then EEPROM access is disabled



Memory Address Register

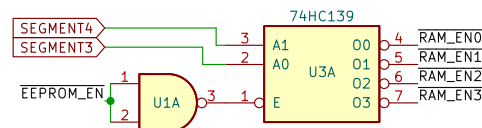


Control Logic Active High/Lows

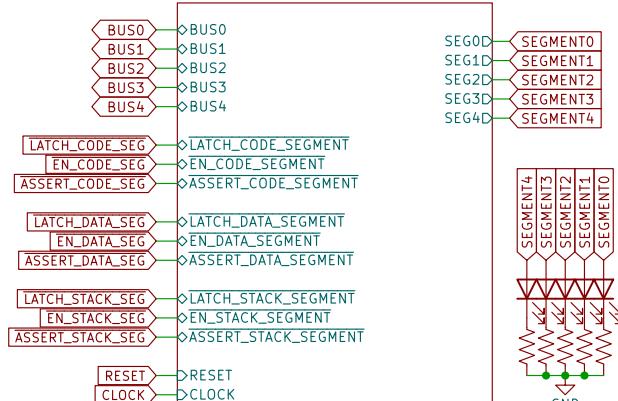


RAM SELECT LOGIC

If EEPROM is HIGH (disabled) then this MUX is enabled, it then uses SEGMENT[3,4] to choose a RAM enable line

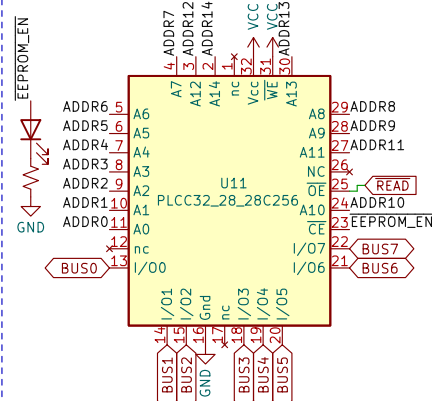


Data Segments



File: data-segments.kicad_sch

EEPROM



RAM Array



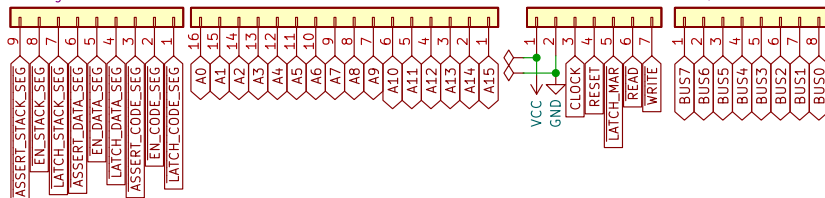
File: ram-array.kicad_sch

Segment Control

Address Bus

Mem Control

I/O Data Bus



RAM \$8000 - \$20000

ROM \$0000 - \$7fff

32K ROM | 2M RAM

Trilobyte - theWickedWebDev/8-bit-computer

Sheet: /

File: memory.kicad_sch

Title: Memory Module

Size: User Date: 2020-03-11

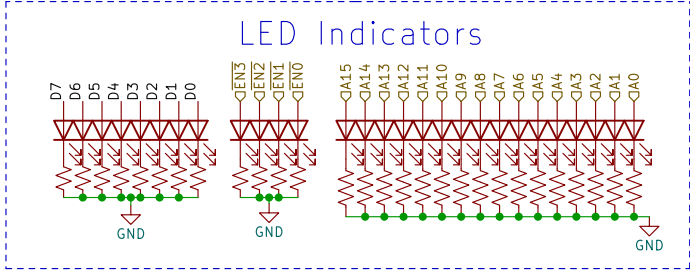
KiCad E.D.A. kicad (6.0.0-0)

Rev: 1.6

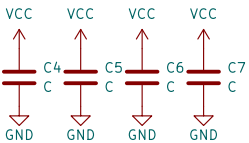
Id: 1/7

RAM Array Module

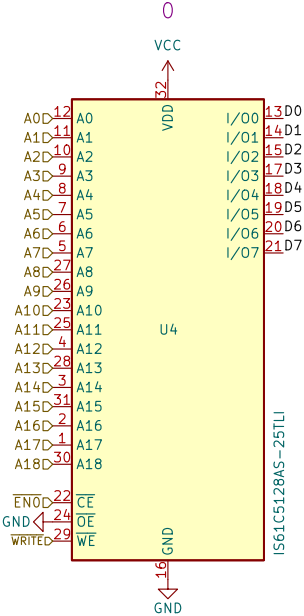
LED Indicators



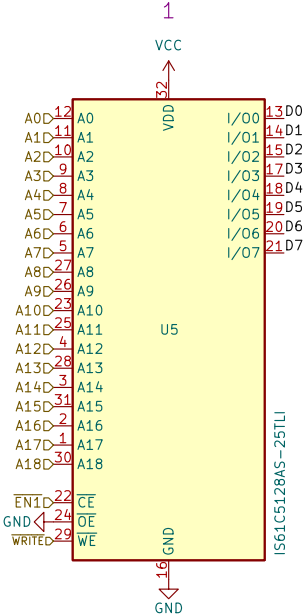
Smoothing Caps



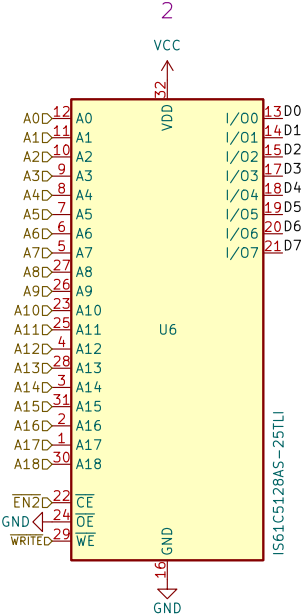
SRAM 512k



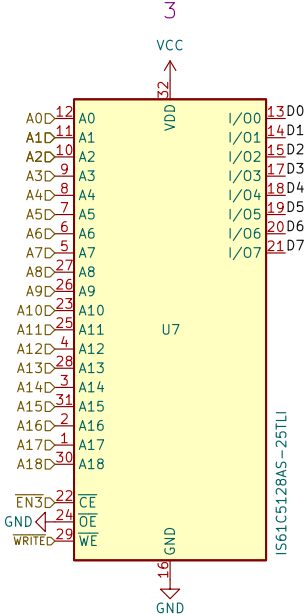
SRAM 512k



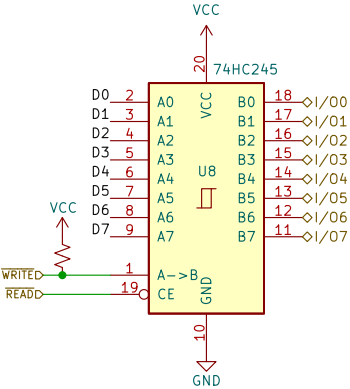
SRAM 512k



SRAM 512k



Data BUS Trceiver



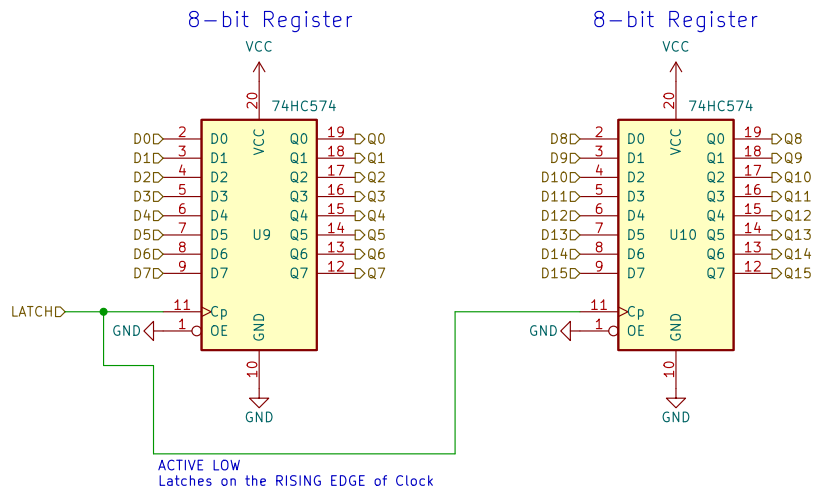
Sheet: /RAM Array/
File: ram-array.kicad_sch

Title:

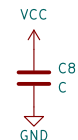
Size: User Date:
KiCad E.D.A. kicad (6.0.0-0)

Rev:
Id: 2/7

MEMORY ADDRESS REGISTER



Smoothing Cap



Sheet: /Memory Address Register/
File: MAR.kicad_sch

Title:

Size: A5
KiCad E.D.A. kicad (6.0.0-0)

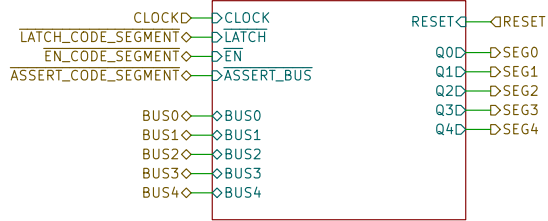
Date:

Rev:

Id: 3/7

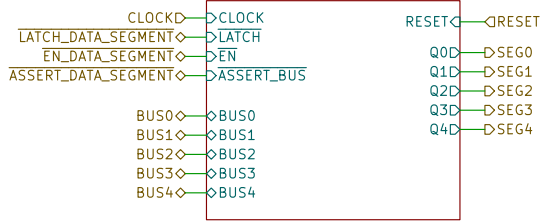
Segments

Code Segment



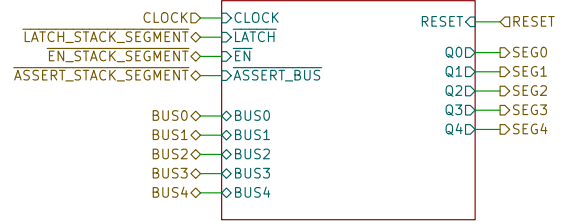
File: segment-register.kicad_sch

Data Segment



File: segment-register.kicad_sch

Stack Segment



File: segment-register.kicad_sch

Sheet: /Data Segments/
File: data-segments.kicad_sch

Title:

Size: User

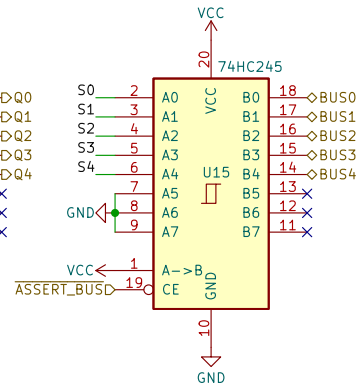
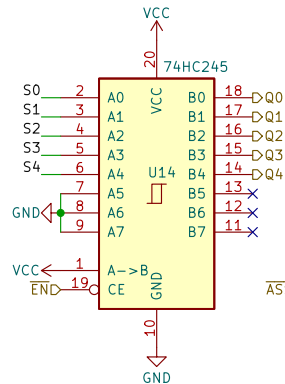
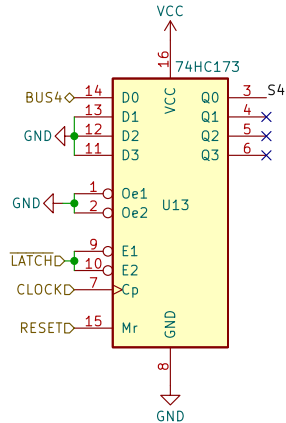
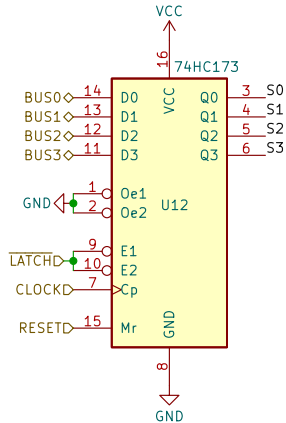
Date:

Rev:

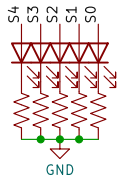
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Id: 5/7

Segment Registers: Data, Code & Stack



LED Indicators



Sheet: /Data Segments/Data Segment/
File: segment-register.kicad_sch

Title:

Size: A5 Date:
KiCad E.D.A. kicad (6.0.0-0)

Rev:

Id: 6/7