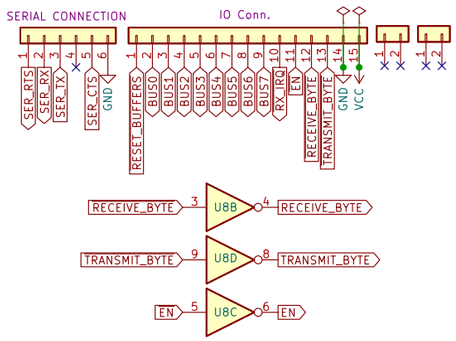
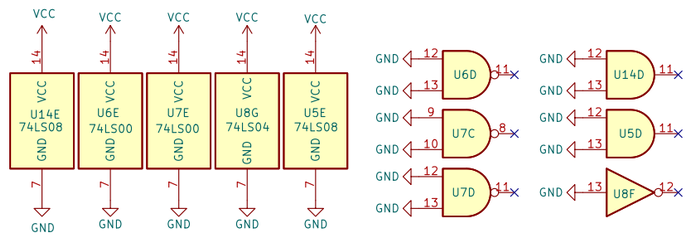
UART – SERIAL PORT MODULE

(2) 64x8 FIFO BUFFERS // TX and RX

CONNECTIONS



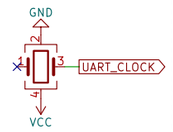
LOGIC GATE



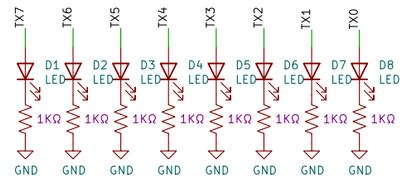
CLOCK

1MHz

62500 Baudrate



LED INDICATORS



$\overline{RX\_IRQ}$ – When LOW, there is no more data in buffer to read

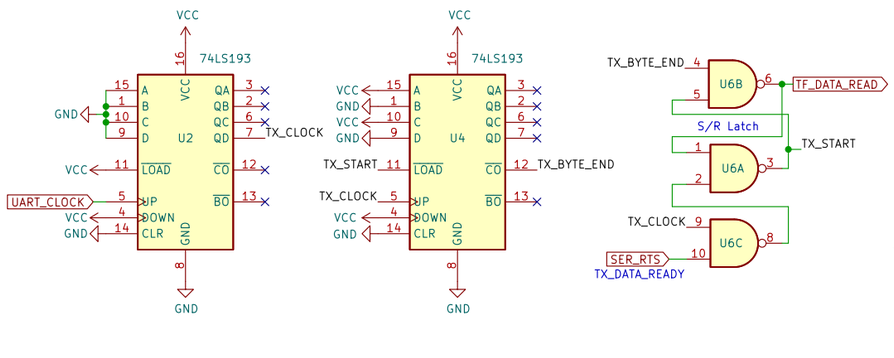
RECEIVE_BYTE – LOW to HIGH transition, asserts a byte onto data bus from the RX buffer

$\overline{TX\_BUFF\_FULL}$ – When LOW, there is no room in tx buffer, if HIGH there is more roon to transmit

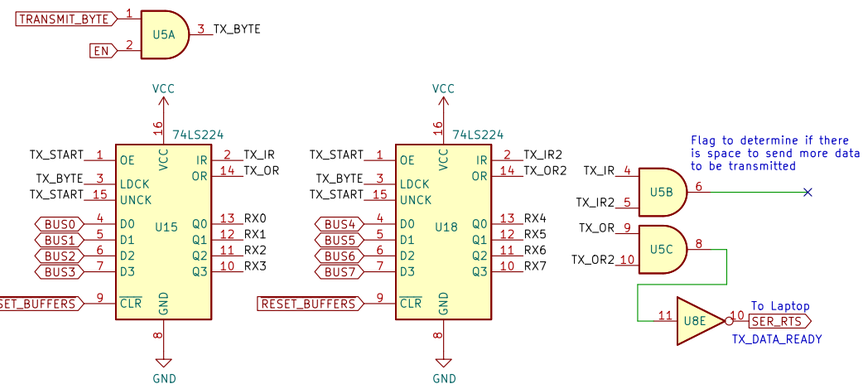
TRANSMIT_BYTE – LOW to HIGH transition sends byte from data bus to the TX buffer

$\overline{RESET\_BUFFERS}$ – When LOW all FIFO buffers are reset

SERIAL TRANSMIT DATA

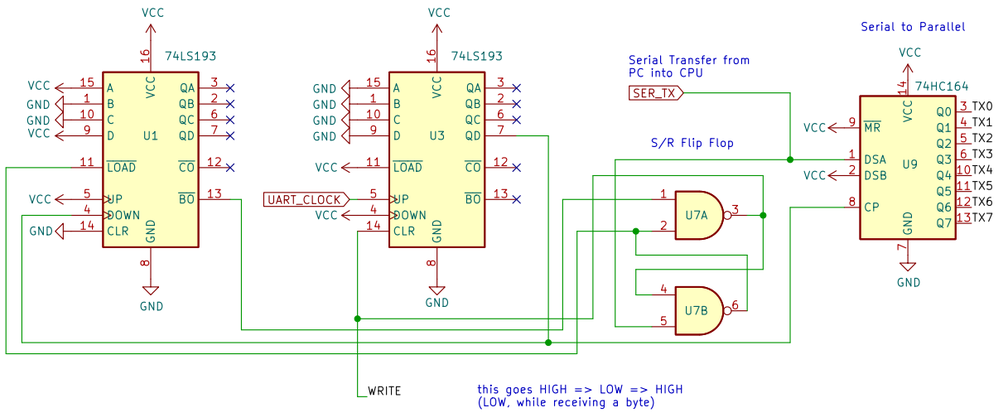


TRANSMIT FIFO

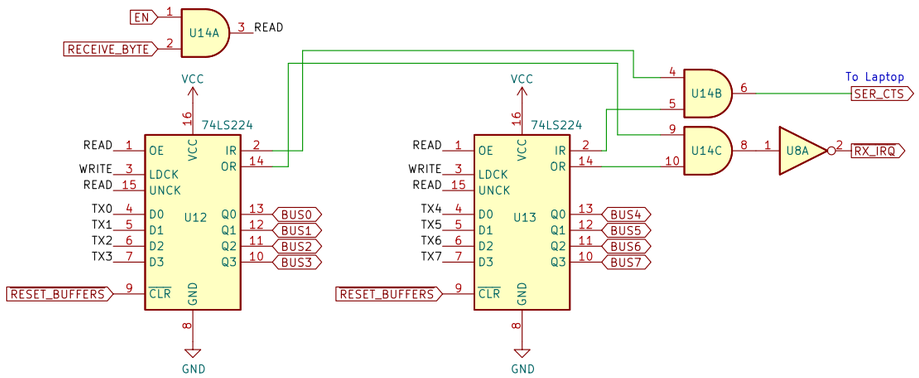


SERIAL RECEIVE DATA

Counts down from 9 to 0, which then triggers a $\overline{BO}$ borrow. This signal is then sent to the SR Flip-Flop which resets this counter to 0x9 again, as well as CLR clears the next counter.



RECEIVE FIFO



Transmit & Receive w/ FIFO Buffers

theWickedWebDev/8-bit-computer

Sheet: /

File: UART.kicad_sch

Title: Serial Port (UART)

Size: User	Date: 2022-02-10	**Rev: V1**
KiCad E.D.A. kicad (6.0.0-0)		Id: 1/1