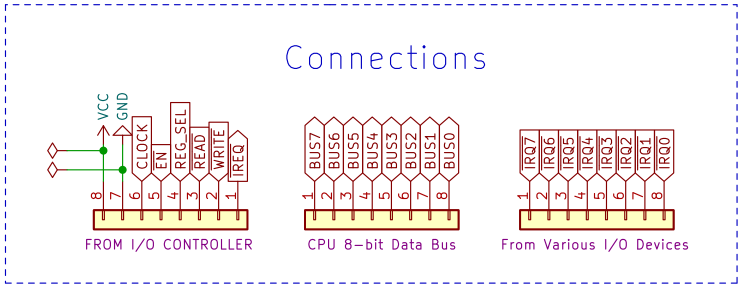
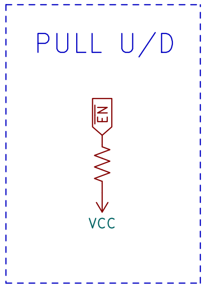
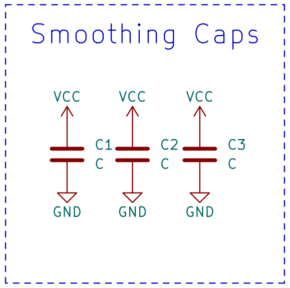
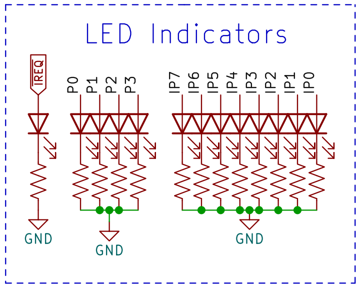
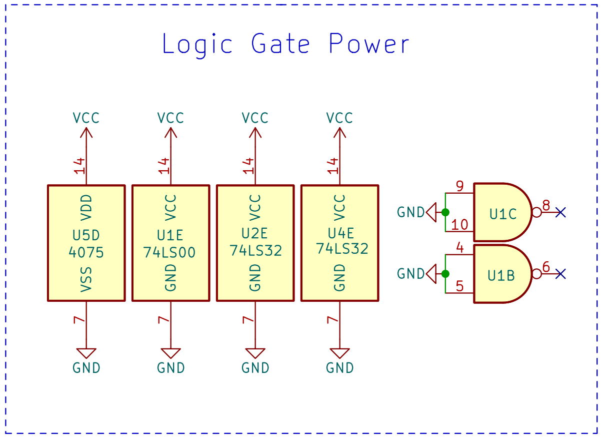
INTERRUPT REQUEST HANDLER

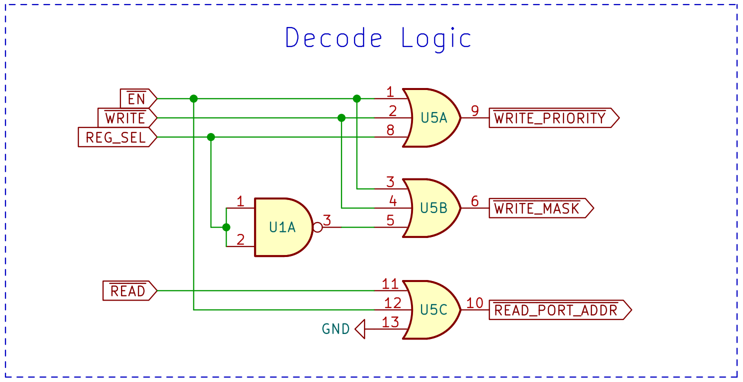


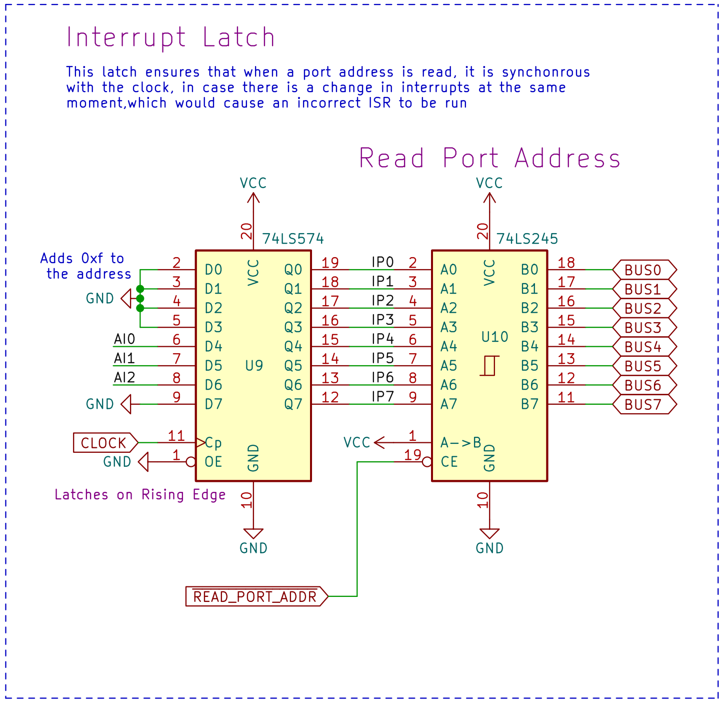




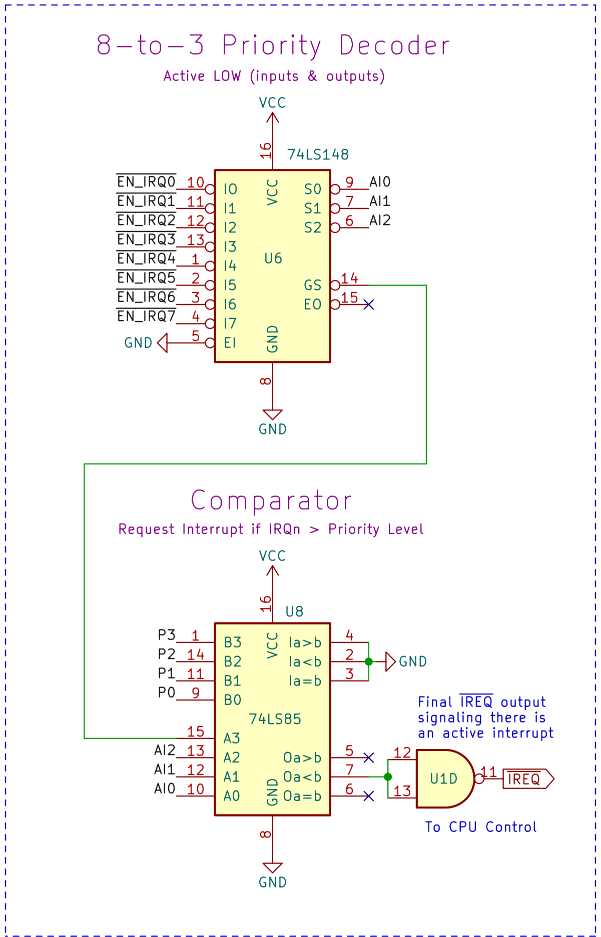


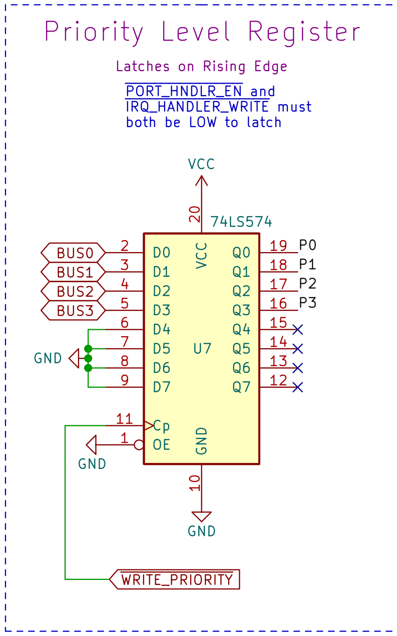


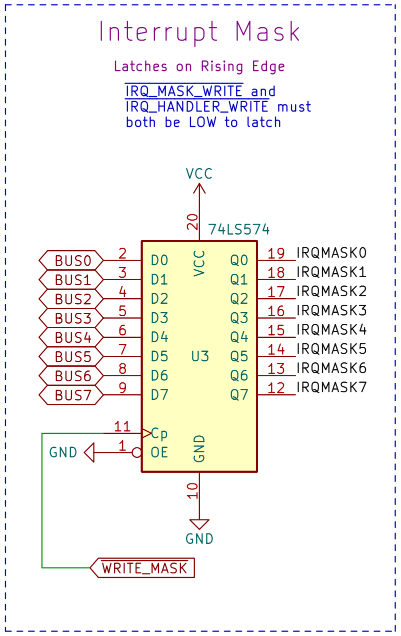


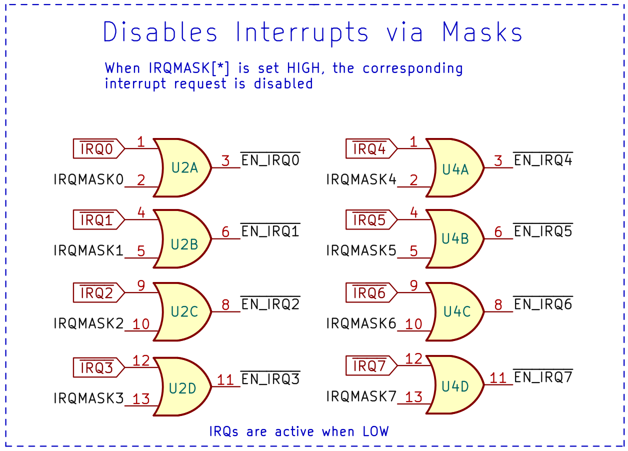


This latch ensures that when a port address is read, it is synchonrous with the clock, in case there is a change in interrupts at the same moment,which would cause an incorrect ISR to be run






Interrupt Mask
Latches on Rising Edge
IRQ_MASK_WRITE and IRQ_HANDLER_WRITE must both be LOW to latch
VCC
74LS574
BUS0 BUS1 BUS2 BUS3 BUS4 BUS5 BUS6 BUS7
IRQMASK0 IRQMASK1 IRQMASK2 IRQMASK3 IRQMASK4 IRQMASK5 IRQMASK6 IRQMASK7
U3
GND
WRITE_MASK


Disables Interrupts via Masks
IRQ0 IRQMASK0 U2A EN_IRQ0
IRQ1 IRQMASK1 U2B EN_IRQ1
IRQ2 IRQMASK2 U2C EN_IRQ2
IRQ3 IRQMASK3 U2D EN_IRQ3
IRQ4 IRQMASK4 U4A EN_IRQ4
IRQ5 IRQMASK5 U4B EN_IRQ5
IRQ6 IRQMASK6 U4C EN_IRQ6
IRQ7 IRQMASK7 U4D EN_IRQ7
IRQs are active when LOW

When IRQMASK[*] is set HIGH, the corresponding interrupt request is disabled

MASK LOGIC

Active LOW IRQn
Active HIGH MASKn

If either of these are HIGH then then that interrupt is disabled/inactive

IREQ's are OR'ed with the mask bits

IRQ Example Assembly

```
IRQPORT: 0x0
IRQMASKPORT: 0x1

SETUP_IRQ:
    # Enables two IREQs
    OUT IRQMASKPORT, 0b0111111

    # Sets priority level to all
    OUT IRQPORT, 0x8

IRQ:
    PUSH CS
    IN S1, IRQPORT
    JMPF (0:s1)
```

Interrupt Vector Table

$0:00f0: IRQ0
$0:00f1: IRQ1
$0:00f2: IRQ2
$0:00f3: IRQ3
$0:00f4: IRQ4
$0:00f5: IRQ5
$0:00f6: IRQ6
$0:00f7: IRQ7

PRIORITY LOGIC

IRQ7 – Highest Priority
IRQ0 – Lowest Priority

If the curent Interrupt address from the Priority Decoder output has a priority higher than the Priority Level, then an IREQ is triggered

Priority Examples

A value of 8 written to the priority latch will enable all interrupts.
A value of 5 written to the priority latch will enable IQR0 – IRQ4. IRQ5 – IRQ7 will be disabled.
A value of 3 written to the priority latch will enable IQR0 – IRQ2. IRQ3 – IRQ7 will be disabled.
A value of 0 written to the priority latch will disable all interrupts.

Pinout Description

IREQ – (output) Signals to the CPU there is an interrupt

WRITE – (input) Trigers a latch on a register. Used in conjunction with INT_PORT_REQ and either PORT_HNDLR_EN or IRQ_MASK_WRITE

READ – (input) Triggers a latch on the Interrupt Port Register and asserts its value onto the bus. Only when PORT_HNDLR_EN is LOW.

ADDR[4,5] – (input) Used to select Mask or Priority registers

INT_PORT_EN – (input) Enable all functionality on LOW signal

w/ Priority Level Register & Mask Register
theWickedWebDev/8-bit-computer
Sheet: /
File: new-interrupt-handler.kicad_sch
Title: Interrpt Request Handler Module

Size: User	Date: 2022-02-10	**Rev: v6**
KiCad E.D.A. eeschema (6.0.0-0)		Id: 1/1