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ASSIGNMENT 1

Ans 1- Shift registers are digital memory circuitry found in devices such as calculators, computers and data processing systems. With the shift register, data or bits are entered into the system in a serial or parallel manner. They enter from one direction and as more data is added, shift operations until they point the output end.

Type of shift registers :

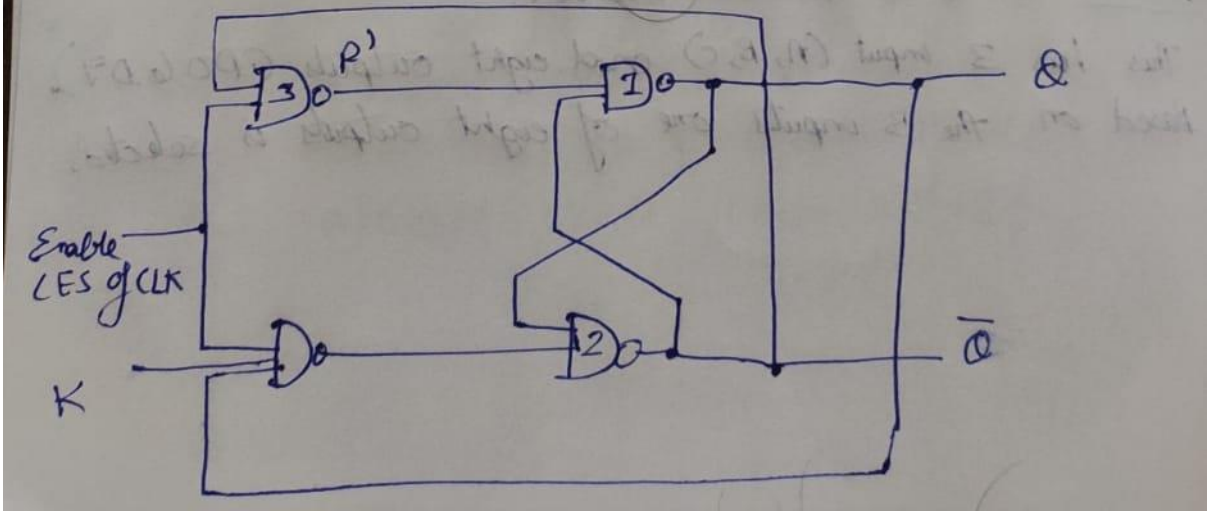
1) SISO : This shift operator allows serial input and generate a serial output, so this is named as SISO or Serial in Serial out shift registers. Because there is just one output, and a time the data leaves the register one bit in a serial manner.

2) SIPO : The shift register allows serial input and generates a parallel output, so this is known as serial in parallel out.

3) PISO : The shift register allows parallel input and generate a serial output, so this is known as parallel in serial out.

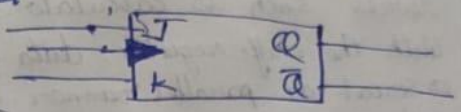
4) PIPO : The shift register, which allows parallel input / data is given seperately to each flip flop and in a simultaneous manner and also produces a parallel output is known as parallel in parallel out

Ans 2: JK flip flop



The characteristic table is useful during analysis of sequential circuits when the value of a flip-flop inputs are known and we want to find the value of the flip flop output Q after the rising edge of the clock signal.

Truth table :



Inputs		Output	
J	K	Q_n (Present State)	Q_n (Next State)
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

$$Q_{n+1} = Q_n'(JK + JK') + Q_n(JK' + JK)$$

$$Q_{n+1} = Q_n' J + Q_n K'$$

Ans 3: 3 to 8 ~~Decoder~~ Decoder :

This has 3 input (A, B, C) and eight outputs (D0 to D7). Based on the 3 inputs one of eight outputs is selected.

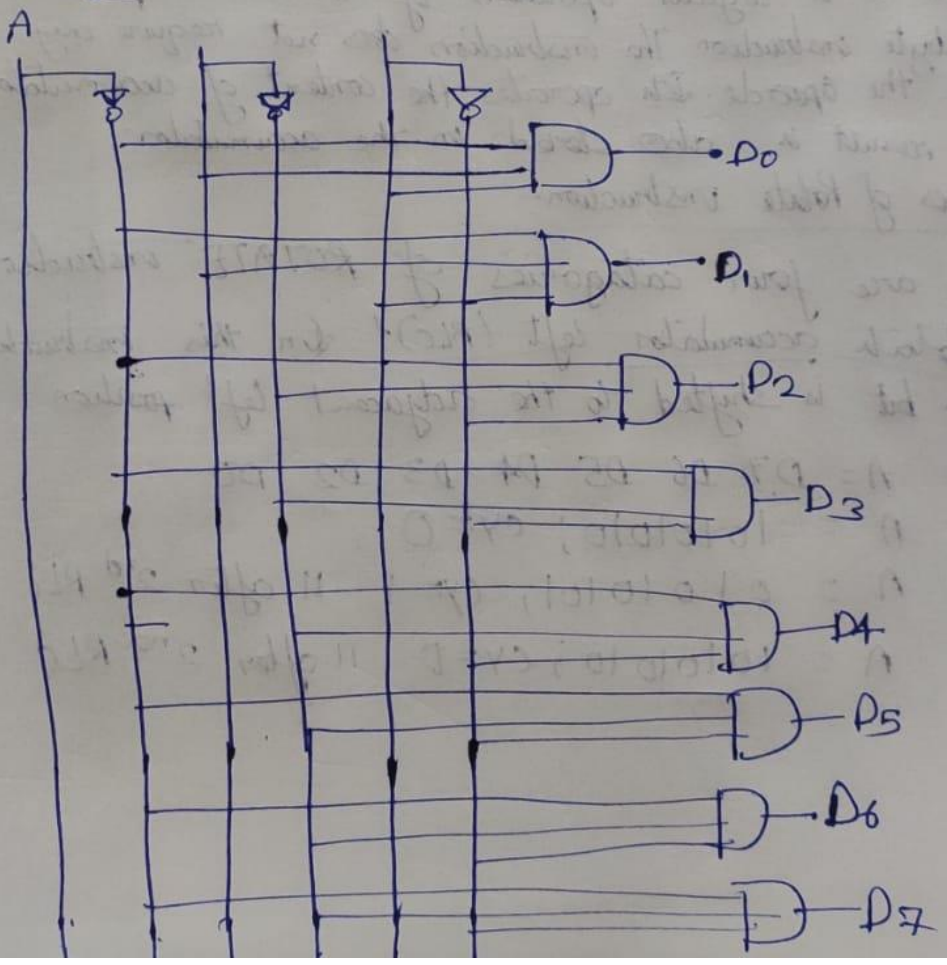
Truth Table

A	B	C	D0	D1	D2	D3	D4	D5	D6	D7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

$D_0 = \bar{A}\bar{B}\bar{C}$ $D_2 = \bar{A}B\bar{C}$ $D_4 = A\bar{B}\bar{C}$ $D_6 = AB\bar{C}$

$D_1 = \bar{A}\bar{B}C$ $D_3 = \bar{A}BC$ $D_5 = A\bar{B}C$ $D_7 = ABC$

logic Diagram :



Ans 4:- 1) No of address lines = 16384
2) No of data lines = 8
3) No of registers = 16k
4) No of memory cell = 112
5) No of chips = 48K × 4 bits RAM

Ans 5:- A Kilobyte (KB) is 1000 bytes
A Megabyte (MB) is 1000 KB
A Gigabyte (GB) is 1000 MB
A Terabyte (TB) is 1000 GB
A Petabyte (PB) is 1000 TB

Ans 6:- Rotate Instructions in 8085:-
Rotate is a logical operation of 8085 microprocessor. It is a 1 byte instruction. The instruction does not require any operand after the opcode. It operates the content of accumulator. The result is also stored in the accumulator.

Types of Rotate instruction:-
There are four catagories of ROTATE instruction.
1) Rotate accumulator left (RLC):- In this instruction, each bit is shifted to the adjacent left position.

e.g A = D7 D6 D5 D4 D3 D2 D1 D0
A = 10101010; CY=0
A = 01010101; CY=1 // after 2nd RLC
A = 10101010; CY=0 // after 2nd RLC

(2) Rotate accumulator left through carry (RAL) -

In this instruction, each bit is shifted to the adjacent left position.

eg: A = D7 D6 D5 D4 D3 D2 D0

A = 10101010; CY = 0
A = 01010100; CY = 1 // after 1st RAL
A = 10101001; CY = 0 // after 2nd RAL

(3) Rotate accumulator right (RRC) -

In this instruction, each bit is shifted to adjacent right position

eg: A = D7 D6 D5 D4 D3 D2 D0

A = 10000001; CY = 0
A = 11000000; CY = 1 // after 1st RRC
A = 01100000; CY = 0 // after 2nd RRC.

(4) Rotate accumulator right through carry (RAR) -

In this instruction, each bit is shifted to the adjacent right position

eg: A = D7 D6 D5 D4 D3 D2 D0

A = 10000001; CY = 0
A = 01000000; CY = 1 // after 1st RAR
A = 10100000; CY = 0 // after 2nd RAR.

Shift registers : There are 4 types of shift registers :

(1) Shift Right (SHR) : The instruction simply shifts the mentioned bits in the register to the right one by one by inserting the same number.

eg: SHR AX, 2 .

(2) Shift Arithmetic Right (SAR) : This instructions shifts the mentioned bits in the register to the right side by one by one, but instead of inserting the zeroes from left end, the MSB is restored.

eg : SAR BX, 5

(3) Shift left (SHL) : The SHL shifts the mentioned bits in the register to the left side one by one by inserting the same no. of zeroes from right end.

eg : SHL AX, 2 .

(4) Shift Arithmetic left (SAL) : This instruction is same as SHL.

eg : SAL CL, 2

Ans 7: (a) #OAG 2000
LDA 2050
MOV H,A
LDA 2051
ADD H
MOV L,P
MVIA 00
ADC A
MOV H,A
SHLD 3050
HLT
#ORG 3000H
DB 23H, 35H

(b) #ORG 2000H
MVI G00
LHCD 2500
MOV A,H
SOB L
DNL 200B
JNR C
STA 2502
MOV A,C
SIA 2503
HLT
#ORG 2500M
DB 49H, 24H

(c) #ORG 5000H

```
MUJ D,00
MUJ A,00
LXJ H,5000
MOV B,M
PMX H
```

(d) #ORG 5000H

```
LXI H,5000
MOV B,M
MVI C,00
INX H
MOV A,M
```

```
#ORG 5000H
# DB 20H,05H.
```

Ans 8- (a) #ORG 8000H

```
Start  LXI H,8040H
       MVI D,00H
       MOV C,M
       DLR C
       JNX H

Check  MOV A,M
       LNX H
       JL Next Byte
       MOV B,M
       MOV M,A
       DCX M
       MOV M,B
       JMX H
       MVI D,00H

Next Byte  DCR C
           JNZ check
           MOV A,D
           JC start
```

```
#ORG 8000H
# DB 00H, 05H, 04H, 01H, 02H, 03H.
```

(b) Descending order.

```
#ORG 8000H
START  LXI  H, 8040H
       MVI  D, 00H
       MOV  C, M
       DLR  C
       JNX  H
CHECK  MOV  A,M
       JNX  H
       CMP  M
       JNL  NEXT Byte
       MOV  B,M
       MOV  M,A
       DCX  H
       MOV  M,B
       JNX  H
       MVI  D,01H

Next Byte  DER  C
           JML  CHECK
           MOV  D,D
           RRL
           JC   START
           MLT

#ORG 8040H
# DB 06H, 05H, 04H, 01H, 02H, 03H.
```

Ans 10 -

Program	Time (T-States)
LXI B, FFFFH	10
LOOP: DCX B	6
MOV A, B	4
ORA C	4
JNZ LOOP	10 (for Jump), 7 (Skip)
RET	10

from the table,

$$10 + (6+4+4+10) \times 65535H - 3 + 10$$

$$= 17 + 24 \times 65535H$$

$$= 1572857$$

So the time delay $= 1572857 \times \frac{1}{3} \mu s$

$$= 0.524285$$