MAX232, MAX2321 DUAL EIA-232 DRIVERS/RECEIVERS

SLLS047I - FEBRUARY 1989 - REVISED OCTOBER 2002

- Meet or Exceed TIA/EIA-232-F and ITU **Recommendation V.28**
- **Operate With Single 5-V Power Supply**
- Operate Up to 120 kbit/s
- **Two Drivers and Two Receivers**
- ±30-V Input Levels
- Low Supply Current . . . 8 mA Typical
- Designed to be Interchangeable With Maxim MAX232
- **ESD Protection Exceeds JESD 22** 2000-V Human-Body Model (A114-A)
- **Applications**

TIA/EIA-232-F **Battery-Powered Systems** Terminals Modems Computers

MAX232I...D, DW, OR N PACKAGE (TOP VIEW) 16 V_{CC} C1+ [V_{S+} [] 2 15 GND C1− [3 14**∏** T1OUT C2+ [] 4 13 R1IN C2- 1 5 12 R10UT 11 T1IN V_S_ [] 6 10 T2IN T20UT **[**] 7 9 R20UT R2IN **∏** 8

MAX232 . . . D, DW, N, OR NS PACKAGE

description/ordering information

The MAX232 is a dual driver/receiver that includes a capacitive voltage generator to supply EIA-232 voltage levels from a single 5-V supply. Each receiver converts EIA-232 inputs to 5-V TTL/CMOS levels. These receivers have a typical threshold of 1.3 V and a typical hysteresis of 0.5 V, and can accept $\pm 30 \text{-V}$ inputs. Each driver converts TTL/CMOS input levels into EIA-232 levels. The driver, receiver, and voltage-generator functions are available as cells in the Texas Instruments LinASIC™ library.

ORDERING INFORMATION

TA	PAC	PACKAGE [†] ORDERABL PART NUMBE		TOP-SIDE MARKING
	PDIP (N)	Tube	MAX232N	MAX232N
	SOIC (D)	Tube	MAX232D	MAX232
0°C to 70°C	3010 (D)	Tape and reel	MAX232DR	IVIAAZSZ
0 0 10 70 0	SOIC (DW)	Tube	MAX232DW	MAX232
	SOIC (DVV)	Tape and reel	MAX232DWR	IVIAAZOZ
	SOP (NS)	Tape and reel	MAX232NSR	MAX232
	PDIP (N)	Tube	MAX232IN	MAX232IN
	SOIC (D)	Tube	MAX232ID	MAX232I
–40°C to 85°C	3010 (D)	Tape and reel	MAX232IDR	IVIAAZOZI
	SOIC (DW)	Tube	MAX232IDW	MAX232I
	SOIC (DW) Tape and reel MAX232IDWF	MAX232IDWR	IVIMAZJZI	

[†]Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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Function Tables

EACH DRIVER

INPUT TIN	OUTPUT TOUT
L	Н
Н	L

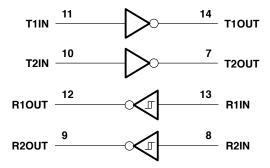
H = high level, L = low level

EACH RECEIVER

INPUT RIN	OUTPUT ROUT
L	Н
Н	L

H = high level, L = low level

logic diagram (positive logic)





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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Input supply voltage range, V _{CC} (see No	te 1)	–0.3 V to 6 V
Positive output supply voltage range, VS.	+	V _{CC} – 0.3 V to 15 V
Negative output supply voltage range, Vs	S=	0.3 V to –15 V
Input voltage range, V _I : Driver		0.3 V to V _{CC} + 0.3 V
Receiver		±30 V
Output voltage range, VO: T1OUT, T2OU	JT	$V_{S-} - 0.3 \text{ V to } V_{S+} + 0.3 \text{ V}$
R10UT, R20	UT	0.3 V to V _{CC} + 0.3 V
Short-circuit duration: T1OUT, T2OUT		
Package thermal impedance, θ_{JA} (see N	lote 2): D package	
	DW package	57°C/W
	N package	67°C/W
	NS package	64°C/W
Lead temperature 1,6 mm (1/16 inch) fro	m case for 10 seconds	260°C
Storage temperature range, T _{stg}		–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage		4.5	5	5.5	V
V _{IH}	High-level input voltage (T1IN,T2IN)		2			V
V _{IL}	Low-level input voltage (T1IN, T2IN)				0.8	V
R1IN, R2IN	Receiver input voltage				±30	V
т.	Oneverting free air temporature	MAX232	0		70	°C
TA	Operating free-air temperature	MAX232I	-40		85	C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 3 and Figure 4)

PARAMETER	TEST CONDITIONS	MIN	TYP [‡]	MAX	UNIT
I _{CC} Supply current	$V_{CC} = 5.5 \text{ V}$, All outputs open, $T_A = 25^{\circ}\text{C}$		8	10	mA

[‡] All typical values are at $V_{CC} = 5 \text{ V}$ and $T_A = 25^{\circ}\text{C}$.

NOTE 3: Test conditions are C1–C4 = 1 μ F at V_{CC} = 5 V ± 0.5 V.



NOTE 1: All voltage values are with respect to network ground terminal.

^{2.} The package thermal impedance is calculated in accordance with JESD 51-7.

DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature range (see Note 3)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT	
۷он	High-level output voltage	T1OUT, T2OUT	R_L = 3 kΩ to GND	5	7		V
VOL	Low-level output voltage‡	T1OUT, T2OUT	$R_L = 3 \text{ k}\Omega$ to GND		- 7	- 5	٧
ro	Output resistance	T1OUT, T2OUT	$V_{S+} = V_{S-} = 0, V_O = \pm 2 V$	300			Ω
los§	Short-circuit output current	T1OUT, T2OUT	$V_{CC} = 5.5 \text{ V}, \qquad V_{O} = 0$		±10		mA
IIS	Short-circuit input current	T1IN, T2IN	V _I = 0			200	μΑ

[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

NOTE 3: Test conditions are C1–C4 = 1 μ F at V_{CC} = 5 V \pm 0.5 V.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$ (see Note 3)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Driver slew rate	R _L = 3 k Ω to 7 k Ω , See Figure 2			30	V/µs
SR(t)	Driver transition region slew rate	See Figure 3		3		V/µs
	Data rate	One TOUT switching		120		kbit/s

NOTE 3: Test conditions are C1–C4 = 1 μ F at V_{CC} = 5 V ± 0.5 V.

RECEIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature range (see Note 3)

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PARAMETER			TEST	CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	R1OUT, R2OUT	$I_{OH} = -1 \text{ mA}$		3.5			V
V_{OL}	Low-level output voltage‡	R1OUT, R2OUT	I _{OL} = 3.2 mA				0.4	V
V _{IT+}	Receiver positive-going input threshold voltage	R1IN, R2IN	V _{CC} = 5 V,	T _A = 25°C		1.7	2.4	V
V _{IT} –	Receiver negative-going input threshold voltage	R1IN, R2IN	V _{CC} = 5 V,	T _A = 25°C	0.8	1.2		V
V _{hys}	Input hysteresis voltage	R1IN, R2IN	V _{CC} = 5 V		0.2	0.5	1	V
rį	Receiver input resistance	R1IN, R2IN	V _{CC} = 5,	T _A = 25°C	3	5	7	kΩ

[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

NOTE 3: Test conditions are C1–C4 = 1 μ F at V_{CC} = 5 V \pm 0.5 V.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$ (see Note 3 and Figure 1)

	PARAMETER	TYP	UNIT
tPLH(R)	Receiver propagation delay time, low- to high-level output	500	ns
tPHL(R)	Receiver propagation delay time, high- to low-level output	500	ns

NOTE 3: Test conditions are C1–C4 = 1 μ F at V_{CC} = 5 V \pm 0.5 V.

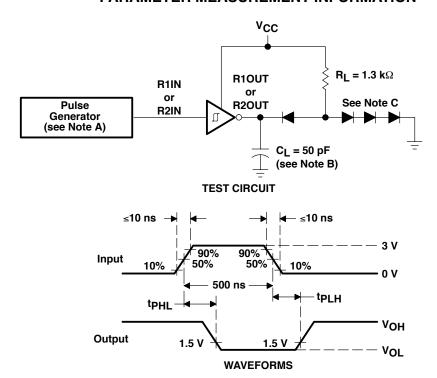


[‡] The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic voltage

[§] Not more than one output should be shorted at a time.

[‡]The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic voltage levels only.

PARAMETER MEASUREMENT INFORMATION

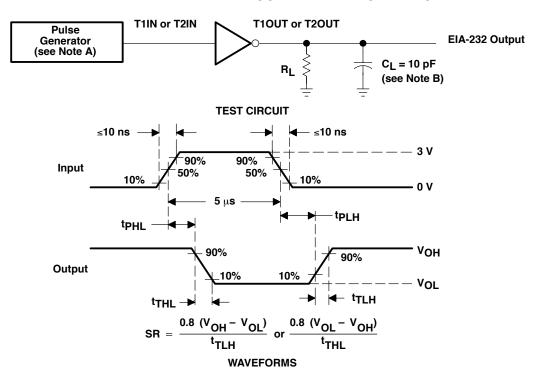


NOTES: A. The pulse generator has the following characteristics: $Z_{\mbox{O}}$ = 50 Ω , duty cycle \leq 50%.

- B. C_L includes probe and jig capacitance.
- C. All diodes are 1N3064 or equivalent.

Figure 1. Receiver Test Circuit and Waveforms for $t_{\mbox{\scriptsize PLH}}$ and $t_{\mbox{\scriptsize PLH}}$ Measurements

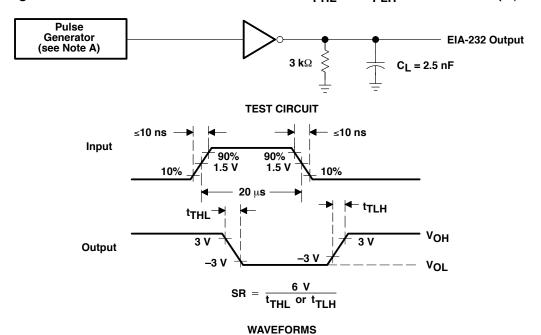
PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: $Z_0 = 50 \Omega$, duty cycle $\leq 50\%$.

B. C_L includes probe and jig capacitance.

Figure 2. Driver Test Circuit and Waveforms for t_{PHL} and t_{PLH} Measurements (5-μs Input)

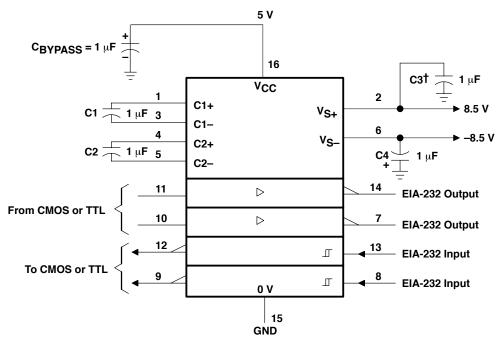


NOTE A: The pulse generator has the following characteristics: Z_O = 50 Ω , duty cycle \leq 50%.

Figure 3. Test Circuit and Waveforms for t_{THL} and t_{TLH} Measurements (20-μs Input)



APPLICATION INFORMATION



†C3 can be connected to V_{CC} or GND.

Figure 4. Typical Operating Circuit

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