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DIMPAL SAMAL

CAREER OBJECTIVE

To obtain a challenging position in an organization that best utilizes my skills, abilities and provide opportunities to enhance my technical skills which would help me to solve critical real time problems while fulfilling the organization goals.

PROFILE SUMMARY

- Around two year of experience in PnR, Synthesis, IR.
- Worked as Physical design Intern with one year experience, has experience in handling multiple blocks in 16 nm technology node.
- Hands on expertise in Floorplan, Placement, Clock Tree Synthesis, Routing, and Timing Closure.
- Good knowledge of ASIC flow.
- Expertise in placement of high-count macros during Floor Planning, Pin Placement, Floorplan Def Resize.
- Good understanding of Floorplan and placement challenges especially for blocks with many and logic intensive designs.
- Good Knowledge in IR and physical Verification.
- Good understanding of static timing analysis and timing fixes for block
- Good knowledge of synthesis, LEC.
- Good in Shell scripting.

WORK EXPERIENCE

- **Maxlinear Technologies** ***June 2024- present***

PD-Design Automation Engineer

- Worked on PD flow development.
- Worked on Gatelevel netlist Handoff script development

Skills used: Innovus,Aprisa,TCL,Python,Linux,Git,

Physical Design Intern ***Jul-2023-Jun 2024***

Block 1 Description

- Instance count: 425904
- IO pins : 655
- Macros :72
- Frequency : 500 MHz

Design Complexities:

- Timing critical paths with more logic depth in the design.
- Analysing and fixing huge congestion at notches using placement blockages, route guides, floorplan changes, bounds.
- Fixed Shorts/Opens and DRC violation .

Block 2 Description

- Instance count: 2.6 Million
- IO pins : 1400
- Macros :57
- Frequency : 500 MHz

Design Complexities:

- Core congestion is high in the design, and it is unrouteable.

- Timing is critical for two of the modules.

Block 3 Description:

- Instance Count : 2 million
- I0 pins :1372 pins
- Macro : 2
- Frequency : 700 Mhz

Design Complexities:

- The Block is type of feedthrough block.
- Automatically placing the pins with respect to given location.
- Reduction in cross talk of clock nets
- Resolving the tran violation issues.

Role :

- Floorplan | Power plan | Placement | Trial route and congestion analysis | CTS | Detail Routing | Timing Closure

Tools used :

- Innovus for Physical design implementation

EDUCATION

Degree	Institute/ Board	CGPA	Year
B.Tech, ECE	IIIT-NUZVID	8.4/10	2019-2023
12th Grade	IIIT-NUZVID	8.0/10	2017-2019
10th Grade	Kendriya Vidyalaya NAD,VSKP [CBSE]	10/10	2007-2017

TECHNICAL SKILLS

Primary Skills: PNR | Synthesis | Timing Analysis and Timing closure

EDA Tools: Cadence Innovus | Aprisa | Genus | Tempus | Xilinx | Arduino | Multisim | LTSpice

Scripting: TCL- Scripting | Shell-Scripting | Verilog | Linux | C

PUBLICATION AND ACADEMIC ACCOLADES

1. **IEEE paper got selected for publishing in VLSID conference**
2. **Achieved Award of Excellence** in International Competition *INNOVATE FPGA 2021-22* a design contest conducted by Intel ,Terasic, San-Jose, California.
3. Achieved **Rajya Puraskar** by the then governor of the association of Bharat Scouts and Guides in the year 2016.

LANGUAGES

English | Hindi | Oriya | Bengali | Telugu | Sanskrit

HOBBIES

Drawing and painting | Playing chess | Learning Languages |Travelling

DECLARATION

I, **Dimpal Samal** hereby declare that the above-mentioned information is correct and genuine to my knowledge and belief, I bear the responsibility for the correctness of the above-mentioned particulars.