DIMPAL SAMAL

CAREER OBJECTIVE

To obtain a challenging position in an organization that best utilizes my skills, abilities and provide opportunities to enhance my technical skills which would enable me to solve critical real time problems while fulfilling the organization goals.

PROFILE SUMMARY

- Around one year of experience in PnR,Synthesis,PV.
- Worked as Physical design Intern with one year experience, has experience in handling multiple blocks in 16 nm technology node
- Hands on expertise in Floorplan, Placement, Clock Tree Synthesis, Routing, and Timing Closure
- Good knowledge of ASIC flow.
- Expertise in placement of high-count macros during Floor Planning, Pin Placement, Floorplan Def Resize.
- Good understanding of Floorplan and placement challenges especially for blocks with many and logic intensive designs.
- Good Knowledge of input files of PnR.
- Good understanding of static timing analysis and timing fixes for block
- Good knowledge of synthesis, LEC.
- Developed the scripts for automation of PNR flow
- Good understanding of Shell scripting.

WORK EXPERIENCE

- **Maxlinear Technologies** *Jul-2022-Jun 2023*

  Physical Design Intern

  Block 1 Description
  - Instance count: 425904
  - IO pins : 655
  - Macros :72
  - Frequency : 500 MHz

  Design Complexities:
  - Timing critical paths with more logic depth in the design.
  - Analysing and fixing huge congestion at notches using placement blockages, route guides, floorplan changes, bounds.
  - Fixed Shorts/Opens and DRC violation to obtain DRC clean design.

Block 2 Description

- Instance count: 2.6 Million
- IO pins : 1400
- Macros :57
- Frequency : 500 MHz

Design Complexities:

- Core congestion is high in the design, and it is unrouteable.
- Timing is critical for two of the modules.

Block 3 Description:

- Instance Count : 2 million
- I0 pins :1372 pins
- Macro : 2
- Frequency : 700 Mhz

Design Complexities:

- The Block is type of feedthrough block.
- Automatically placing the pins with respect to given location.
- Reduction in cross talk of clock nets
- Resolving the tran violation issues.

Role :

• Floorplan | Power plan | Placement | Trial route and congestion analysis | CTS | Detail Routing | Timing Closure

Tools used :

- Innovus for Physical design implementation

- **HPCL**

  April 2024 - present

  Networking Engineer - Graduate Apprenticeship Trainee

  - Confiuring of switches
  - Writing policies for Fortinet-40f firewall

EDUCATION

Degree	Institute/ Board	CGPA	Year
B.Tech, ECE	IIIT-NUZVID	8.8/10	2019-2023
12th Grade	IIIT-NUZVID	8.0/10	2017-2019
10th Grade	Kendriya Vidyalaya NAD,VSKP [CBSE]	10/10	2007-2017

TECHNICAL SKILLS

Primary Skills: PNR | Synthesis | Timing Analysis and Timing closure
EDA Tools: Cadence Innovus | Aprisa | Genus | Tempus | Xilinx | Arduino | Multisim | LTSpice
Scripting: TCL- Scripting | Shell-Scripting | Verilog | Linux | C

ACADEMIC PROJECTS

- **Digital Eye for Aid of Blind people using FPGA**
  Duration: 1 year
  Team Size: 3
  Role Played: Team member
  Skills Used: open cv, verilog , python
  The project aims to help the blind and visually impaired people which makes them independent to a certain extent. The idea is to guide the individual by giving the necessary instructions to reach their location and also by using image processing techniques, the device will be able to convert the text to speech which makes him/her independent to the most extent. Our Prototype plan includes the glasses(spectacles).

- **Vehicle accident Detection**
  Duration: 1 month
  Team Size: 3
  Role Played: Team Leader
  Skills Used: android studio, Verilog, Python and Arduino
  The prototype device is made using De-10 Nano board. We have designed a bot as like vehicle, whenever the vehicle gets tilted or accident occurs the information is conveyed through the app to friends or family member who has been login in the app and they will get a alert message displaying “Accident has been occurred” with a beeping alarm sound whenever the bot is tilted.

- **Implementation of Digital Clock on Nexys-4 DDR Board**
  Duration: 1 Week
  Team Size: 1
  Role Played: Individual
  Skills Used: Verilog
  The clock is made using Verilog on FPGA (nexyx-4 DDR) board. This is implemented using counter module and display module. Counter module consists of sec., min., hours counters. The outputs generated by the digital clock sent to the seven segment display through the decoder. The decoder decodes the decimal input into binary code and then load as input to the seven segment display. The display shows the seconds, minutes, hours that obtained from the clock.

- **Bus Reservation System**

Duration: 1 week
Role Played: Individual
Skills Used: c language
The main objective of this project is to give satisfaction to the customers of booking tickets without going out and waiting for the reservation.

- **Counter using DE-10 Nano Board**
  Duration: 1 Week
  Team Size: 1
  Role Played: individual
  Skills Used: Verilog
  Designed the 4-bit counter and implemented this using Verilog in the Quartus prime software and implemented in De-10 Nano Board using Verilog.

PUBLICATION AND ACADEMIC ACCOLADES

1**. IEEE paper got selected for publishing in VLSID conference**
2. **Achieved Award of Excellence** in International Competition *INNOVATE FPGA 2021-22* a design contest conducted by Intel ,Terasic, San-Jose, California.
3.Achieved **Rajya Puraskar** by the then governor of the association of Bharat Scouts and Guides in the year 2016.

EXTRA AND CO-CURRICULAR ACTIVITIES

1.Got 3rd position in Target ball -National Association Organized by PUNJAB STATE TARGETBALL ASSOCIATION at Sant Nagar,Moga(Rb).
2. Worked as an Event Organizer in Technical fest [Teckzite] conducted by RGUKT, Nuzvid in the year 2021-
22.
3. Participated in Workshop on IOT with Google Assistant conducted by AMZ.
4. Attended the workshop on Digital radio Design organized by IEEE on 11th -12th Dec 2021.
5. Attended AARK IC Technologies webinar on opportunities in RTL Design and Verification on 13th
Dec 2021.

LANGUAGES

English | Hindi | Oriya | Bengali | Telugu | Sanskrit

HOBBIES

Drawing and painting | Playing chess | Learning Languages |Travelling

DECLARATION

I, **Dimpal Samal** hereby declare that the above-mentioned information is correct and genuine to my knowledge and belief, I bear the responsibility for the correctness of the above-mentioned particulars.