ECE 385

Fall 2020

Experiment #1

Introductory TTL Experiment

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Section ABF

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Introduction

The lab is designed to introduce the digital design equipment, and to apply it to the basic concept of circuit design and logic. Also, the exposure to the TTL experiment and its application towards circuit operations shows how to implement logic to design the circuits. The TTL introduction also enables for the practical consideration of clock cycles in terms of delays and glitches (static hazards).

Circuit Design and Operations

The circuit implements a basic input/output design, analyzing simple logic employed. In this case, the circuit takes into consideration of three input (A, B, C), which subsequently goes through a logic series yielding a certain output Z. The initial design consists of 4 2-input NAND gates, where input A and B signals were driven into a NAND gate, inverted B and C signals were driven into another NAND gate, and the output of both former signals were driven into a final NAND gate to yield an output Z (Circuit Schematic). The circuit was tested when various input signals were driven into the circuit to yield a definite output (Figure 1).

A	B	C	Z
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

	BC				
		00	**01**	**11**	**10**
A	**0**	0	1	0	0
	1	0	1	1	1

Figure 1 – Truth Table and Karnaugh Map of Circuit Design

The implementation of circuit design was tested out with a lab oscilloscope, which showed that the current design is practically flawed (Circuit Schematic 1) – there is certain time delay that presents a glitch in the output signal (Figure 2a).

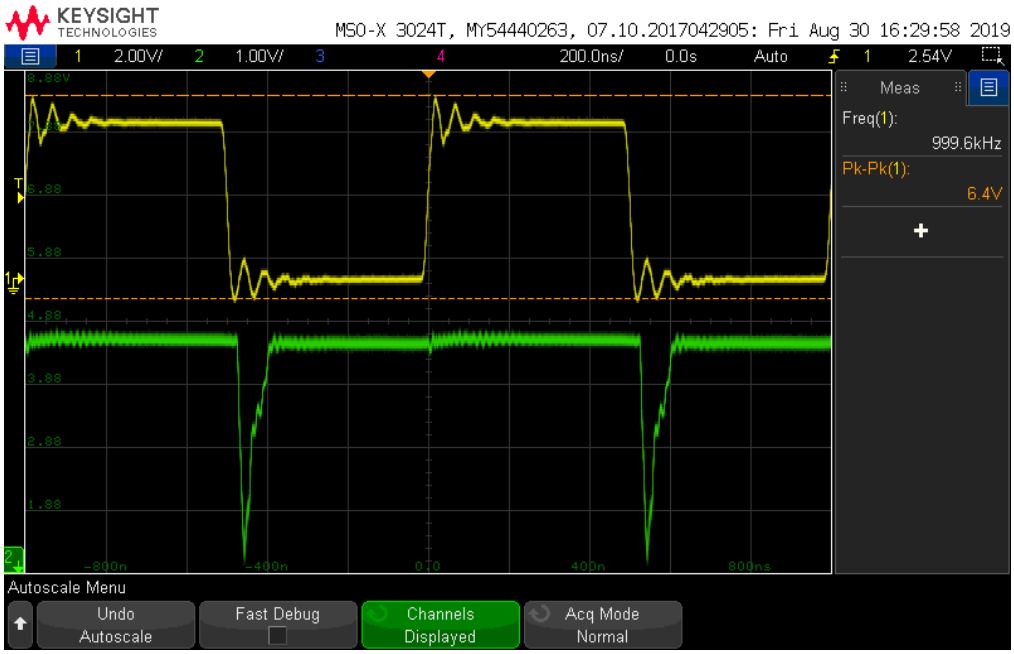


Figure 2a – Scope of First Circuit Design (collected Fall 2019)

As the static hazard causing delay represents a flaw in the practical application of the logical design, an intermediate was amended to the design, with an additional condition – the A and C signals were driven through a separate NAND gate, which is then additionally connected to the output NAND gate (Circuit Schematic 2) – the output then yield a continuous signal (Figure 2b). Also note that despite the practical logic adjustment needed to remove the static hazard, the logic implementation remains the same (or, truth table and K-map remains the same).

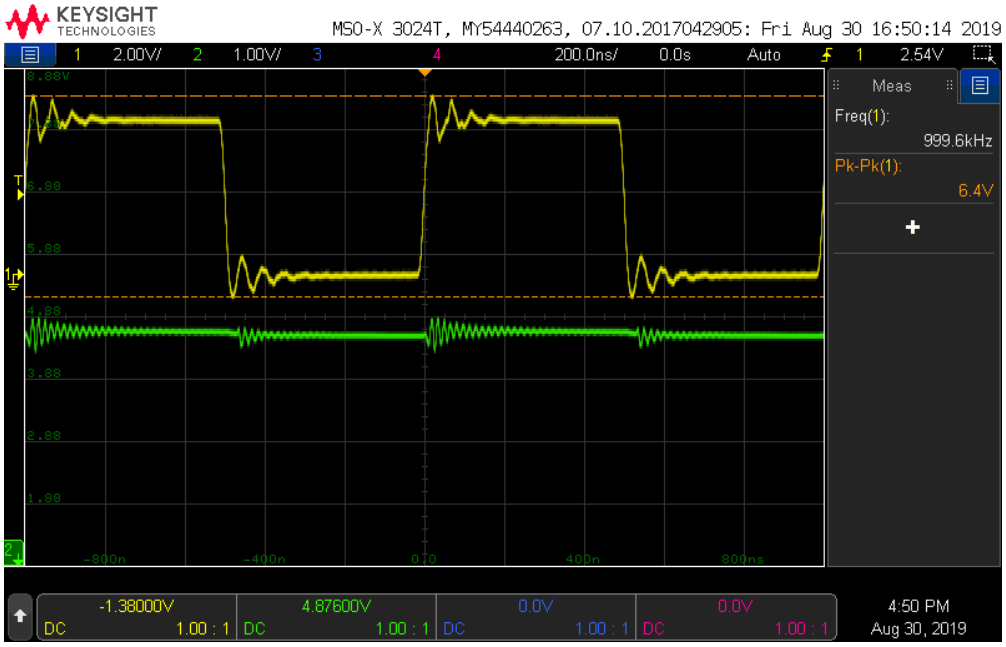
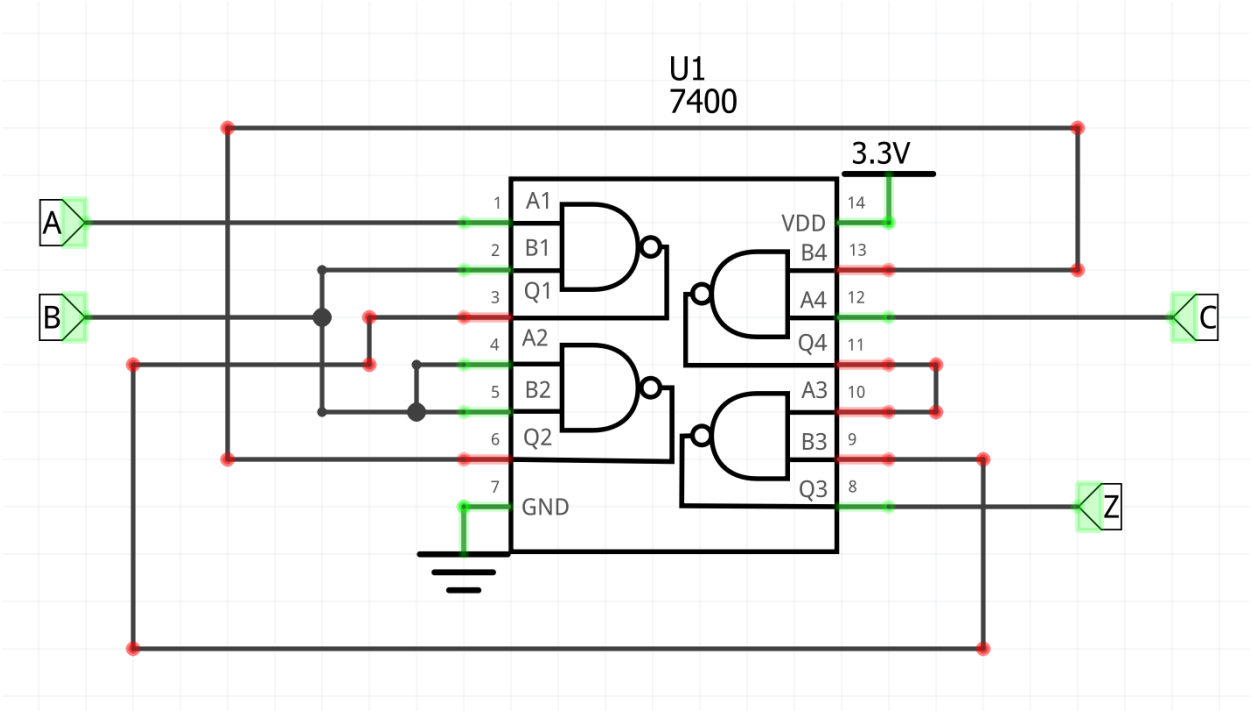
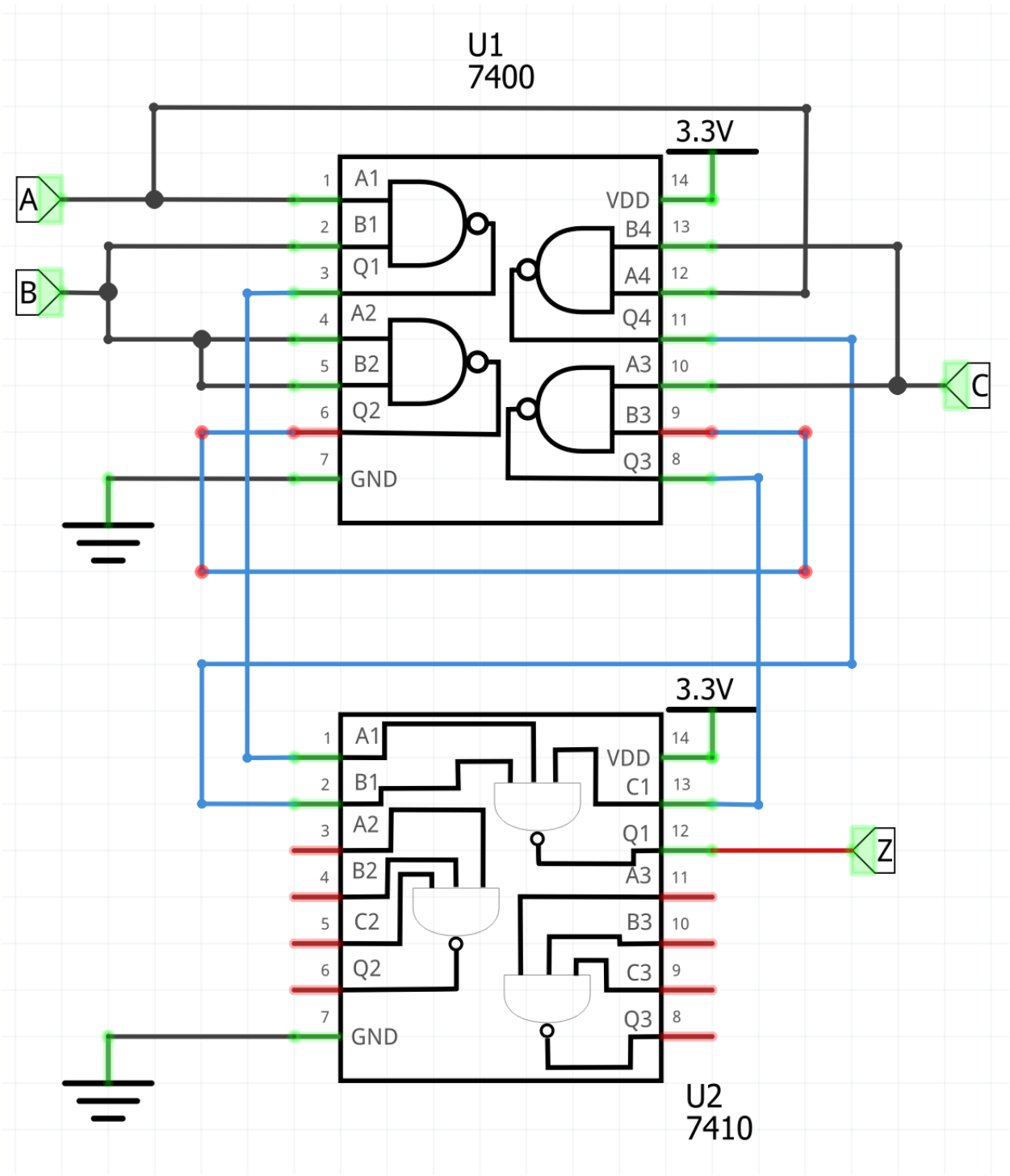


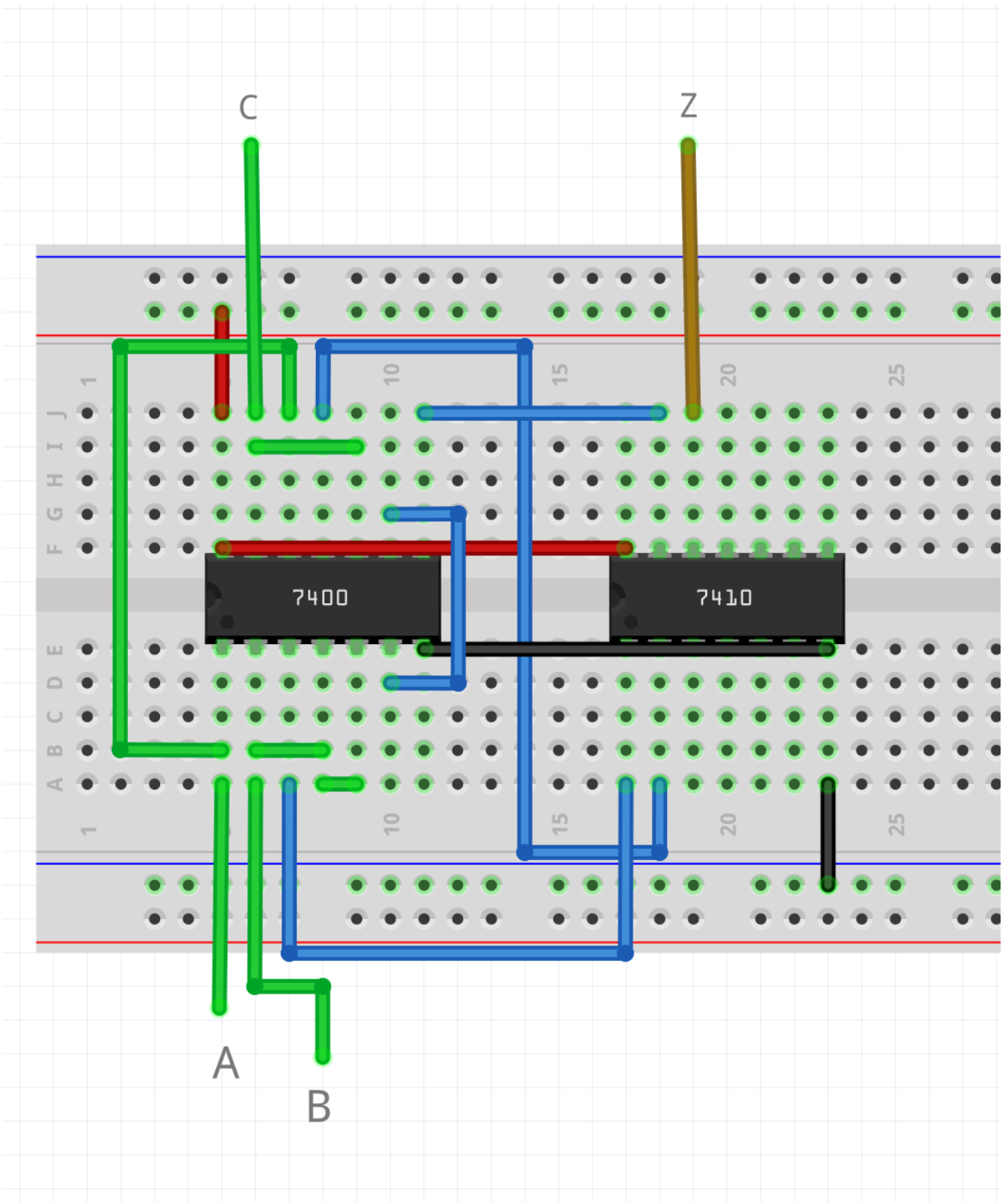
Figure 2b – Scope of Fixed Circuit Design (collected Fall 2019)

Circuit Schematic



Schematic 1 – Static Hazard Design


U1
7400
3.3V
A
B
C
1 A1
2 B1
3 Q1
4 A2
5 B2
6 Q2
7 GND
14 VDD
13 B4
12 A4
11 Q4
10 A3
9 B3
8 Q3
3.3V
1 A1
2 B1
3 A2
4 B2
5 C2
6 Q2
7 GND
14 VDD
13 C1
12 Q1
11 A3
10 B3
9 C3
8 Q3
Z
U2
7410



Schematic 2 – No Static Hazard

Post Experiment Analysis

If given a guaranteed minimum propagation delay of a 7400 is 0ns and that its guaranteed maximum delay time is 20ns, the guaranteed clock diagram is determined by the maximum delay time when the signals pass through each existing impedance (Figure 5).

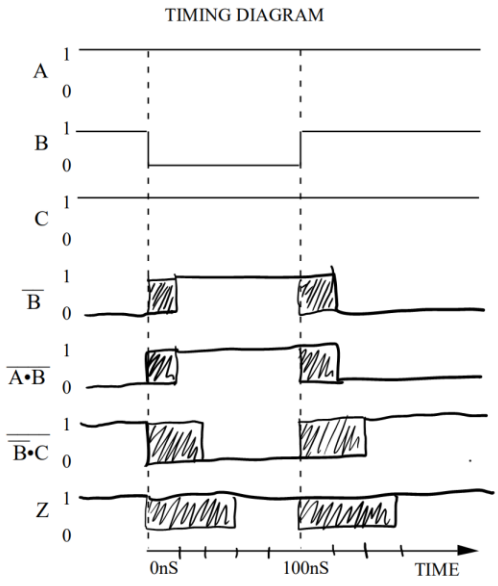


Figure 5 – Timing Diagram

Based on the diagram, it takes 60ns for both the rising edge and the falling edge of B to stabilize in output Z.

A debounced circuit makes sure that only a single signal is acted upon with the closing of contact when potential multiple signals are present. It acts like a switch as it ensures a smooth transition from a high signal to low signal (or vice versa).

General Guide Inquiries

GG.6:

Having a larger noise immunity would allow for the logic to read the correct value even with the added noise through the input. In other words, the chip will yield the right logic despite any noises the input may produce.

The last inverter is observed so that noise immunity can be applied to full effect. Essentially, if there were to be any noise produced through the input, it would not reflect as such through the last inverter as it would the first.

Consider X to be the noise immunity for logic 0 and Y to be the noise immunity for logic 1 (with both being input voltage – defined as VIN). Based on the graph, 0.35V and 3.5V are the outputs measured, with their nominal ranges as double difference from standard. So, if VIN is between

0.35 and 1.15, the output would be within the nominal range for logic ‘1’ – the range is 1.15 – 0.35 = 0.8V. Also, between 1.35V and 3.5V for VIN, VOUT is determined to not be ‘0’, so the range would be 3.5-1.35 = 2.15V. Since the noise immunity is determined by the smallest of ranges of X and Y, 2.15 > 0.8 so the noise immunity is determined to be 0.8V.

GG.31:

In regards to LED, different LEDs have different characteristics (which may include differing forwarding bias). As such, if you share resistors and add more than 1 LEDs, that means that you are trying to share signals between LEDs with potentially different characteristics – ie… some LEDs may not even turn on.

Conclusion

This lab covered the introductory transistor-transistor logic using logic gates in order to design a functional circuit. Throughout the process, this lab also introduced the practical application of hardware glitches (ie.. static hazard) that delays the output logic. The lab essentially covered the transition between the theoretical and practical component of the transistor-transistor logic with fairly few problems, especially in the design process. Based on this lab, a practical application taken into consideration is the influence of static hazards in transistor logic through the entirety of the circuit, especially in regards to its effect on the output.