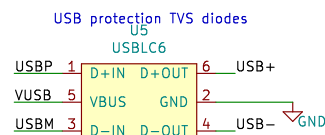


Connector Pin	PCB Pin	TP Pin
VUSB	VUSB	TP6 USB
5V0	5V0	TP7 5V0
4V0	4V0	TP8 4V0
3V3	3V3	TP9 3V3
D+	USBP	
D-	USBM	
PG00D	PG00D	TP10 PG00D

3V3 Place one decoupling cap at each power pin.



3V3 → VCC

PPSD → PPS\_GPS  
TXDD → TX\_GPS  
RXD → RX\_GPS  
RST → RESET\_GPS

The diagram shows two pin connection tables for the debugger and external SPI interface.

**DEBUG INTERFACE**

Signal	Pin
SWCLK	1
SWDIO	2
RST	3
3V3	4
GND	5

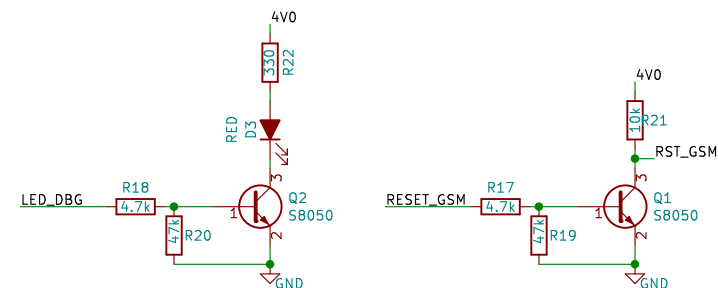
Connector: J1 Conn\_01x05

**EXTERNAL SPI INTERFACE**

Signal	Pin
3V3	1
SPI_SCK	2
SPI_MISO	3
SPI_MOSI	4
GND	5

Connector: J4 Conn\_01x05

Figure 1 illustrates the control logic for two switches, SW1 and SW2, which are Push-DPDT (Double Pole Double Throw) switches. SW1 controls the TX\_1, RX\_GPS, RX\_USB, RX\_1, TX\_GPS, and TX\_USB lines. SW2 controls the TX\_2, RX\_GSM, RX\_USB, RX\_2, TX\_GSM, and TX\_USB lines. The diagrams show the internal wiring and connections for each switch, including the common, normally open, and normally closed contacts.



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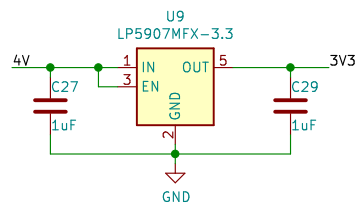
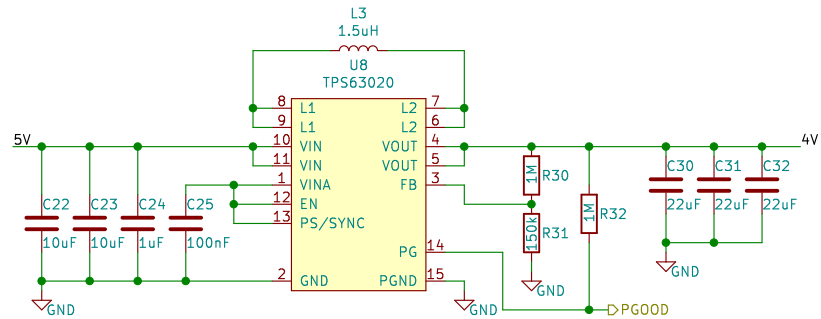
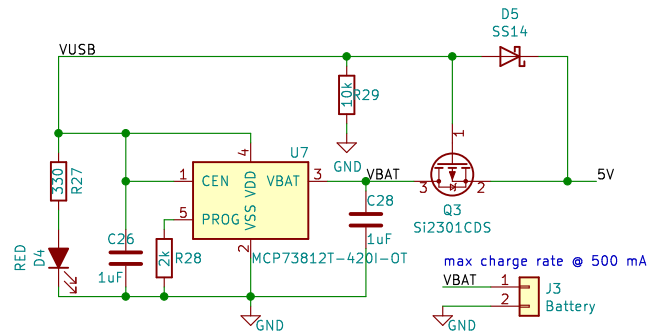
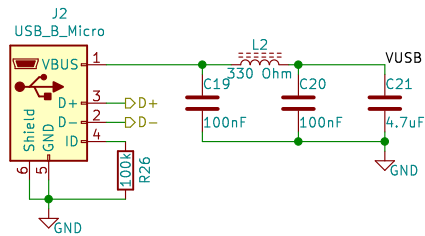
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Rev: 1.0  
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VUSB  $\rightarrow$  VUSB  
5V  $\rightarrow$  5V  
3V3  $\rightarrow$  3V3  
4V  $\rightarrow$  4V



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Size: A4

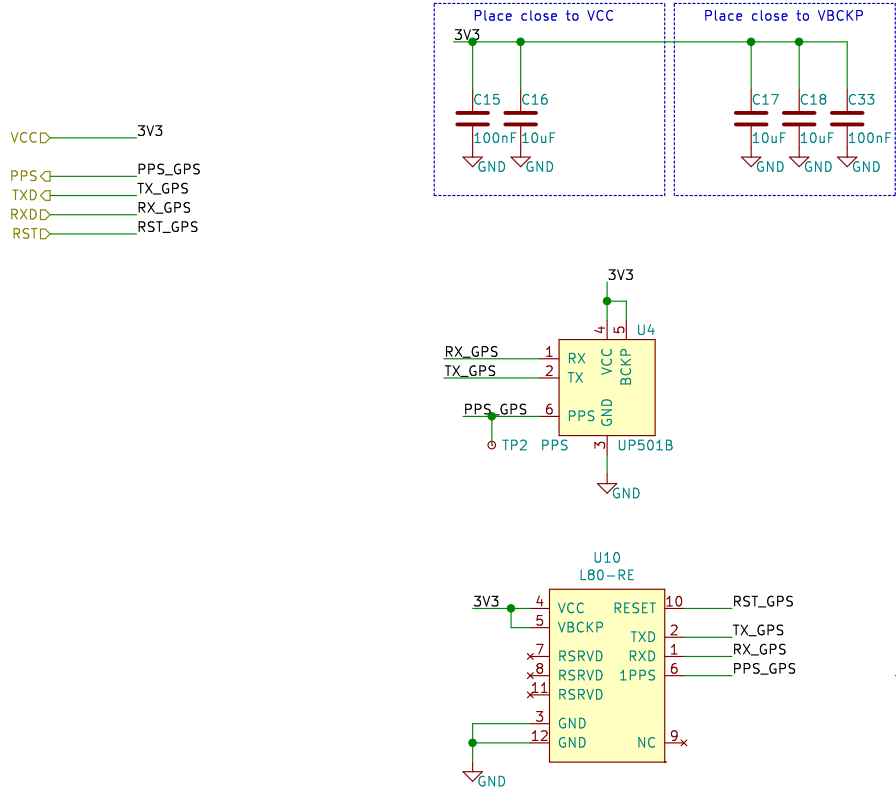
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Rev: 1

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Id: 2/3

## Decoupling capacitors



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