

The schematic diagram shows the V\_GATE driver circuit. It begins with a BATT supply connected to a green line. This line passes through diode D1B (BAW56) in series with a 47nF capacitor C2 to pump1. It then passes through diode D2A (BAV99) in series with a 47nF capacitor C4 to pump2. Finally, it passes through diode D2B (BAV99) in series with a 1uF capacitor C5 to GND. The output of the final diode is labeled V\_GATE.

Pin configuration for SWD J1:

- Pin 1: +3V3
- Pin 2: SWCLK
- Pin 3: GND
- Pin 4: SWDIO
- Pin 5: NRST
- Pin 6: UART\_TX



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