1. Description

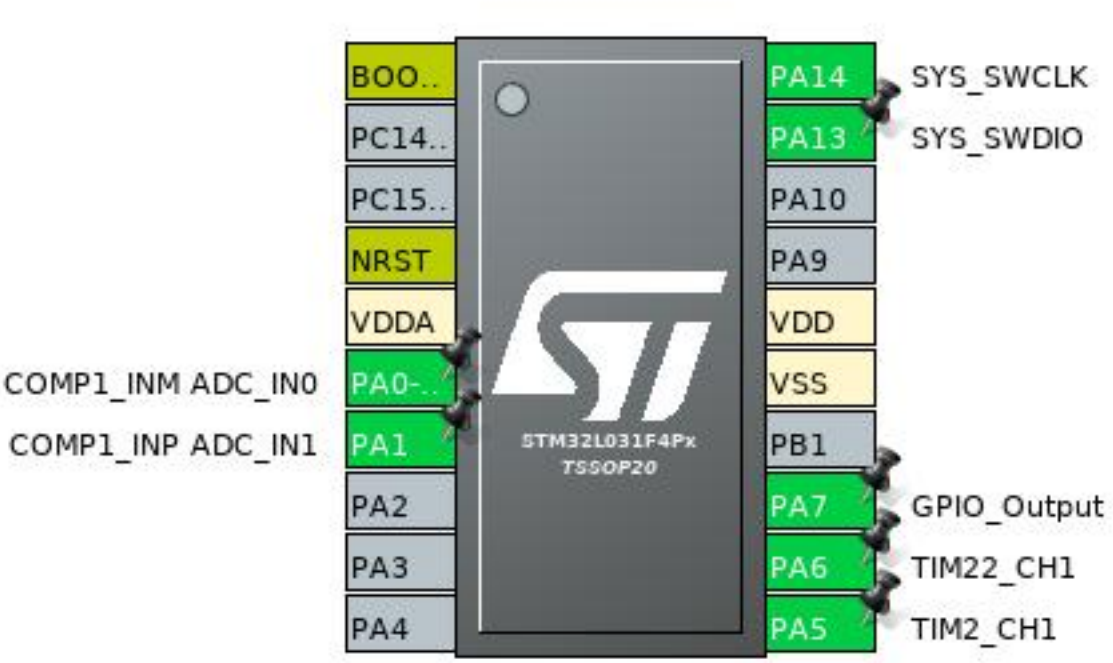
1.1. Project

Project Name	adc-dma
Board Name	custom
Generated with:	STM32CubeMX 5.3.0
Date	08/04/2019

1.2. MCU

MCU Series	STM32L0
MCU Line	STM32L0x1
MCU name	STM32L031F4Px
MCU Package	TSSOP20
MCU Pin number	20

2. Pinout Configuration

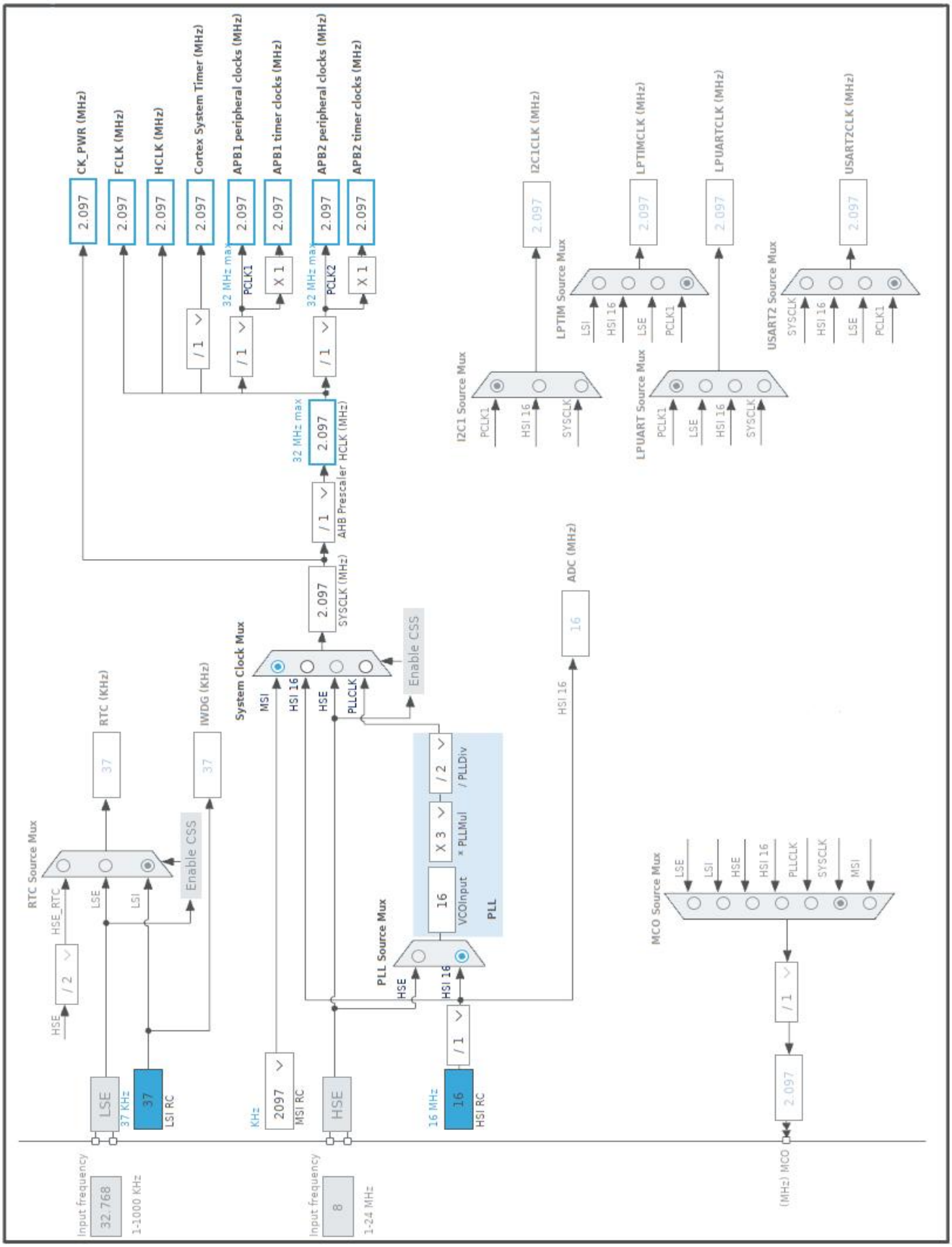


3. Pins Configuration

Pin Number TSSOP20	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	BOOT0	Boot		
4	NRST	Reset		
5	VDDA	Power		
6	PA0-CK_IN	I/O	COMP1_INM, ADC_IN0	
7	PA1	I/O	COMP1_INP, ADC_IN1	
11	PA5	I/O	TIM2_CH1	
12	PA6	I/O	TIM22_CH1	
13	PA7 *	I/O	GPIO_Output	
15	VSS	Power		
16	VDD	Power		
19	PA13	I/O	SYS_SWDIO	
20	PA14	I/O	SYS_SWCLK	

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	adc-dma
Project Folder	/home/peter/repos/stm32-adc-dma/adc-dma
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_L0 V1.11.2

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32L0
Line	STM32L0x1
MCU	STM32L031F4Px
Datasheet	027063_Rev4

6.2. Parameter Selection

Temperature	25
Vdd	3.0

7. IPs and Middleware Configuration

7.1. ADC

mode: IN0

mode: IN1

7.1.1. Parameter Settings:

ADC_Settings:

Clock Prescaler	**Synchronous clock mode divided by 2 ***
Resolution	ADC 12-bit resolution
Data Alignment	Right alignment
Scan Direction	Forward
Continuous Conversion Mode	**Enabled ***
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	**Enabled ***
End Of Conversion Selection	End of single conversion
Overrun behaviour	**Overrun data overwritten ***
Low Power Auto Wait	Disabled
Low Frequency Mode	Disabled
Auto Off	Disabled
Oversampling Mode	Disabled

ADC_Regular_ConversionMode:

Sampling Time	**12.5 Cycles ***
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None

WatchDog:

Enable Analog WatchDog Mode	false

7.2. COMP1

Input [+]: INP

Input [-]: INM

7.2.1. Parameter Settings:

Basic Parameters:

Trigger Mode	**Interrupt mode with Rising/Falling Edges detection ***
Output Polarity	**Inverted ***
Low Power Timer (LPTIM) Connection	Disabled

7.3. RCC

7.3.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Buffer Cache	Enabled
Prefetch	Disabled
Preread	Enabled
Flash Latency(WS)	0 WS (1 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
MSI Calibration Value	0
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1

7.4. SYS

mode: Debug Serial Wire

Timebase Source: SysTick

7.5. TIM2

Channel1: PWM Generation CH1

7.5.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**4095 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

7.6. TIM22

Channel1: PWM Generation CH1

7.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**4095 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC	PA0-CK_IN	ADC_IN0	Analog mode	No pull-up and no pull-down	n/a	
	PA1	ADC_IN1	Analog mode	No pull-up and no pull-down	n/a	
COMP1	PA0-CK_IN	COMP1_INM	Analog mode	No pull-up and no pull-down	n/a	
	PA1	COMP1_INP	Analog mode	No pull-up and no pull-down	n/a	
SYS	PA13	SYS_SWDIO	n/a	n/a	n/a	
	PA14	SYS_SWCLK	n/a	n/a	n/a	
TIM2	PA5	TIM2_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
TIM22	PA6	TIM22_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	
GPIO	PA7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	

8.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC	DMA1_Channel1	Peripheral To Memory	**Medium ***

ADC: DMA1_Channel1 DMA request Settings:

Mode:	**Circular ***
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

8.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable Interrupt	true	0	0
Hard fault interrupt	true	0	0
System service call via SWI instruction	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA1 channel 1 interrupt	true	0	0
ADC, COMP1 and COMP2 interrupts (COMP interrupts through EXTI lines 21 and 22)	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash and EEPROM global interrupt	unused		
RCC global interrupt	unused		
TIM2 global interrupt	unused		
TIM22 global interrupt	unused		

*** User modified value**

9. Software Pack Report