HIGH-SPEED DIFFERENTIAL LINE DRIVERS

FEATURES

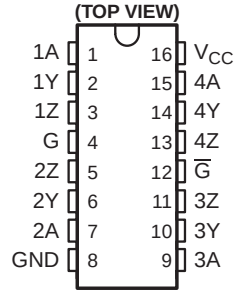
- **Meet or Exceed the Requirements of ANSI TIA/EIA-644 Standard**
- **Low-Voltage Differential Signaling With Typical Output Voltage of 350 mV and 100-Ω Load**
- **Typical Output Voltage Rise and Fall Times of 500 ps (400 Mbps)**
- **Typical Propagation Delay Times of 1.7 ns**
- **Operate From a Single 3.3-V Supply**
- **Power Dissipation 25 mW Typical Per Driver at 200 MHz**
- **Driver at High Impedance When Disabled or With V_{CC} = 0**
- **Bus-Terminal ESD Protection Exceeds 8 kV**
- **Low-Voltage TTL (LVTTL) Logic Input Levels**
- **Pin Compatible With AM26LS31, MC3487, and µA9638**
- **Cold Sparing for Space and High Reliability Applications Requiring Redundancy**

DESCRIPTION

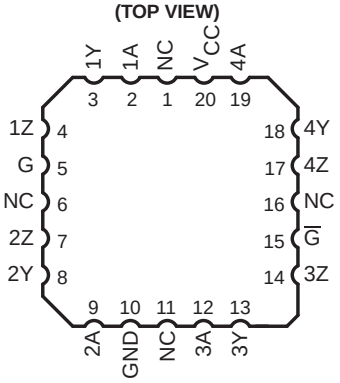
The SN55LVDS31, SN65LVDS31, SN65LVDS3487, and SN65LVDS9638 are differential line drivers that implement the electrical characteristics of low-voltage differential signaling (LVDS). This signaling technique lowers the output voltage levels of 5-V differential standard levels (such as TIA/EIA-422B) to reduce the power, increase the switching speeds, and allow operation with a 3.3-V supply rail. Any of the four current-mode drivers will deliver a minimum differential output voltage magnitude of 247 mV into a 100-Ω load when enabled.

The intended application of these devices and signaling technique is both point-to-point and multidrop (one driver and multiple receivers) data transmission over controlled impedance media of approximately 100 Ω. The transmission media may be printed-circuit board traces, backplanes, or cables. The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media and the noise coupling to the environment.

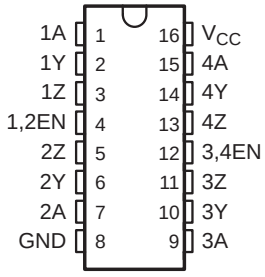
SN55LVDS31 . . . J OR W
SN65LVDS31 . . . D OR PW
(Marked as **LVDS31** or **65LVDS31**)
(TOP VIEW)



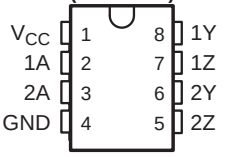
SN55LVDS31FK
(TOP VIEW)



SN65LVDS3487D
(Marked as **LVDS3487** or **65LVDS3487**)
(TOP VIEW)



SN65LVDS9638D (Marked as **DK638** or **LVDS38**)
SN65LVDS9638DGN (Marked as **L38**)
SN65LVDS9638DGK (Marked as **AXG**)
(TOP VIEW)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (CONTINUED)

The SN65LVDS31, SN65LVDS3487, and SN65LVDS9638 are characterized for operation from –40°C to 85°C. The SN55LVDS31 is characterized for operation from –55°C to 125°C.

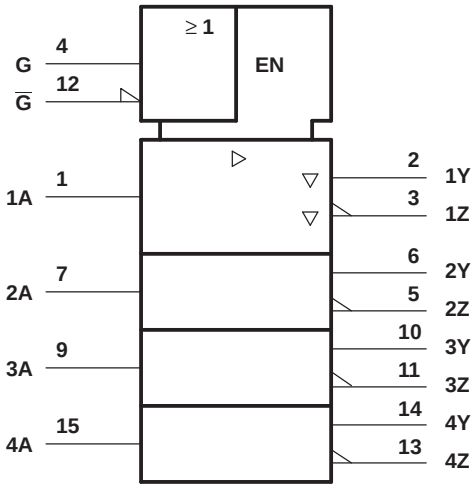
AVAILABLE OPTIONS

T_A	PACKAGE(1)					
	SMALL OUTLINE		MSOP	CHIP CARRIER (FK)	CERAMIC DIP (J)	FLAT PACK (W)
	(D)	(PW)				
–40°C to 85°C	SN65LVDS31D	SN65LVDS31PW	—	—	—	—
	SN65LVDS3487D	—	—	—	—	—
	SN65LVDS9638D	—	SN65LVDS9638DGN	—	—	—
	—	—	SN65LVDS9638DGK	—	—	—
–55°C to 125°C	—	—	—	SNJ55LVDS31FK	SNJ55LVDS31J	SNJ55LVDS31W SN55LVDS31W

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

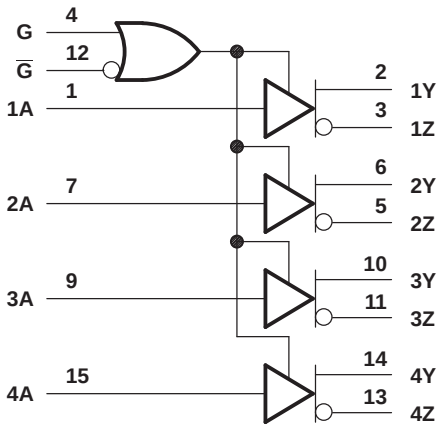
logic symbol†

SN55LVDS31, SN65LVDS31

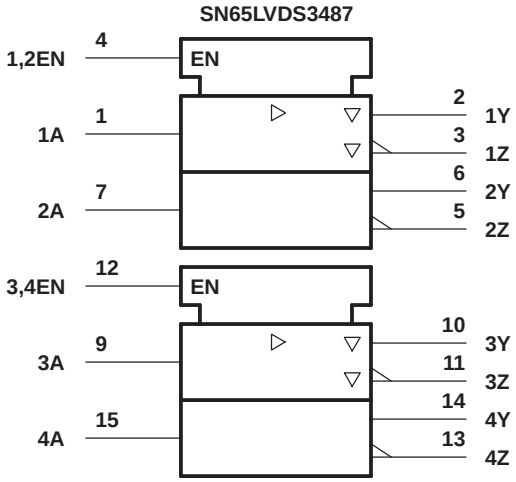


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

'LVDS31 logic diagram (positive logic)

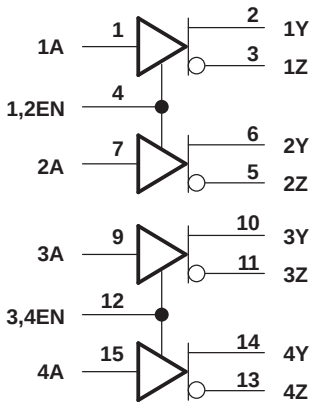


logic symbol†

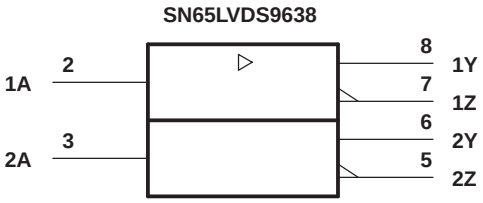


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN65LVDS3487 logic diagram (positive logic)

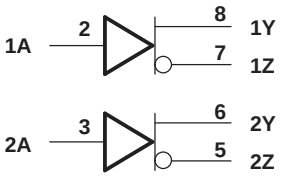


logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

SN65LVDS9638 logic diagram (positive logic)



FUNCTION TABLES

SN55LVDS31, SN65LVDS31 (1)

INPUT A	ENABLES		OUTPUTS	
	G	G	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z
Open	H	X	L	H
Open	X	L	L	H

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off)

SN65LVDS3487 (1)

INPUT A	ENABLE EN	OUTPUTS	
		Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z
Open	H	L	H

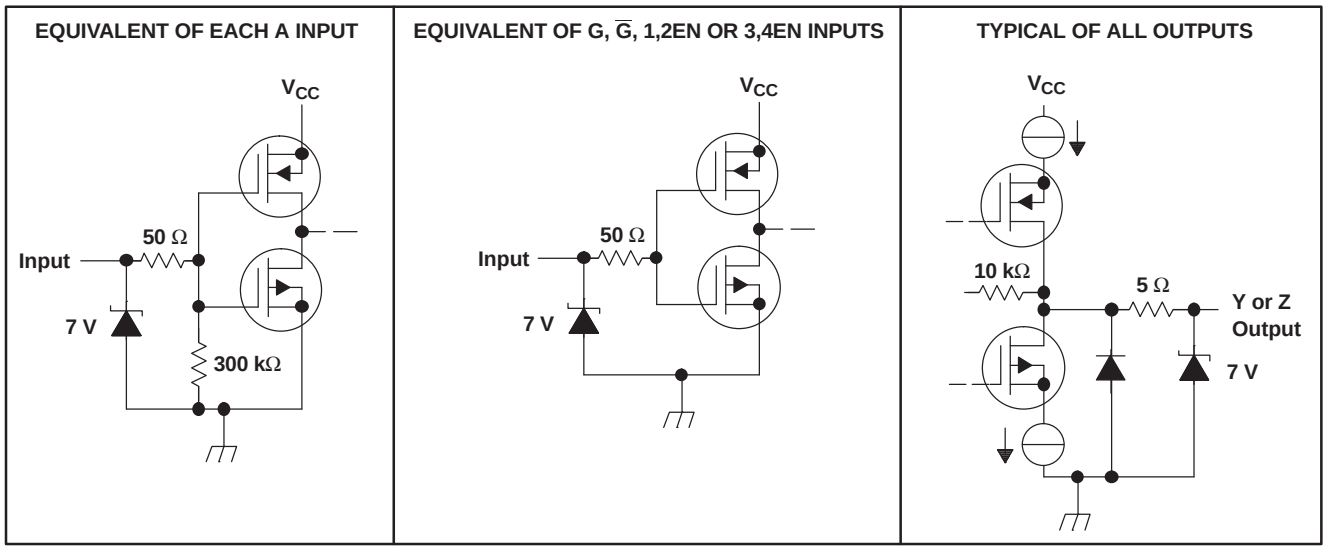
(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off)

SN65LVDS9638 (1)

INPUT A	OUTPUTS	
	Y	Z
H	H	L
L	L	H
Open	L	H

(1) H = high level, L = low level

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		UNIT
V_{CC}	Supply voltage range(2)	–0.5 V to 4 V
V_I	Input voltage range	–0.5 V to V_{CC} + 0.5 V
	Continuous total power dissipation	See Dissipation Rating Table
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C
T_{stg}	Storage temperature range	–65°C to 150°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages, except differential I/O bus voltages, are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR(1) ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D (8)	725 mW	5.8 mW/°C	464 mW	377 mW	—
D (16)	950 mW	7.6 mW/°C	608 mW	494 mW	—
DGK	425 mW	3.4 mW/°C	272 mW	221 mW	—
DGN(2)	2.14 W	17.1 mW/°C	1.37 W	1.11 W	—
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
PW (16)	774 mW	6.2 mW/°C	496 mW	402 mW	—
W	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.
(2) The PowerPAD™ must be soldered to a thermal land on the printed-circuit board. See the application note *PowerPAD Thermally Enhanced Package* (SLMA002).

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	3.3	3.6	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
T_A	Operating free-air temperature	SN65 prefix	–40		85	°C
		SN55 prefix	–55		125	

SN55LVDS31 ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{OD}	Differential output voltage magnitude	R_L = 100 Ω,	See Figure 2	247	340	454	mV
ΔV_{OD}	Change in differential output voltage magnitude between logic states	R_L = 100 Ω,	See Figure 2	–50		50	mV
$V_{OC(SS)}$	Steady-state common-mode output voltage	See Figure 3		1.125	1.2	1.375	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states	See Figure 3		–50		50	mV
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage	See Figure 3			50	150	mV
I_{CC}	Supply current	V_I = 0.8 V or 2 V,	Enabled, No load		9	20	mA
		V_I = 0.8 or 2 V,	R_L = 100 Ω, Enabled		25	35	
		V_I = 0 or V_{CC},	Disabled		0.25	1	
I_{IH}	High-level input current	V_{IH} = 2			4	20	µA
I_{IL}	Low-level input current	V_{IL} = 0.8 V			0.1	10	µA
I_{OS}	Short-circuit output current	$V_{O(Y)}$ or $V_{O(Z)}$ = 0			–4	–24	mA
		V_{OD} = 0				±12	
I_{OZ}	High-impedance output current	V_O = 0 or 2.4 V				±1	µA
$I_{O(OFF)}$	Power-off output current	V_{CC} = 0,	V_O = 2.4 V			±4	µA
C_i	Input capacitance				3		pF

(1) All typical values are at T_A = 25°C and with V_{CC} = 3.3 V.

SN55LVDS31 SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 100 Ω, C_L = 10 pF, See Figure 2	0.5	1.4	4	ns
t_{PHL}	Propagation delay time, high-to-low-level output		1	1.7	4.5	ns
t_r	Differential output signal rise time (20% to 80%)		0.4	0.5	1	ns
t_f	Differential output signal fall time (80% to 20%)		0.4	0.5	1	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$)			0.3	0.6	ns
$t_{sk(o)}$	Channel-to-channel output skew(2)			0.3	0.6	ns
t_{PZH}	Propagation delay time, high-impedance-to-high-level output	See Figure 4		5.4	15	ns
t_{PZL}	Propagation delay time, high-impedance-to-low-level output			2.5	15	ns
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output			8.1	17	ns
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output			7.3	15	ns

(1) All typical values are at T_A = 25°C and with V_{CC} = 3.3 V.
(2) $t_{sk(o)}$ is the maximum delay time difference between drivers on the same device.

SN65LVDSxxxx ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS		SN65LVDS31 SN65LVDS3487 SN65LVDS9638			UNIT
					MIN	TYP(1)	MAX	
V_{OD}	Differential output voltage magnitude		R_L = 100 Ω,	See Figure 2	247	340	454	mV
ΔV_{OD}	Change in differential output voltage magnitude between logic states		R_L = 100 Ω,	See Figure 2	–50		50	mV
$V_{OC(SS)}$	Steady-state common-mode output voltage		See Figure 3		1.125	1.2	1.375	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states		See Figure 3		–50		50	mV
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage		See Figure 3			50	150	mV
I_{CC}	Supply current	SN65LVDS31, SN65LVDS3487	V_I = 0.8 V or 2 V,	Enabled, No load		9	20	mA
			V_I = 0.8 or 2 V,	R_L = 100 Ω, Enabled		25	35	
			V_I = 0 or V_{CC},	Disabled		0.25	1	
		SN65LVDS9638	V_I = 0.8 V or 2 V	No load		4.7	8	mA
				R_L = 100 Ω		9	13	
I_{IH}	High-level input current		V_{IH} = 2			4	20	μA
I_{IL}	Low-level input current		V_{IL} = 0.8 V			0.1	10	μA
I_{OS}	Short-circuit output current		$V_{O(Y)}$ or $V_{O(Z)}$ = 0			–4	–24	mA
			V_{OD} = 0				±12	
I_{OZ}	High-impedance output current		V_O = 0 or 2.4 V				±1	μA
$I_{O(OFF)}$	Power-off output current		V_{CC} = 0,	V_O = 2.4 V			±1	μA
C_i	Input capacitance					3		pF

(1) All typical values are at T_A = 25°C and with V_{CC} = 3.3 V.

SN65LVDSxxxx SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN65LVDS31 SN65LVDS3487 SN65LVDS9638			UNIT
			MIN	TYP(1)	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 100 Ω, C_L = 10 pF, See Figure 2	0.5	1.4	2	ns
t_{PHL}	Propagation delay time, high-to-low-level output		1	1.7	2.5	ns
t_r	Differential output signal rise time (20% to 80%)		0.4	0.5	0.6	ns
t_f	Differential output signal fall time (80% to 20%)		0.4	0.5	0.6	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$)			0.3	0.6	ns
$t_{sk(o)}$	Channel-to-channel output skew(2)			0	0.3	ns
$t_{sk(pp)}$	Part-to-part skew(3)				800	ps
t_{PZH}	Propagation delay time, high-impedance-to-high-level output	See Figure 4		5.4	15	ns
t_{PZL}	Propagation delay time, high-impedance-to-low-level output			2.5	15	ns
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output			8.1	15	ns
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output			7.3	15	ns

(1) All typical values are at T_A = 25°C and with V_{CC} = 3.3 V.
(2) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, same temperature, and have identical packages and test circuits.

PARAMETER MEASUREMENT INFORMATION

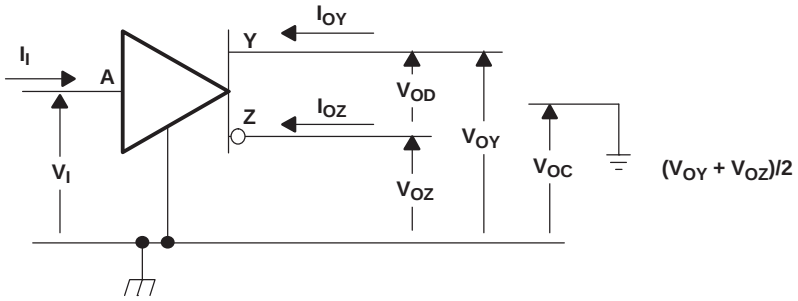
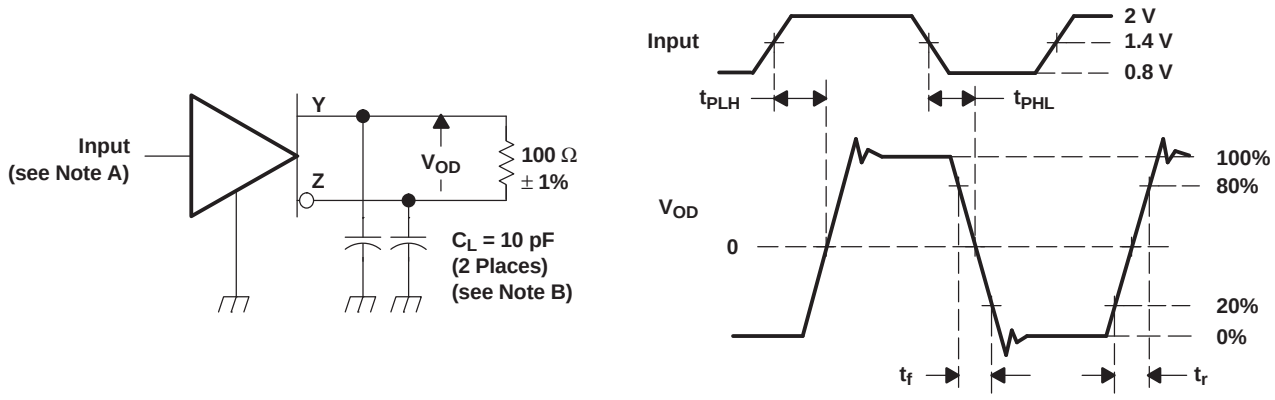
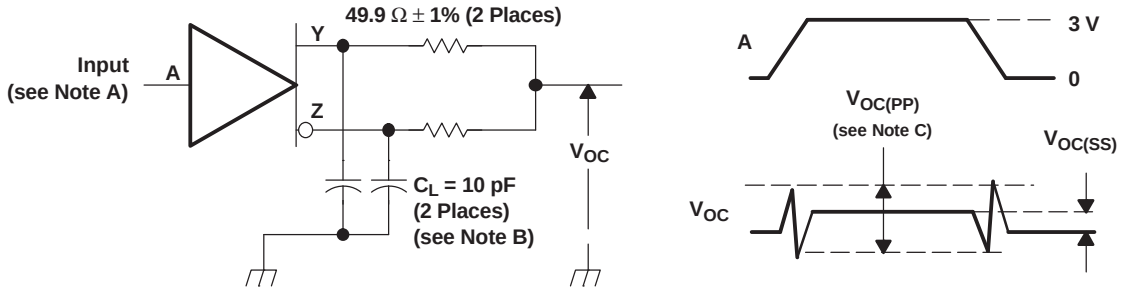


Figure 1. Voltage and Current Definitions



NOTES: A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns.
B. C_L includes instrumentation and fixture capacitance within 6 mm of the D.U.T.

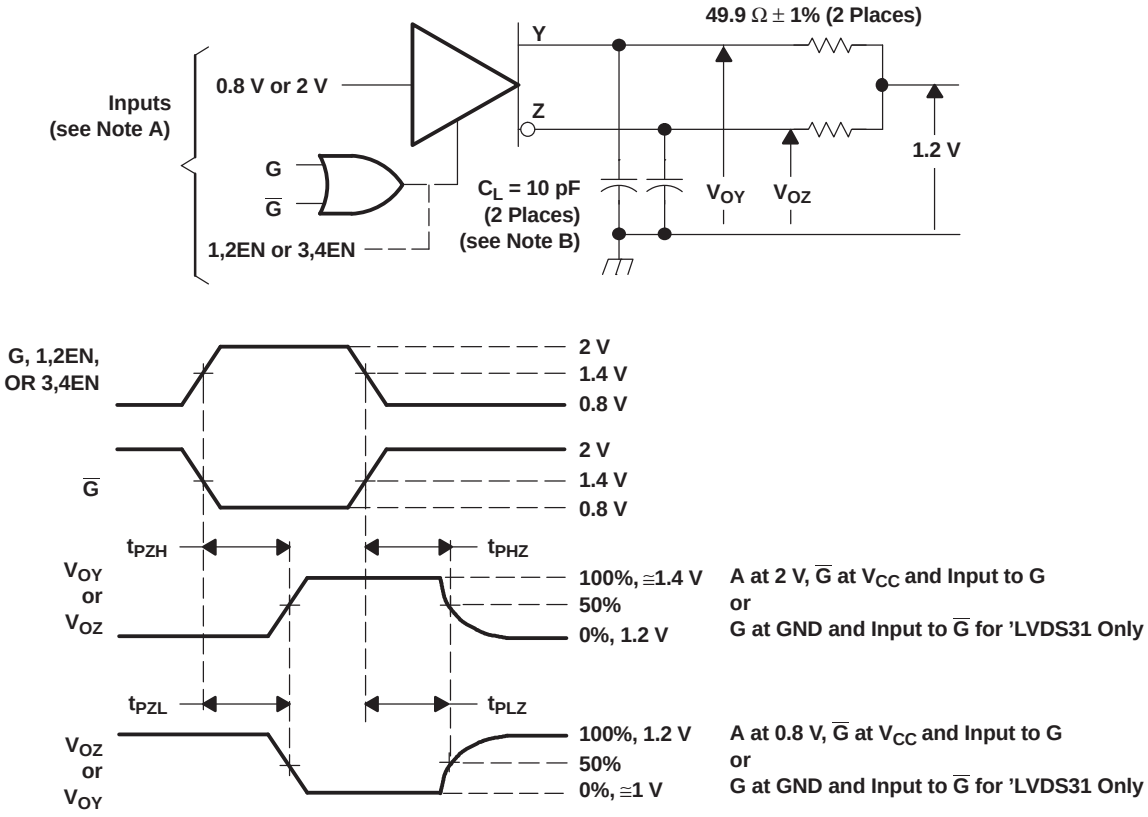
Figure 2. Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal



NOTES: A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns.
B. C_L includes instrumentation and fixture capacitance within 6 mm of the D.U.T.
C. The measurement of $V_{OC(PP)}$ is made on test equipment with a –3-dB bandwidth of at least 300 MHz.

Figure 3. Test Circuit and Definitions for the Driver Common-Mode Output Voltage

PARAMETER MEASUREMENT INFORMATION (continued)



NOTES: A. All input pulses are supplied by a generator having the following characteristics: t_r or t_f < 1 ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns.
B. C_L includes instrumentation and fixture capacitance within 6 mm of the D.U.T.

Figure 4. Enable-/Disable-Time Circuit and Definitions

TYPICAL CHARACTERISTICS

**SN55LVDS31, SN65LVDS31
SUPPLY CURRENT
vs
FREQUENCY**

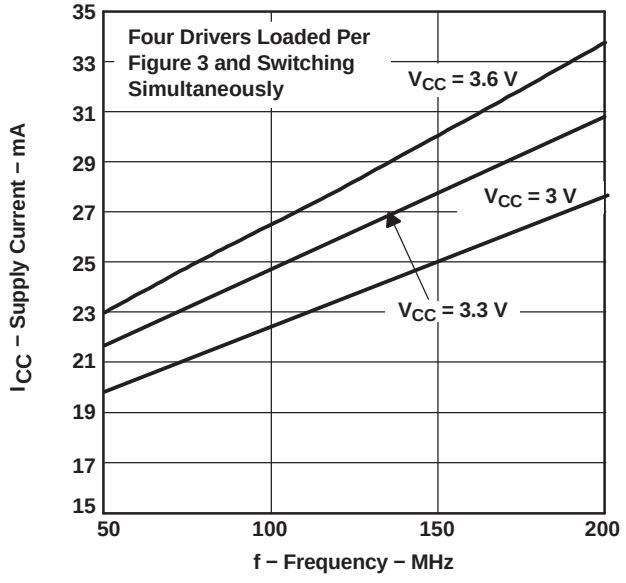


Figure 5.

**LOW-TO-HIGH PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE**

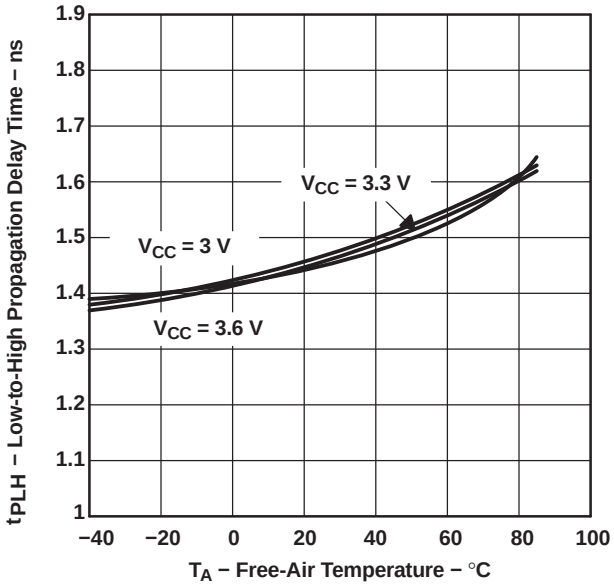


Figure 6.

**HIGH-TO-LOW PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE**

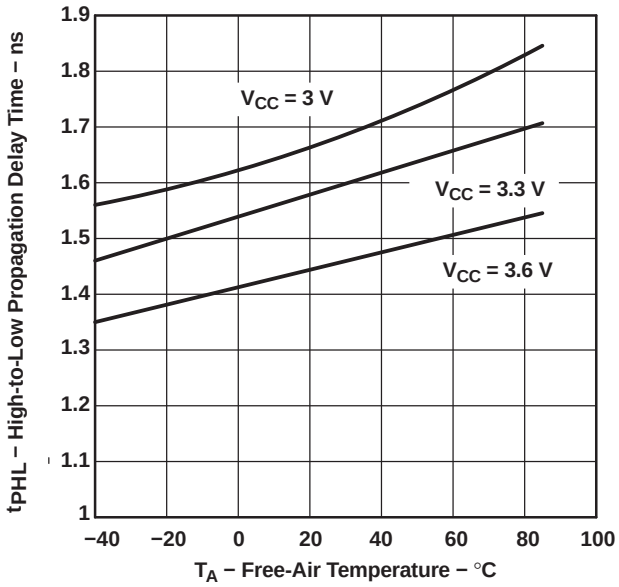
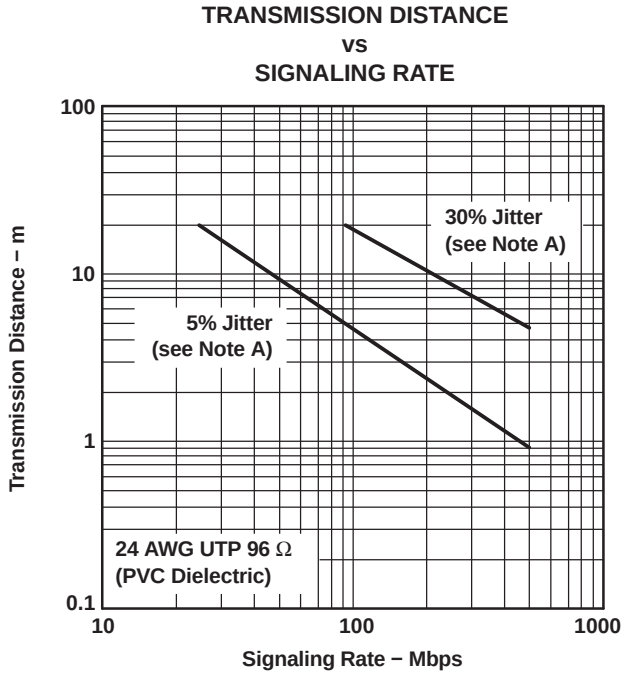


Figure 7.

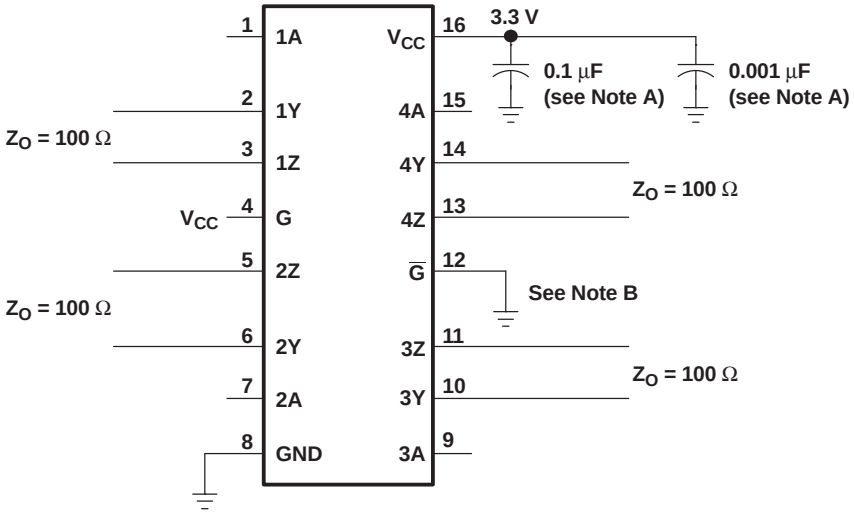
APPLICATION INFORMATION

The devices are generally used as building blocks for high-speed point-to-point data transmission where ground differences are less than 1 V. Devices can interoperate with RS-422, PECL, and IEEE-P1596. Drivers/receivers approach ECL speeds without the power and dual supply requirements.



A. This parameter is the percentage of distortion of the unit interval (UI) with a pseudorandom data pattern.

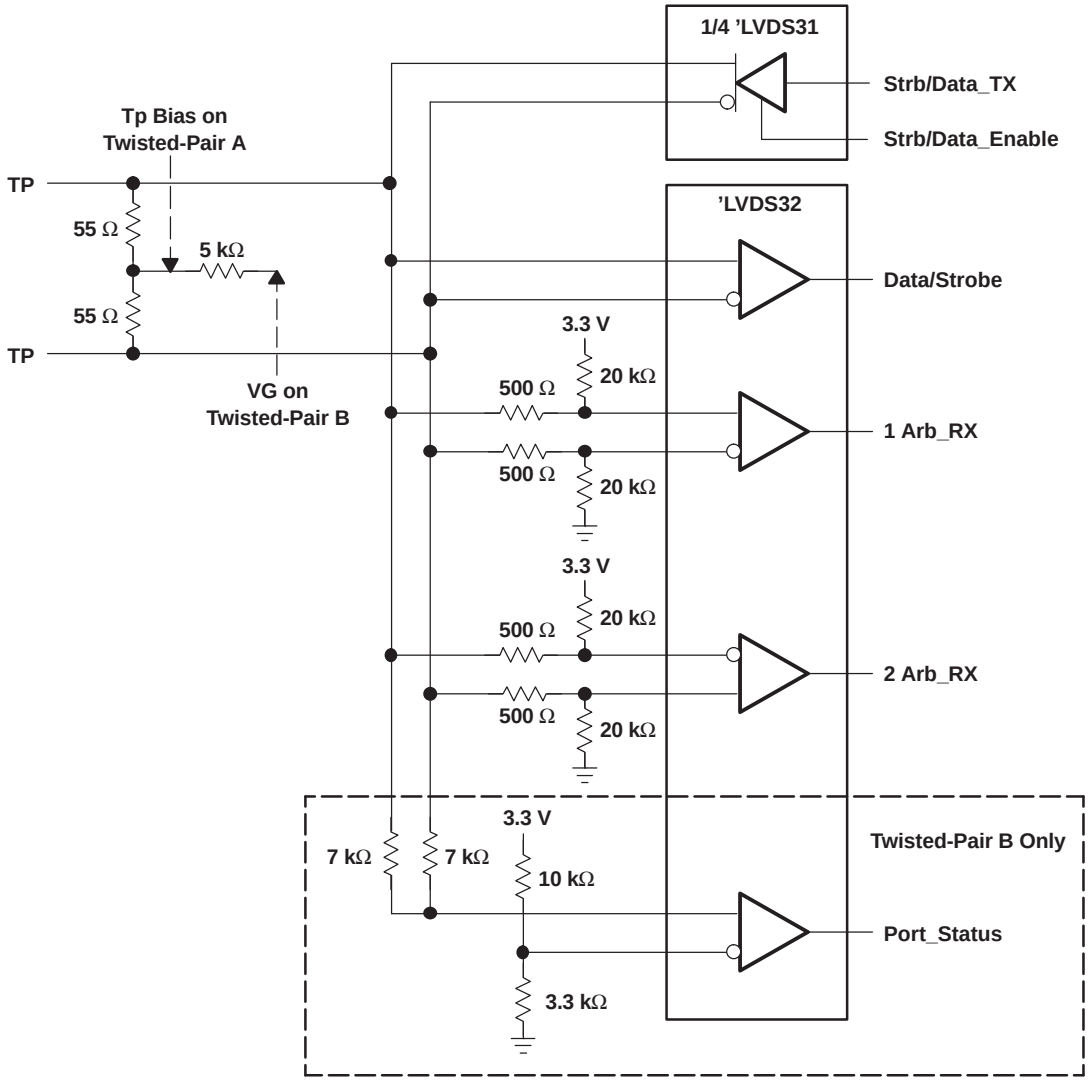
Figure 8. Typical Transmission Distance Versus Signaling Rate



NOTES: A. Place a 0.1-μF and a 0.001-μF Z5U ceramic, mica, or polystyrene dielectric, 0805 size, chip capacitor between V_{CC} and the ground plane. The capacitors should be located as close as possible to the device terminals.
B. Unused enable inputs should be tied to V_{CC} or GND, as appropriate.

Figure 9. Typical Application Circuit Schematic

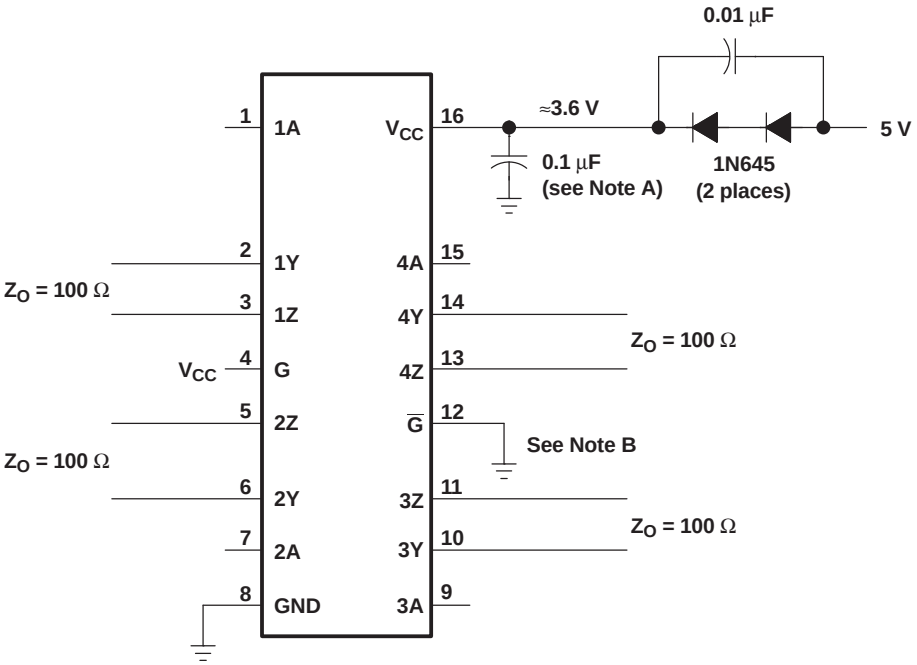
APPLICATION INFORMATION (continued)



NOTES: A. Resistors are leadless, thick film (0603), 5% tolerance.
B. Decoupling capacitance is not shown, but recommended.
C. V_{CC} is 3 V to 3.6 V.
D. The differential output voltage of the 'LVDS31 can exceed that specified by IEEE1394.

Figure 10. 100-Mbps IEEE 1394 Transceiver

APPLICATION INFORMATION (continued)



A. Place a 0.1-µF Z5U ceramic, mica, or polystyrene dielectric, 0805 size, chip capacitor between V_{CC} and the ground plane. The capacitor should be located as close as possible to the device terminals.

B. Unused enable inputs should be tied to V_{CC} or GND, as appropriate.

Figure 11. Operation With 5-V Supply

COLD SPARING

Systems using cold sparing have a redundant device electrically connected without power supplied. To support this configuration, the spare must present a high-input impedance to the system so that it does not draw appreciable power. In cold sparing, voltage may be applied to an I/O before and during power up of a device. When the device is powered off, V_{CC} must be clamped to ground and the I/O voltages applied must be within the specified recommended operating conditions.

RELATED INFORMATION

IBIS modeling is available for this device. Contact the local TI sales office or the TI Web site at www.ti.com for more information.

For more application guidelines, see the following documents:

- *Low-Voltage Differential Signaling Design Notes* (SLLA014)
- *Interface Circuits for TIA/EIA-644* (LVDS) (SLLA038)
- *Reducing EMI With LVDS* (SLLA030)
- *Slew Rate Control of LVDS Circuits* (SLLA034)
- *Using an LVDS Receiver With RS-422 Data* (SLLA031)
- *Evaluating the LVDS EVM* (SLLA033)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9762101Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9762101Q2A SNJ55LVDS31FK	Samples
5962-9762101QEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9762101QEA SNJ55LVDS31J	Samples
5962-9762101QFA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9762101QFA SNJ55LVDS31W	Samples
SN55LVDS31W	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN55LVDS31W	Samples
SN65LVDS31D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS31	Samples
SN65LVDS31DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS31	Samples
SN65LVDS31DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS31	Samples
SN65LVDS31DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS31	Samples
SN65LVDS31NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS31	Samples
SN65LVDS31NSRG4	ACTIVE	SO	NS	16		TBD	Call TI	Call TI	-40 to 85		Samples
SN65LVDS31PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS31	Samples
SN65LVDS31PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS31	Samples
SN65LVDS31PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS31	Samples
SN65LVDS31PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS31	Samples
SN65LVDS31QPWQ1	OBSOLETE	TSSOP	PW	16		TBD	Call TI	Call TI	-40 to 125		
SN65LVDS31QPWRQ1	OBSOLETE	TSSOP	PW	16		TBD	Call TI	Call TI	-40 to 125		

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65LVDS3487D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS3487	Samples
SN65LVDS3487DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS3487	Samples
SN65LVDS3487DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS3487	Samples
SN65LVDS3487DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVDS3487	Samples
SN65LVDS9638D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	DK638	Samples
SN65LVDS9638DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	DK638	Samples
SN65LVDS9638DGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AXG	Samples
SN65LVDS9638DGKG4	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AXG	Samples
SN65LVDS9638DGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AXG	Samples
SN65LVDS9638DGKRG4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AXG	Samples
SN65LVDS9638DGN	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	L38	Samples
SN65LVDS9638DGNR	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	L38	Samples
SN65LVDS9638DGNRG4	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	L38	Samples
SN65LVDS9638DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	DK638	Samples
SN65LVDS9638DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	DK638	Samples
SNJ55LVDS31FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9762101Q2A SNJ55 LVDS31FK	Samples
SNJ55LVDS31J	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9762101QE A SNJ55LVDS31J	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SNJ55LVDS31W	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9762101QFA SNJ55LVDS31W	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF SN55LVDS31, SN65LVDS31 :

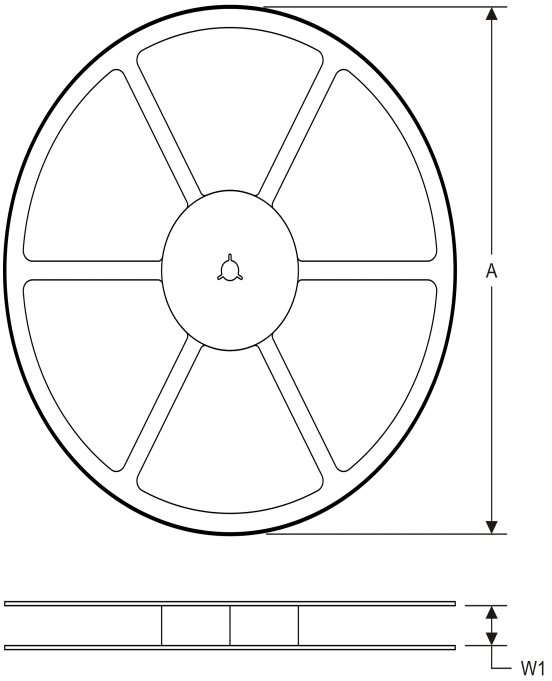
- Catalog: SN75LVDS31
- Enhanced Product: SN65LVDS31-EP
- Space: SN55LVDS31-SP

NOTE: Qualified Version Definitions:

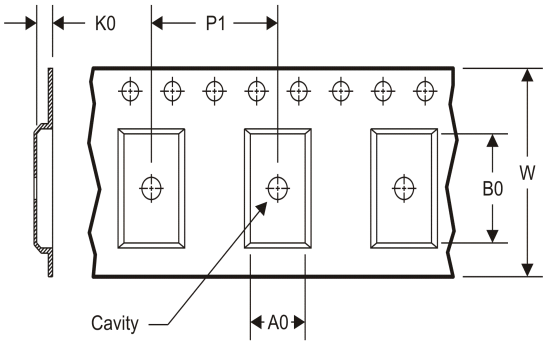
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



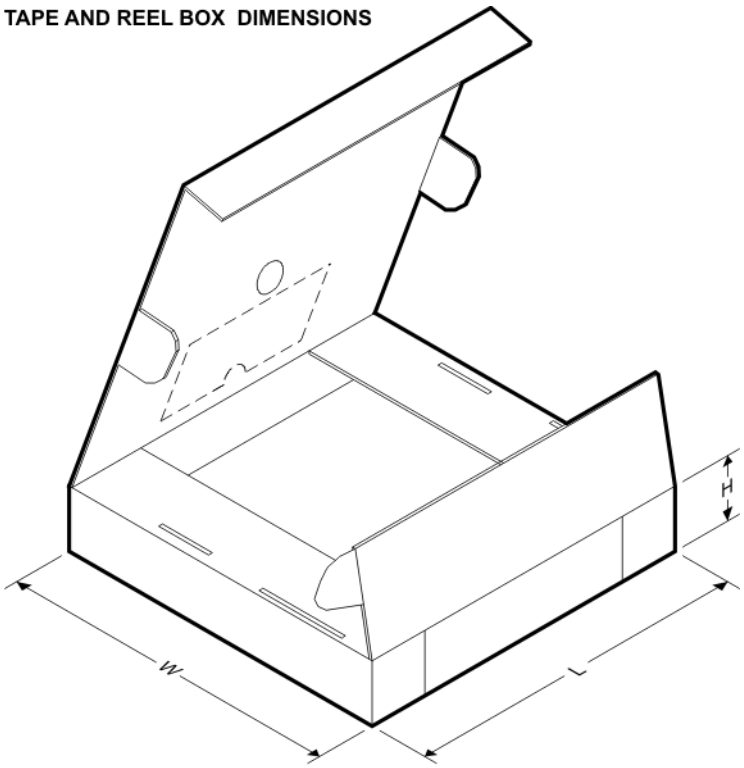
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVDS31DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN65LVDS31NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN65LVDS31PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN65LVDS3487DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN65LVDS9638DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
SN65LVDS9638DGNR	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
SN65LVDS9638DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65LVDS9638DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



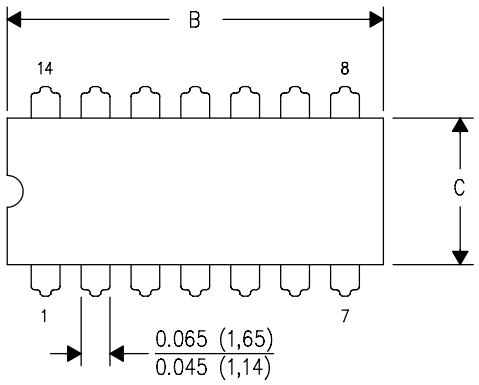
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVDS31DR	SOIC	D	16	2500	333.2	345.9	28.6
SN65LVDS31NSR	SO	NS	16	2000	367.0	367.0	38.0
SN65LVDS31PWR	TSSOP	PW	16	2000	367.0	367.0	35.0
SN65LVDS3487DR	SOIC	D	16	2500	367.0	367.0	38.0
SN65LVDS9638DGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
SN65LVDS9638DGNR	MSOP-PowerPAD	DGN	8	2500	358.0	335.0	35.0
SN65LVDS9638DR	SOIC	D	8	2500	340.5	338.1	20.6
SN65LVDS9638DR	SOIC	D	8	2500	367.0	367.0	35.0

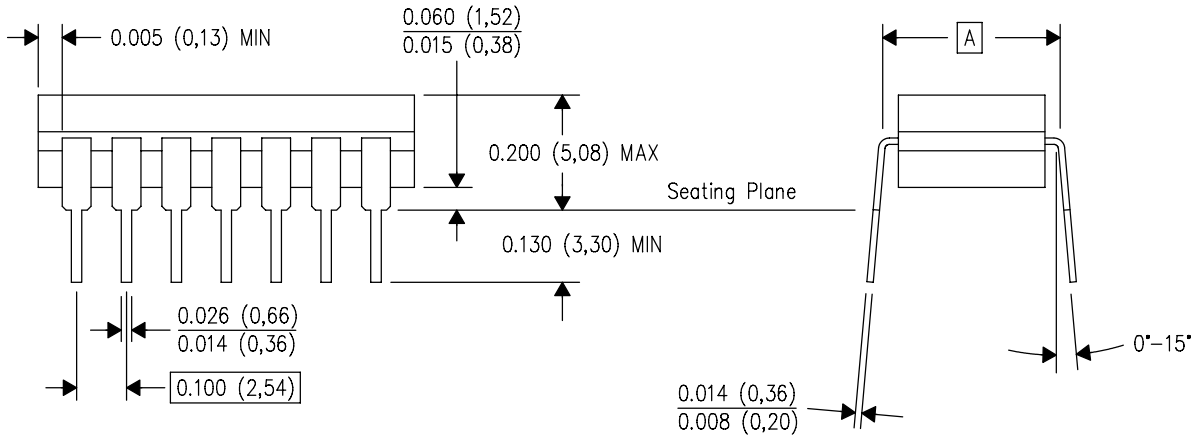
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



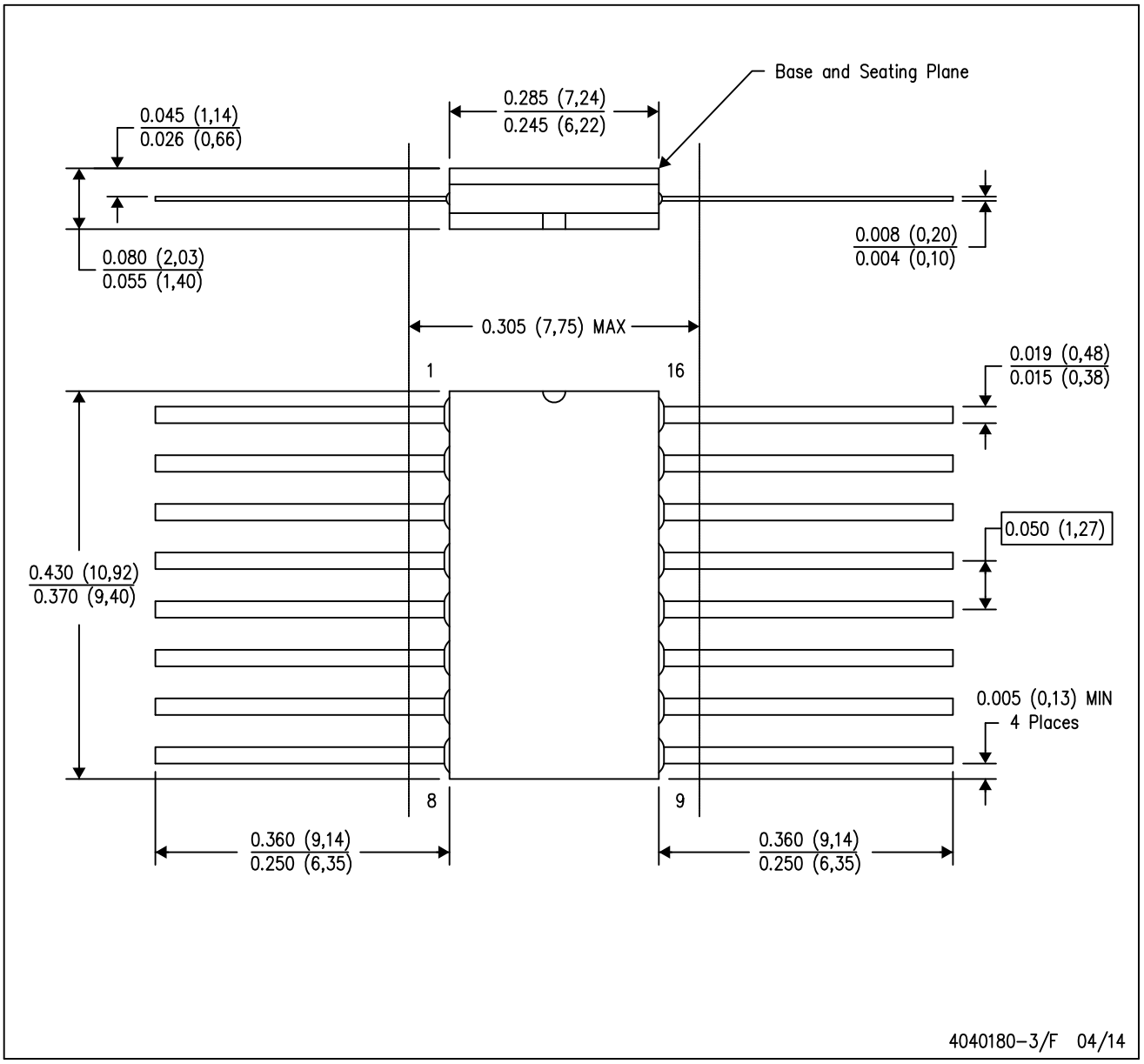
DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

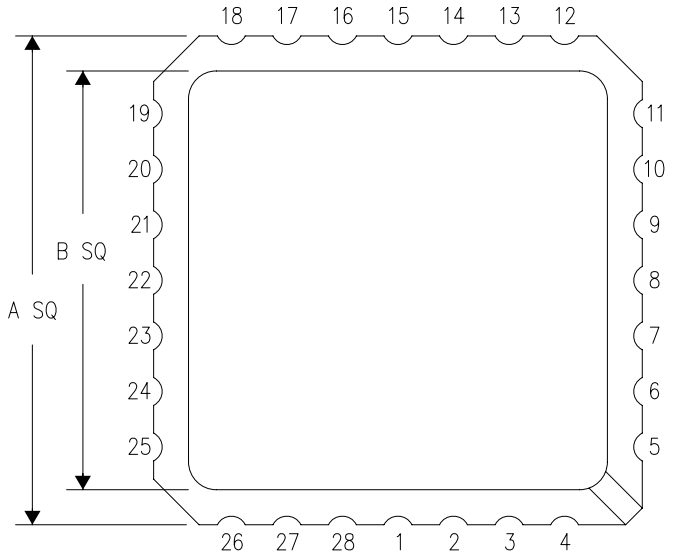
W (R–GDFP–F16) CERAMIC DUAL FLATPACK



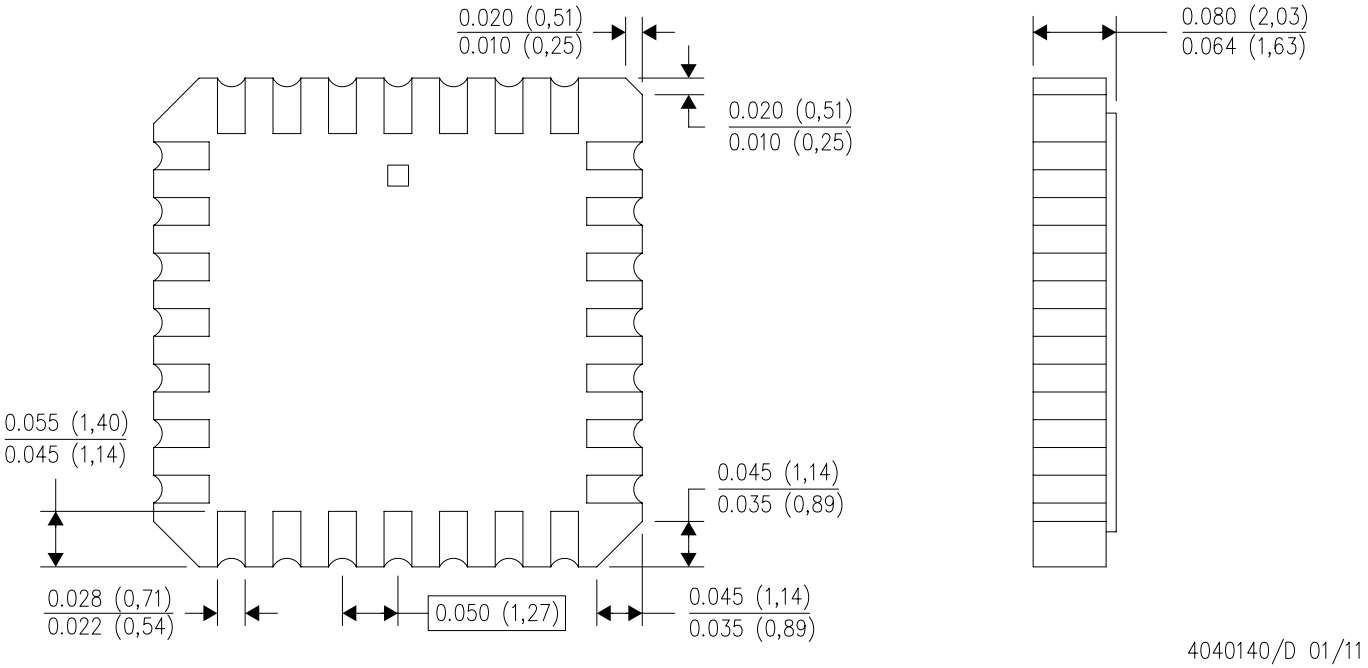
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP2–F16

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



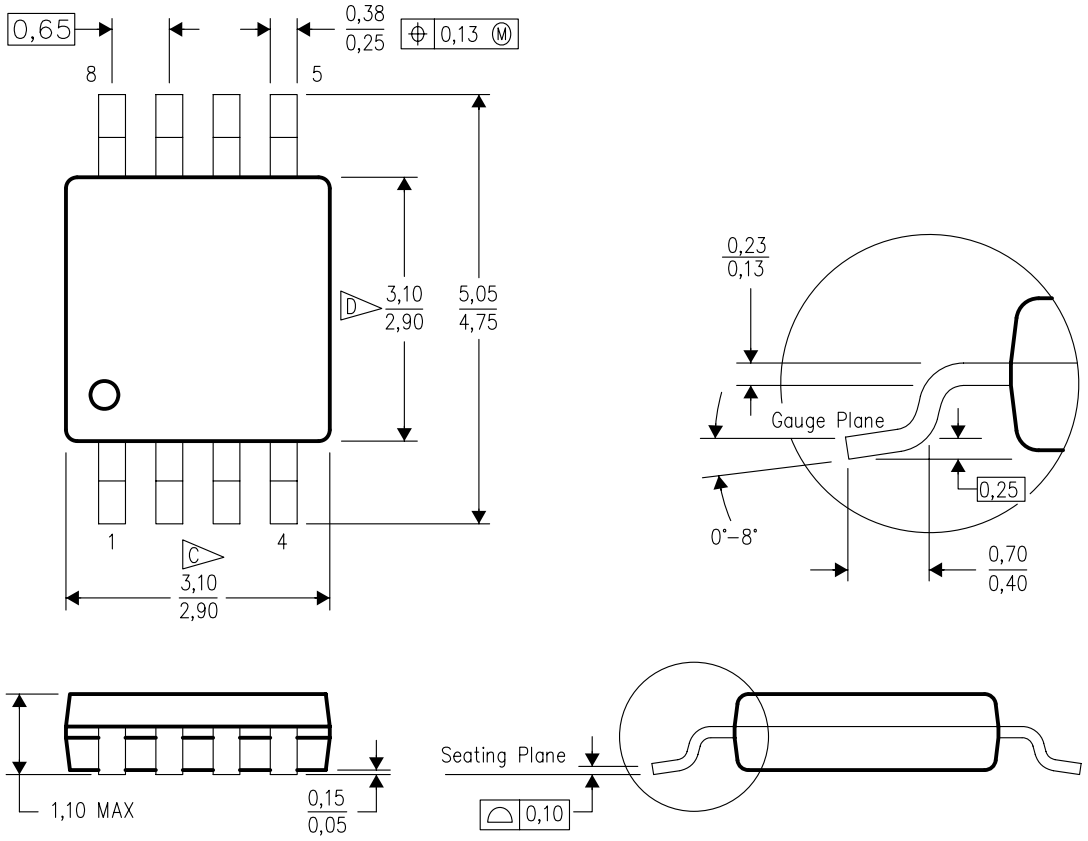
NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

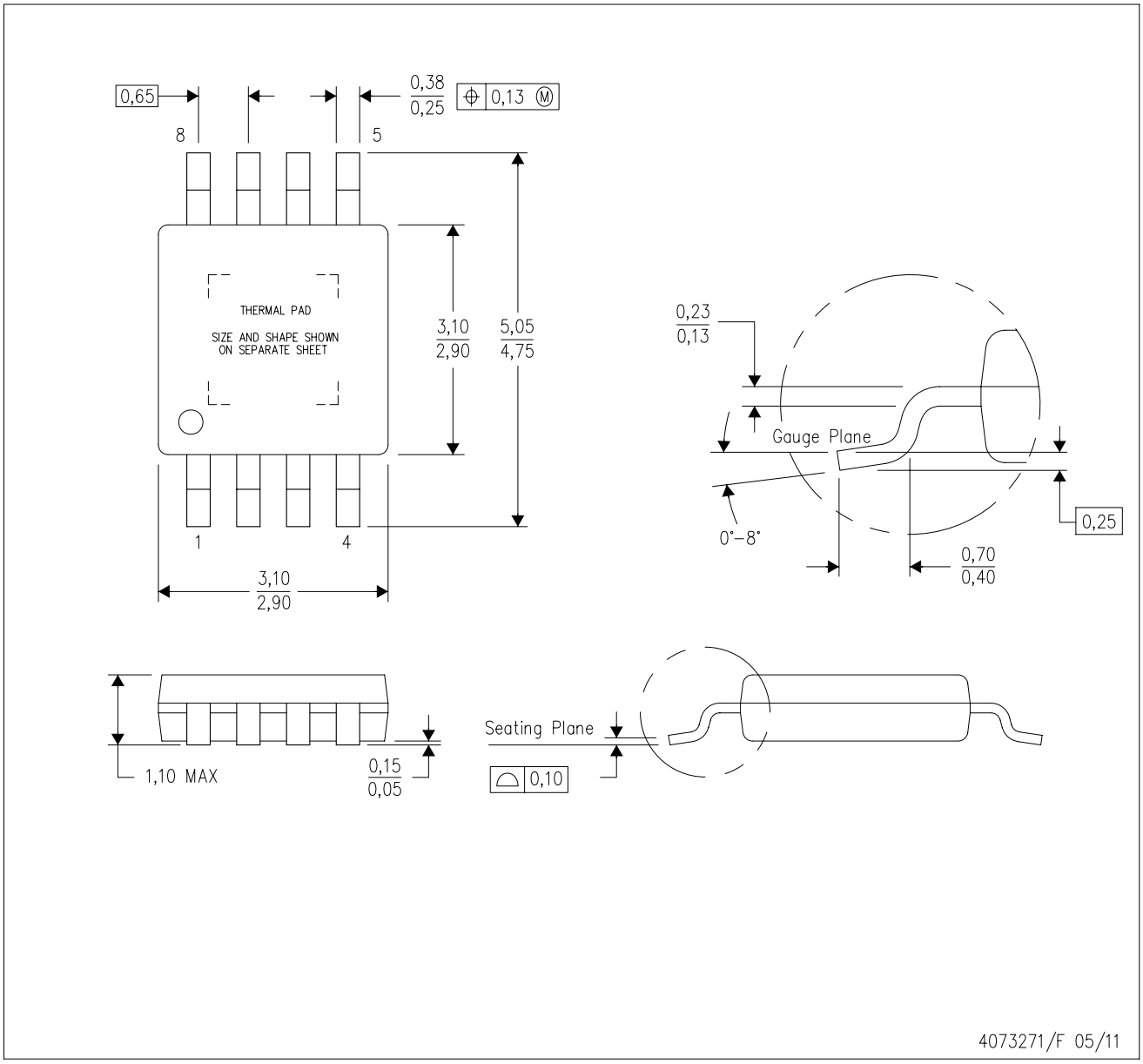
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGN (S–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–187 variation AA–T

PowerPAD is a trademark of Texas Instruments.

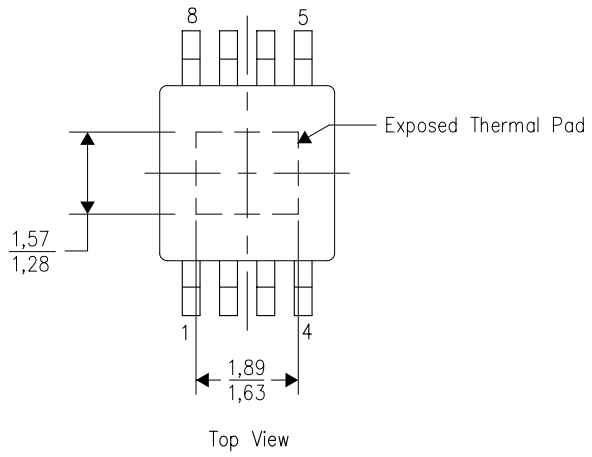
DGN (S–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

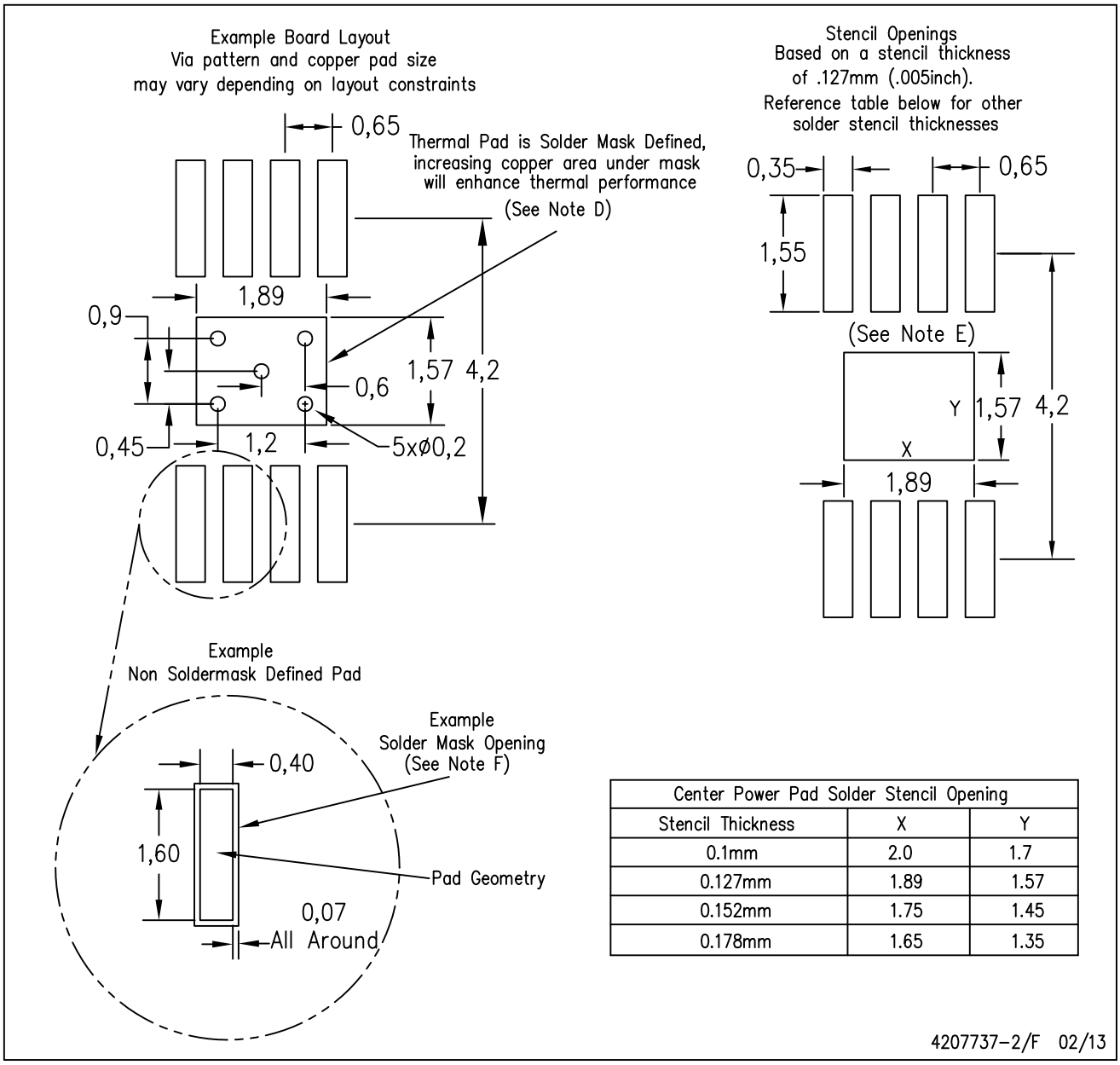
Exposed Thermal Pad Dimensions

4206323–2/I 12/11

NOTE: All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

DGN (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

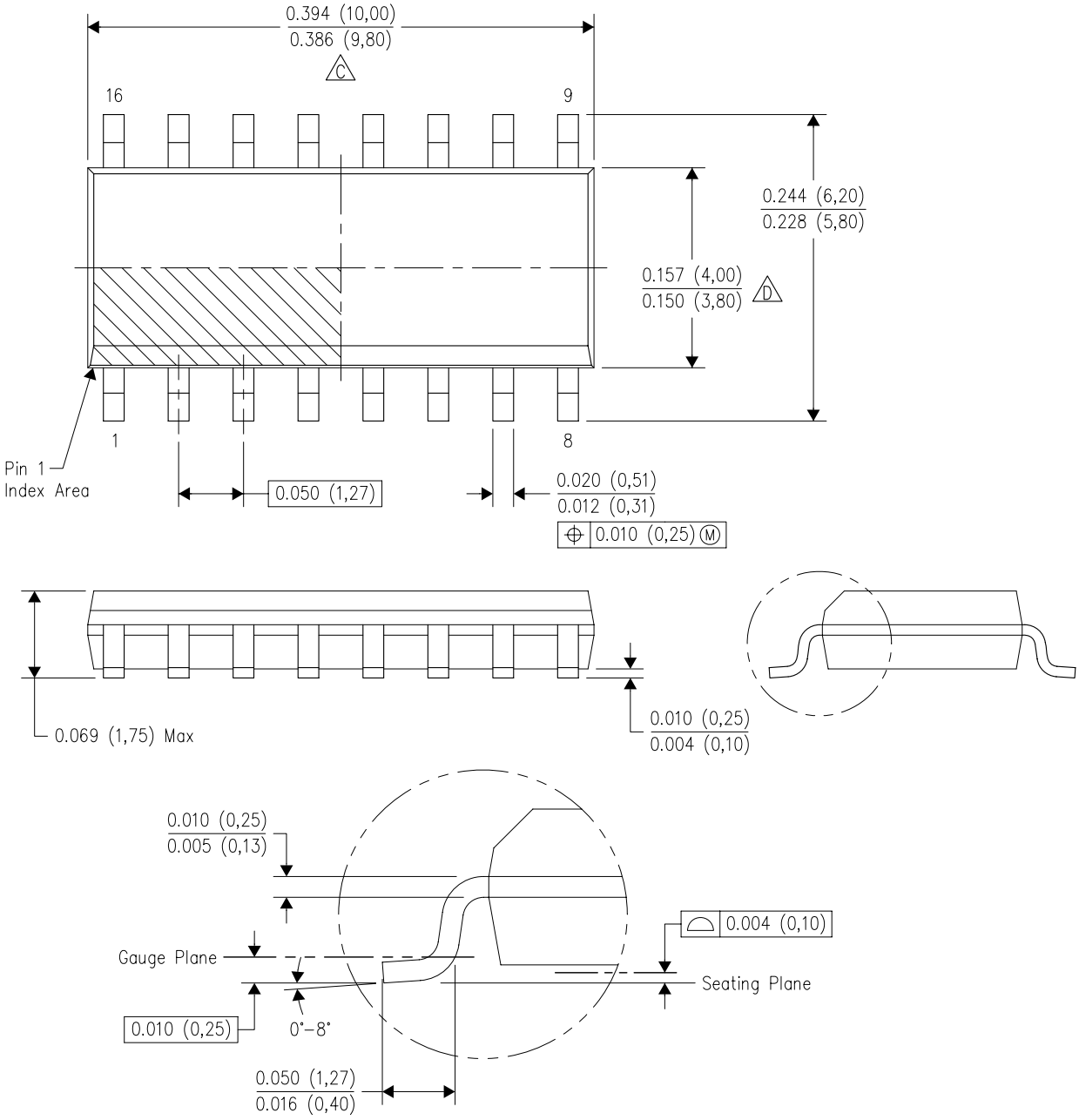


Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.0	1.7
0.127mm	1.89	1.57
0.152mm	1.75	1.45
0.178mm	1.65	1.35

4207737–2/F 02/13

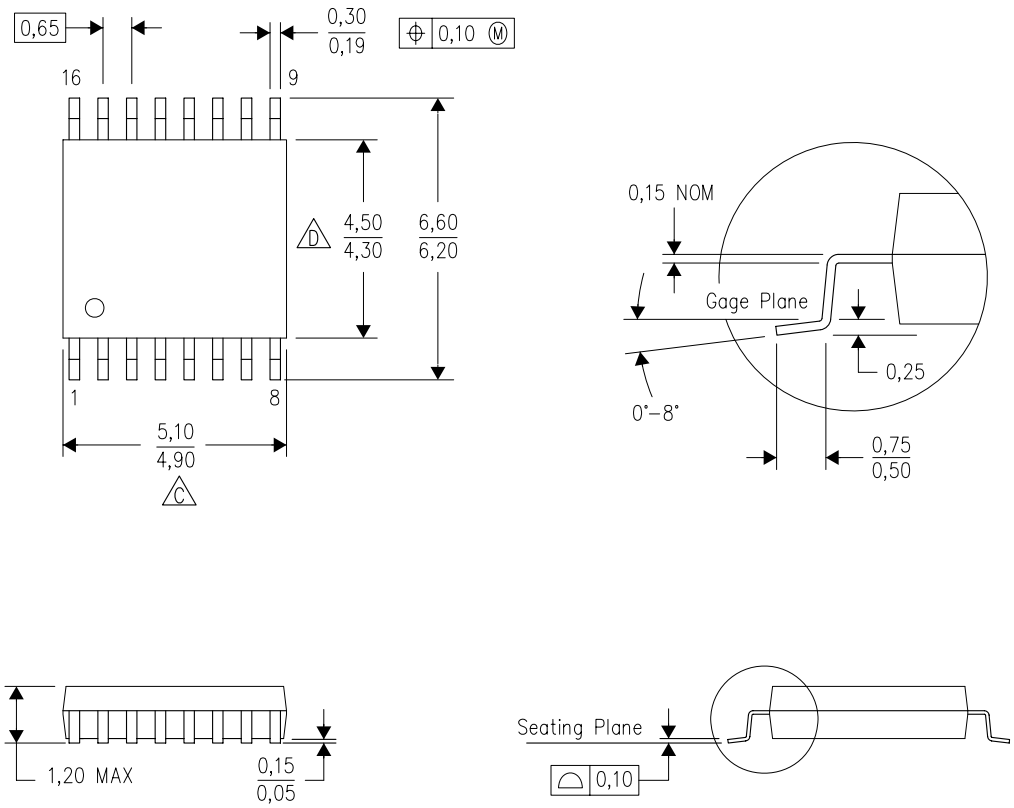
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

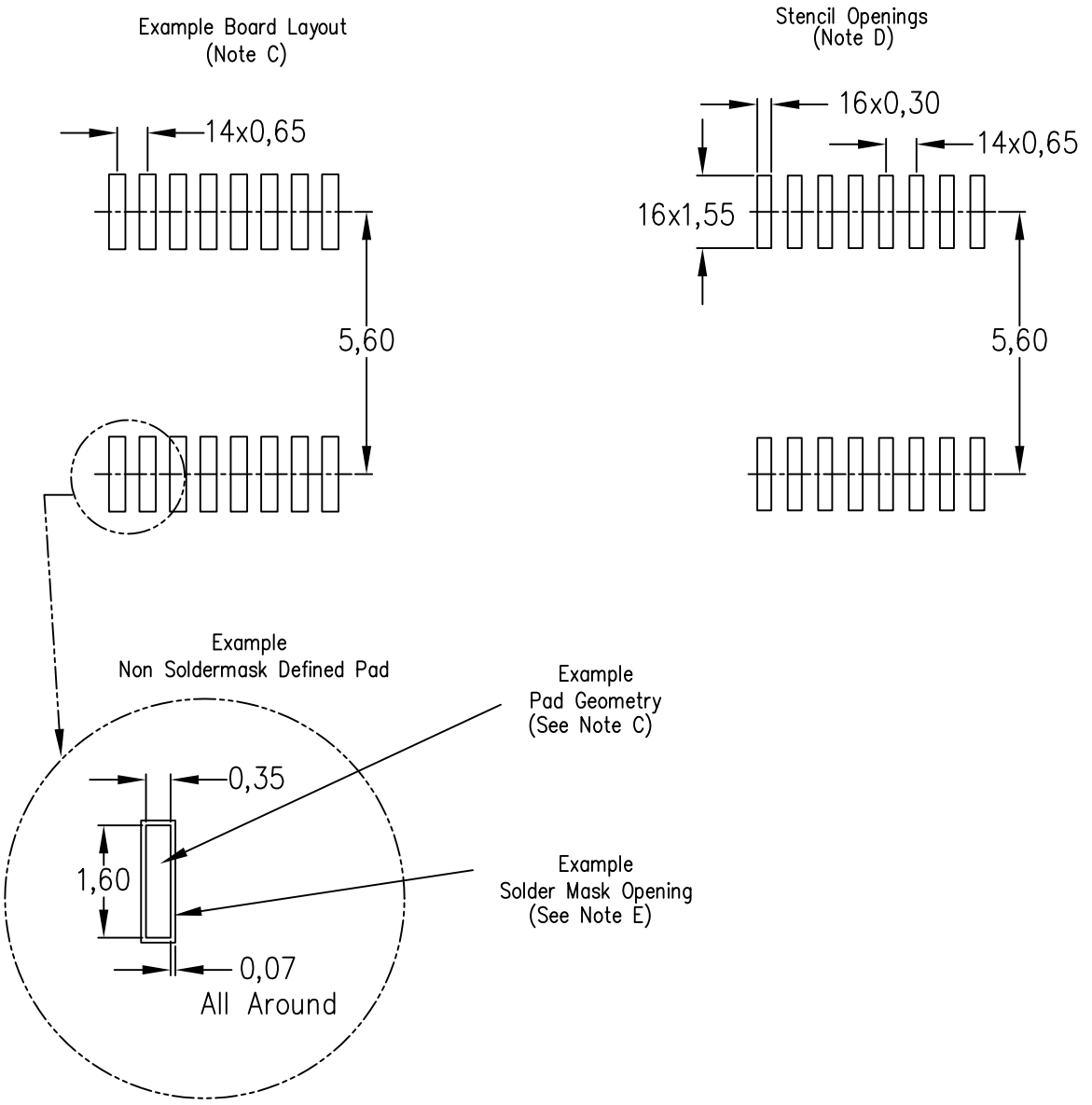
PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



4040064–4/G 02/11

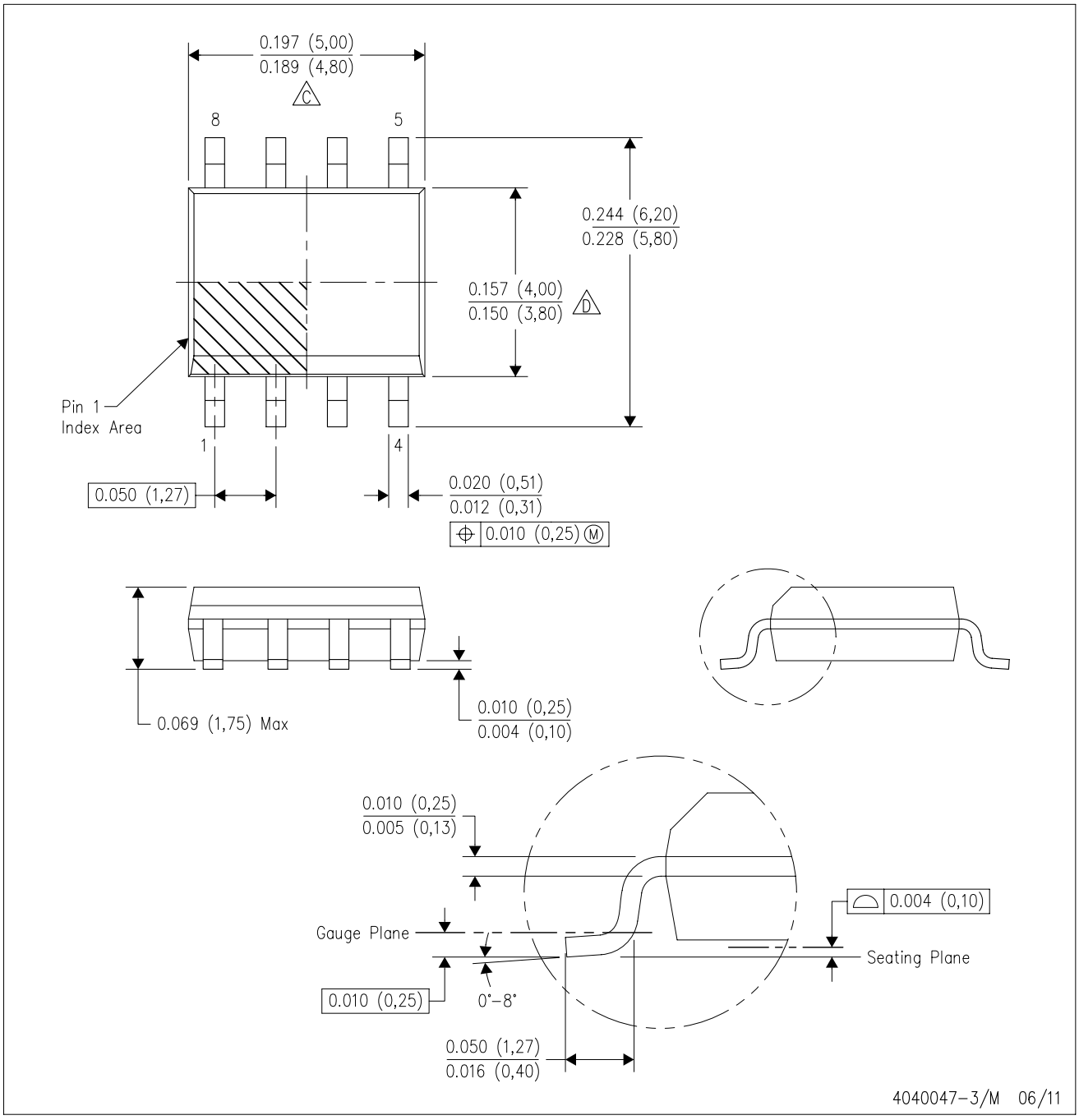
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



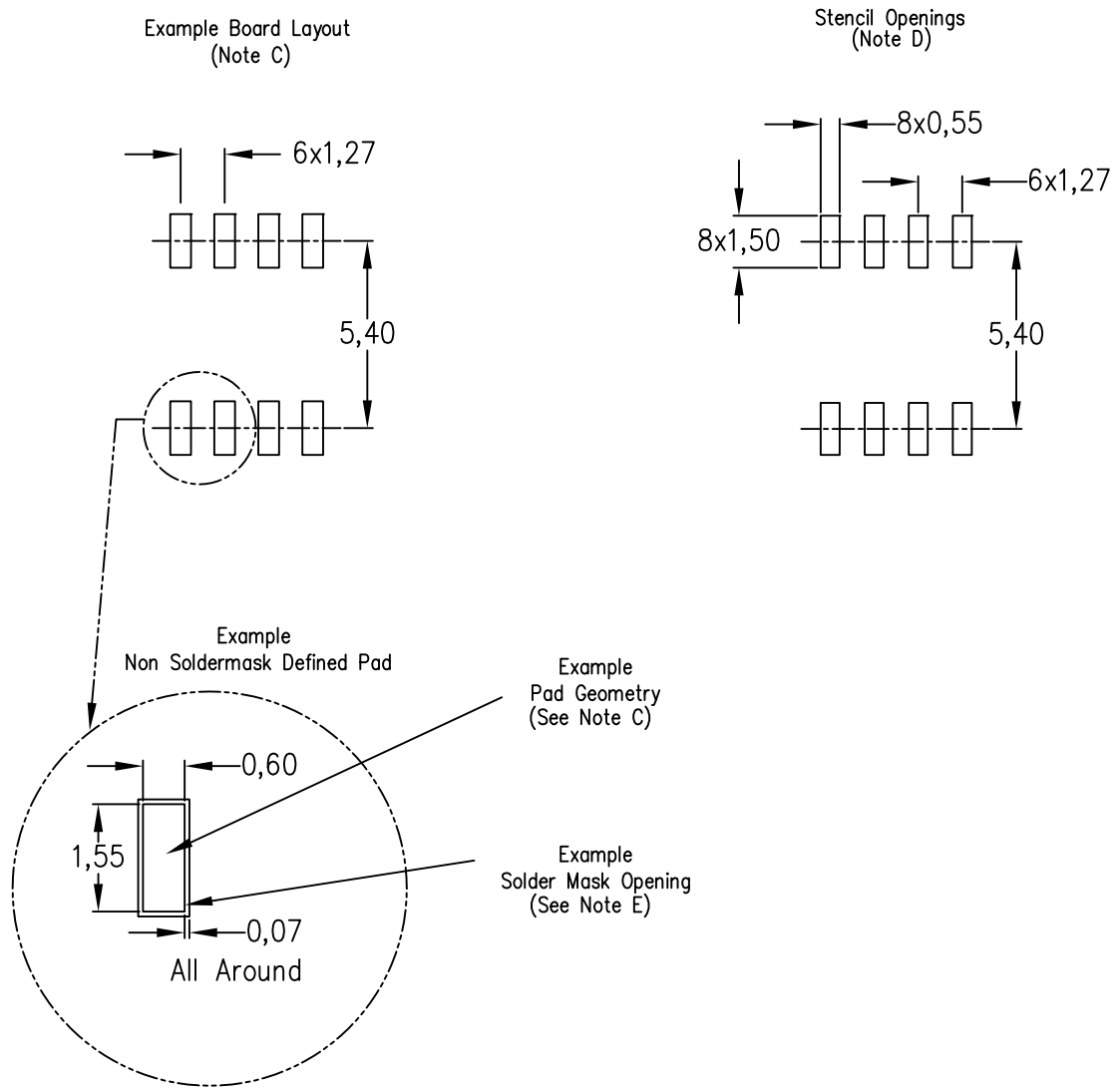
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE

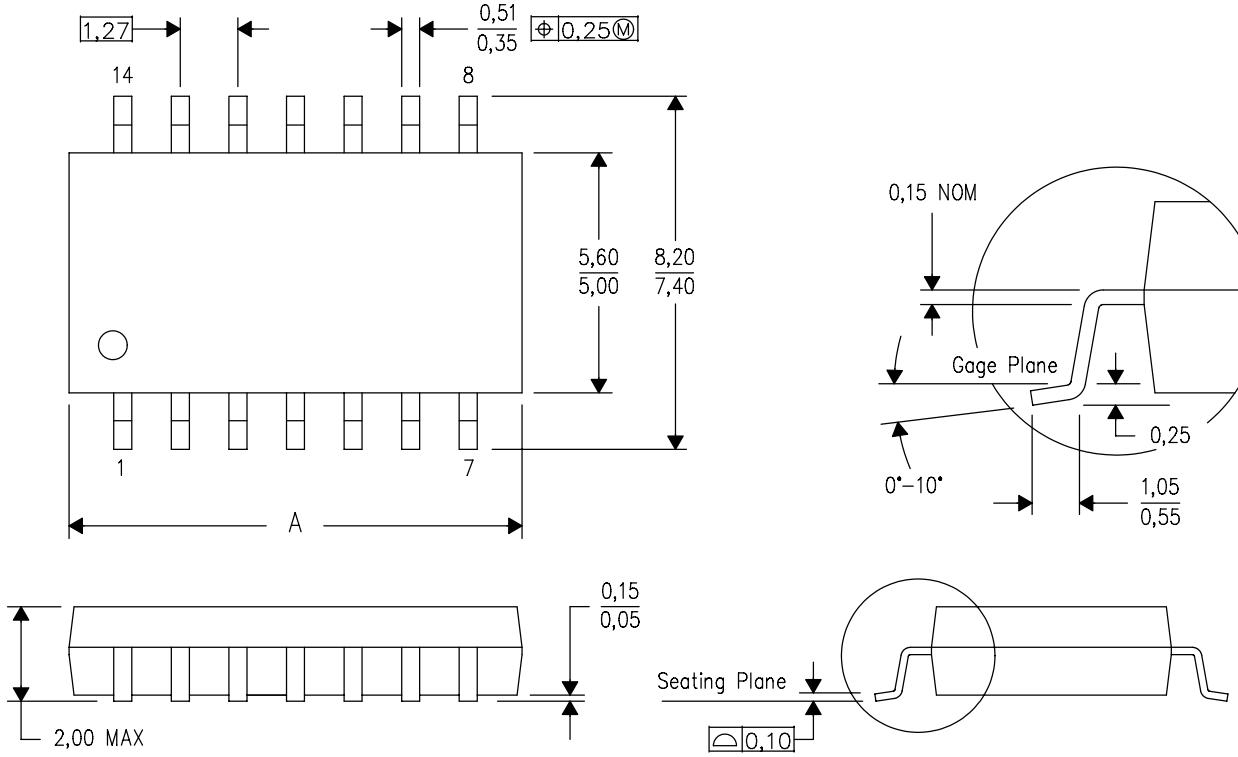


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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