Perf-V FPGA develop board
User manual
1.0

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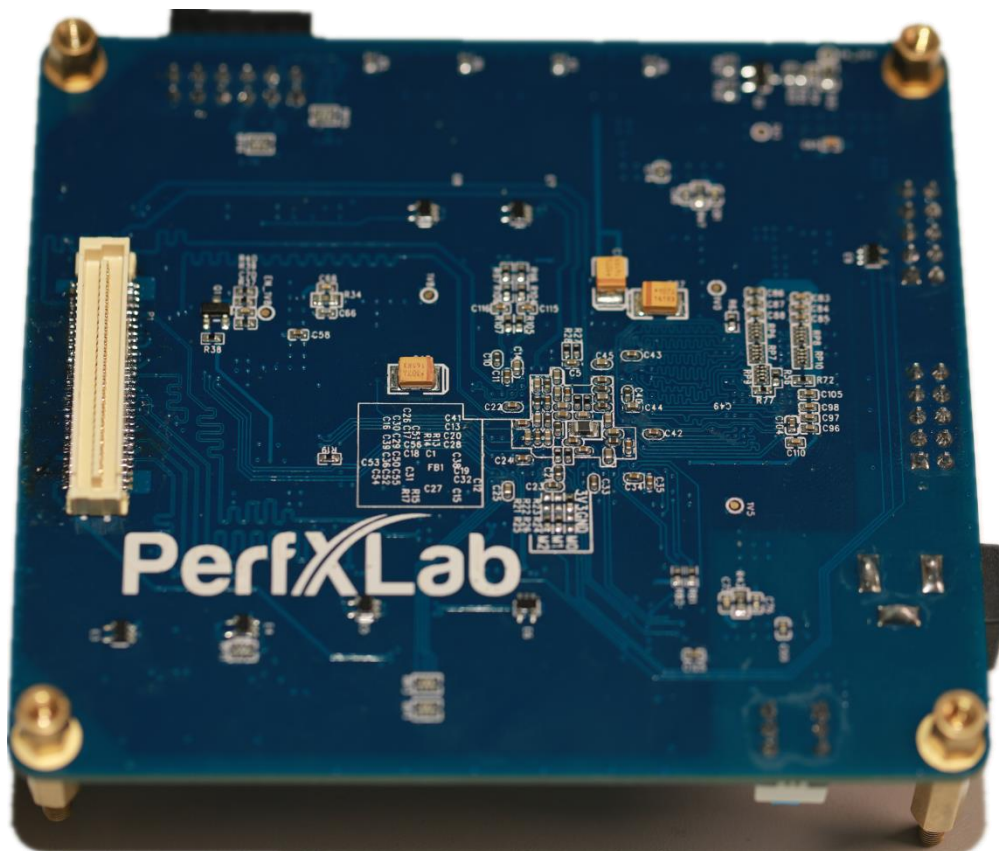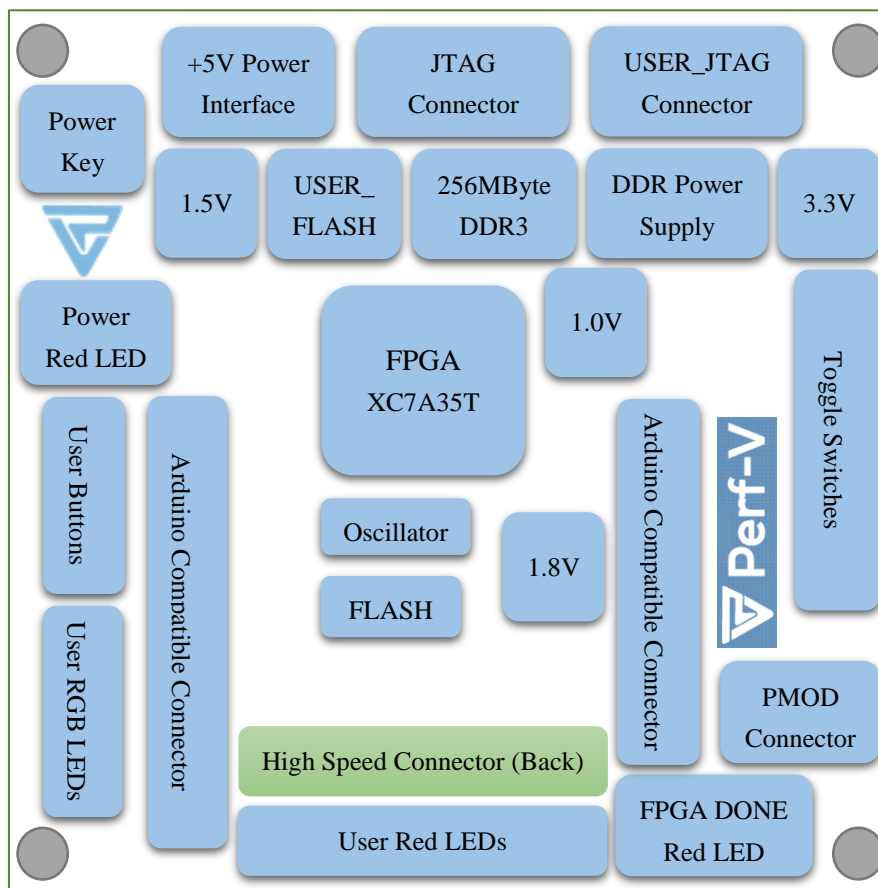
1 Development Board Overview

Front

Back

The development board is based on Xilinx Artix-7 FPGA (part number XC7A35T-1FTG256C), adopting 256-pin FBGA package. The resources of this FPGA are shown below:

| Device | Logic Cells | Configurable Logic Blocks (CLBs) | | DSP48E1 Slices[2] | Block RAM Blocks[3] | | | CMTs[4] | PCIe[5] | GTPs | XADC Blocks | Total I/O Banks[6] | Max User I/O[7] |
		Slices[1]	Max Distributed RAM (Kb)		18 Kb	36 Kb	Max (Kb)						
XA7A12T	12,800	2,000	171	40	40	20	720	3	1	2	1	3	150
XA7A15T	16,640	2,600	200	45	50	25	900	5	1	4	1	5	210
XA7A25T	23,360	3,650	313	80	90	45	1,620	3	1	4	1	3	150
XA7A35T	33,280	5,200	400	90	100	50	1,800	5	1	4	1	5	210
XA7A50T	52,160	8,150	600	120	150	75	2,700	5	1	4	1	5	210
XA7A75T	75,520	11,800	892	180	210	105	3,780	6	1	4	1	6	285
XA7A100T	101,440	15,850	1,188	240	270	135	4,860	6	1	4	1	6	285

Main parameters:
- Logic Cells: 33280;
- DSP48E1 Slices: 90;
- Configurable Logic Blocks (CLBs): 400Kb;
- Block RAM Blocks: 1800Kb;
- Clock Management Tiles (CMTs): 5;
- Max User I/O: 210;
- Core Voltage: 1.0V;
- Temperature Range: 0 to 85℃;

The structure diagram of the whole system:

Size	85mm*95mm
FPGA	XC7A35T-1FTG256C XC7A50T-1FTG256C XC7A100T-1FTG256C
FPGA External Clock Source	50MHz
FLASH and USER_FLASH	N25Q064A, 8MB (64Mbit) storage capacity, 108MHz (Max) clock frequency N25Q064A, 8MB (64Mbit) storage capacity, 108MHz (Max) clock frequency
DDR3	MT41J128M16JT, 256MB (2Gbit), 16Megx16x8Banks
LEDs	1 FPGA_DONE indicator
	1 power indicator
	3 user RGB LEDs
	4 user RED LEDs
Buttons (Switches)	1 RESET button
	4 user soft-touch buttons
	4 user toggle switches
JTAG	10-pin 2.54mm standard interface
USER_JTAG	10-pin 2.54mm standard interface
Power Supply System	5V input
	3.3V output, 1.8V output, 1.5V output, 1.0V output, 0.75V output
Connectors	1 Arduino Compatible Connector
	1 PMOD Connector
	1 High Speed Connector

2 Development Board Function Description

2.1 Artix-7 FPGA Pin Assignment

XC7A35T-1FTG256C has 5 I/0 Banks. U2E is the dedicated configuration Bank of the FPGA, the connections of the other four I/O Banks are shown in the following table.

Bank	Application
Bank14（3.3V）	LED/KEY/P1/P2
Bank15（3.3V）	P1/P2/JP1
Bank34（3.3V）	USER_JTAG/USER_FLASH/P1
Bank35（1.5V）	DDR3

2.2 Expansion Connectors

The development board has three user connectors: P1, P2 and JP1.

2.2.1 P1 (High Speed) Connector

P1 is a high-speed socket connector with 17 pairs of differential signals (one of the pairs can be multiplexed with a high-speed differential input AD sampling I/O port), 1 pair of dedicated high-speed AD sampling I/O port, and 5V, 3.3V, 1.8V power supply.
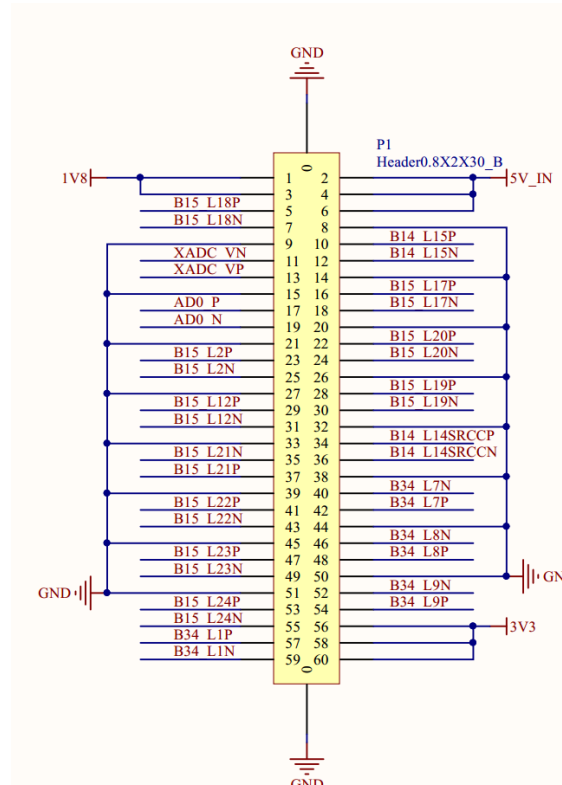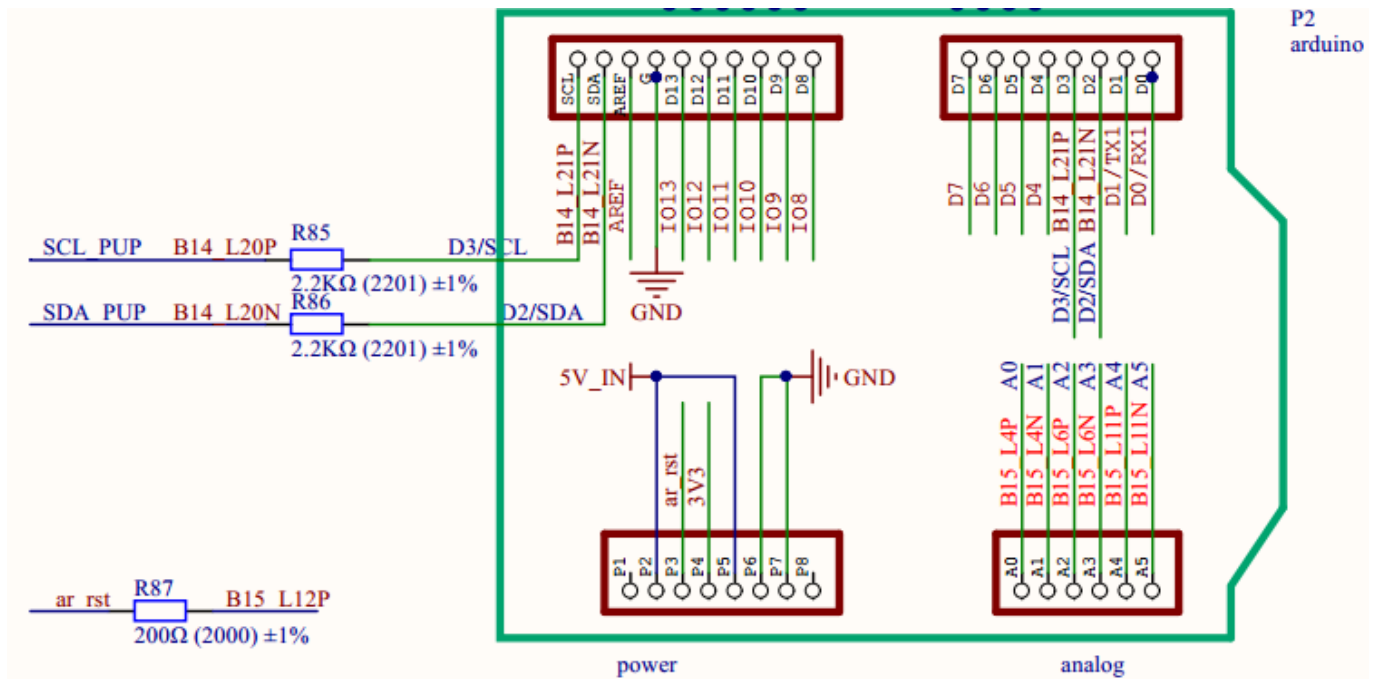
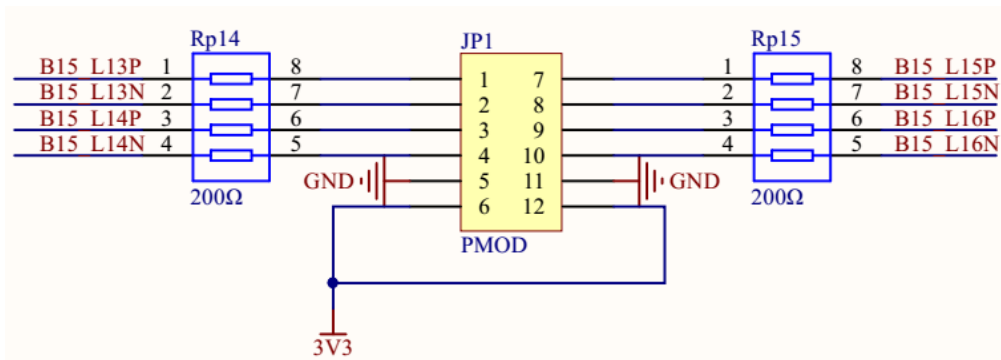| P1 Connector Pin Assignment					
P1 Pin	Signal Name	FPGA Pin	P1 Pin	Signal Name	FPGA Pin
1	1V8	-	2	5V_IN	-
3	1V8	-	4	5V_IN	-
5	B15_L18P	F15	6	5V_IN	-
7	B15_L18N	E15	8	GND	-
9	GND	-	10	B14_L15P	R12
11	XADC_VN	J7	12	B14_L15N	T1
13	XADC_VP	H8	14	GND	-
15	GND	-	16	B15_L17P	E16
17	AD0_P	C8	18	B15_L17N	D16
19	AD0_N	C9	20	GND	-
21	GND	-	22	B15_L20P	H12
23	B15_L2P	A8	24	B15_L20N	H13
25	B15_L2N	A9	26	GND	-
27	GND	-	28	B15_L19P	H11
29	B15_L12P	D13	30	B15_L19N	G12
31	B15_L12N	C13	32	GND	-
33	GND	-	34	B14_L14 RCCP	P10
35	B15_L21N	F14	36	B14_L14 RCCN	P11
37	B15_L21P	G14	38	GND	-
39	GND	-	40	B34_L7N	R1
41	B15_L22P	H16	42	B34_L7P	R2
43	B15_L22N	G16	44	GND	-
45	GND	-	46	B34_L8N	T2
47	B15_L23P	J15	48	B34_L8P	R3
49	B15_L23N	J16	50	GND	-
51	GND	-	52	B34_L9N	T3
53	B15_L24P	H14	54	B34_L9P	T4
55	B15_L24N	G15	56	3V3	-
57	B34_L1P	L4	58	3V3	-
59	B34_L1N	M4	60	3V3	-

2.2.2 P2 (Arduino) Connector

P2 is compatible with Arduino. It contains 6 pairs of single-ended input or differential input AD sampling port, a set of UART ports, a set of SPI ports, a set of IIC ports, and 10 general purpose digital I/O ports.

P2 Connector Pin Assignment					
P2 Pin	Signal Name	FPGA Pin	P2 Pin	Signal Name	FPGA Pin
P1	-	-	A0	B15_L4P	B10
P2	5V_IN	-	A1	B15_L4N	B11
P3	B15_12P	D13	A2	B15_L6P	D8
P4	3V3	-	A3	B15_L6N	D9
P5	5V_IN	-	A4	B15_L11P	C11
P6	GND	-	A5	B15_L11N	C12
P7	GND	-	D8	B14_L16N	T13
P8	-	-	D9	B14_L16P	R13
D0	B14_L19N	N6	D10	CK_SS	R7
D1	B14_L19P	M6	D11	CK_MOSI	R6
D2	B14_L21N	T8	D12	CK_MISO	T5
D3	B14_L21P	T7	D13	CK_SCK	R5
D4	B14_L11 SRCCN	P13	G	GND	-
D5	B14_L11 SRCCP	N13	AREF	B14_L6N	M12
D6	B14_L17N	R11	SDA	B14_L21N	T8
D7	B14_L17P	R10	SCL	B14_L21P	T7

2.2.3 JP1 (PMOD) Connector

JP1 is a PMOD connector with 8 general purpose digital I/O.

JP1 (PMOD) Connector Pin Assignment					
JP1 Pin	Signal Name	FPGA Pin	JP1 Pin	Signal Name	FPGA Pin
1	B15_L13P	E12	2	B15_L13N	E13
3	B15_L14P	E11	4	B15_L14N	D11
5	GND	-	6	3V3	-
7	B15_L15P	D14	8	B15_L15N	D15
9	B15_L16P	F12	10	B15_L16N	F13
11	GND	-	12	3V3	-

2.3 Power Supplies

2.3.1 Power Conversion

```
5V Power Input ──o o── ⌒ ──┬──→ TPS54331 ──→ 3.3V
              Power   Fuse   │
              Key            ├──→ TPS54331 ──→ 1.8V
                             │
                             ├──→ TPS54331 ──→ 1.5V ──┐
                             │                        ↓
                             │              TPS51200 ──→ VTT/0.75V
                             │
                             └──→ TPS54331 ──→ 1.0V
```
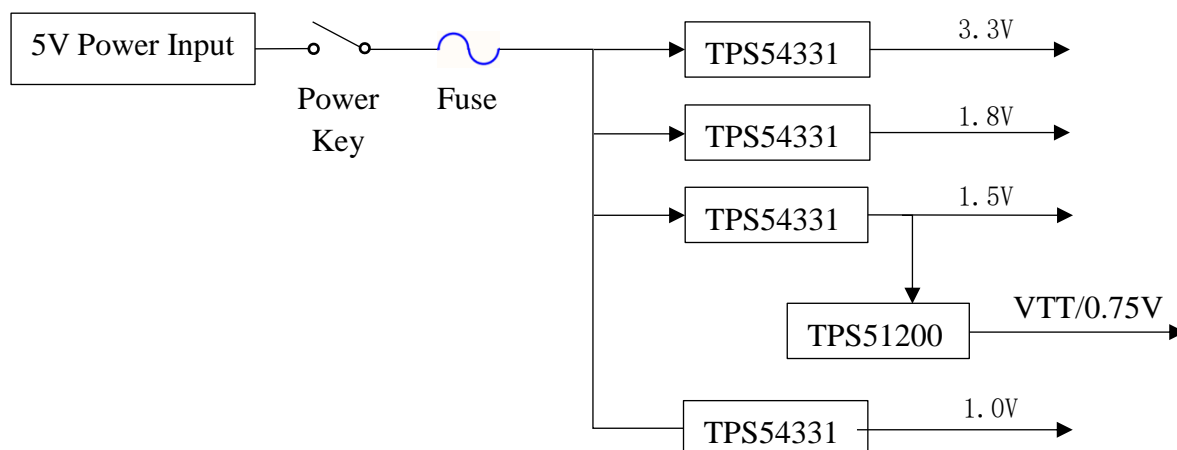
2.3.2 Function Allocation

3.3V	FPGA_Bank14/Bank15/Bank34/FLASH/Crystal Oscillator/ LED/RGB_LED/Buttons/Toggle Switches
1.8V	FPGA Auxiliary Voltage
1.5V	DDR3/FPGA_Bank35
VTT	DDR3
1.0V	FPGA Core Voltage

2.3.3 Power-on Sequence

The circuit is designed in accordance with the power-on sequence requirements of the Artix-7 FPGA (1.0V→1.8V→1.5V and 3.3V) to ensure that the chip works properly.

Development board adopts a 6-layer PCB design. A separate PWR layer and a separate GND layer are reserved so that the power supply has a good stability. Test points are reserved for each power supply on the PCB so that the user can confirm the voltage on the board.

2.4 Active Crystal Oscillator

The development board provides 50Mhz active crystal oscillator circuit as the clock source of the FPGA system. Crystal oscillator output signal SYS_CLK is connected to BANK14 global clock pin N14 (IO_L12P_T1_MRCC_14) of FPGA. This 50Mhz clock can
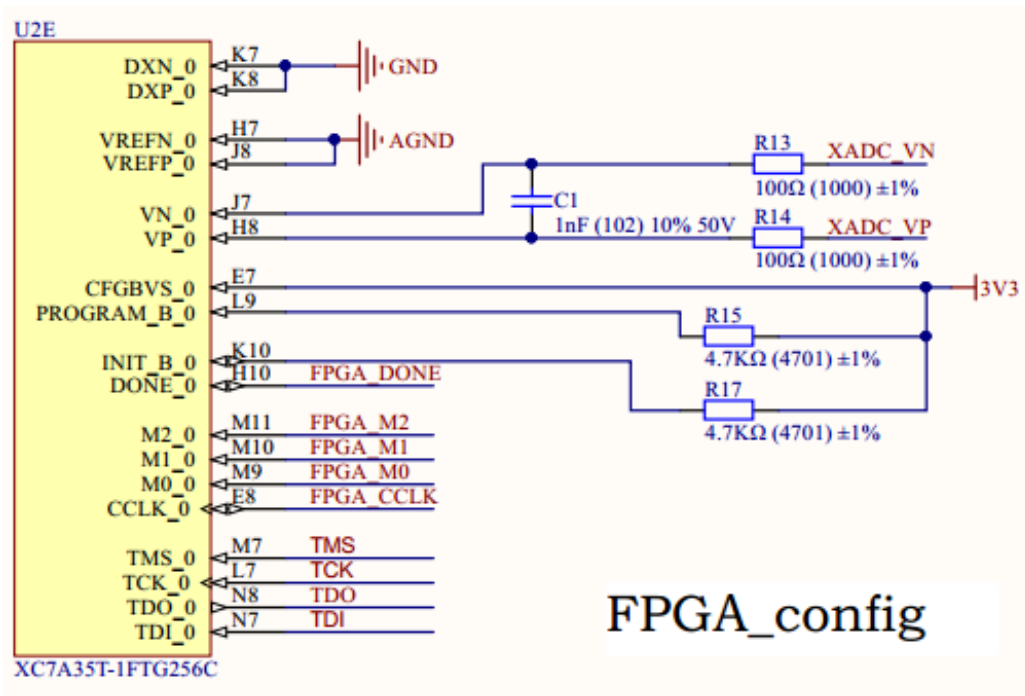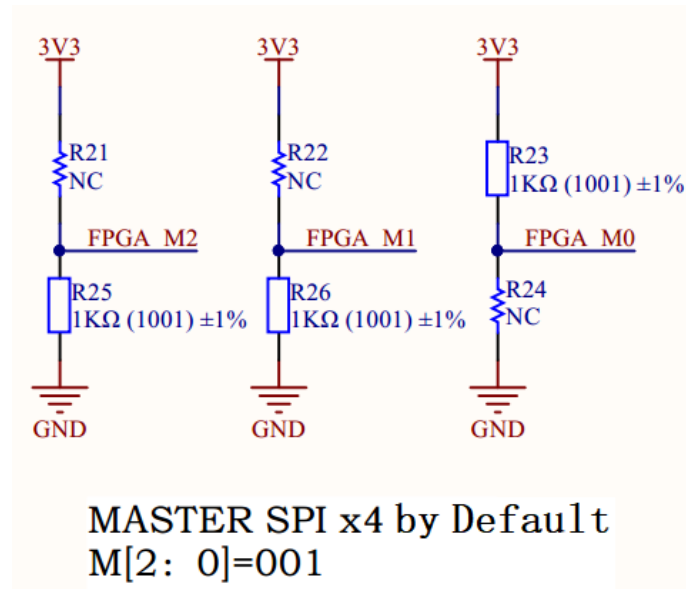
be used to drive user logic circuits in the FPGA.
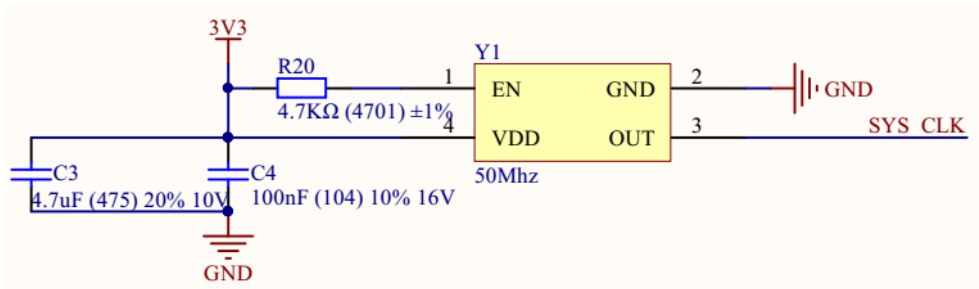
2.5 FPGA Boot

By default, the FPGA Configuration Mode Pin M[2:0] is set to 3'b001 on this board. After power-on, the FPGA will default to booting from SPI Flash.
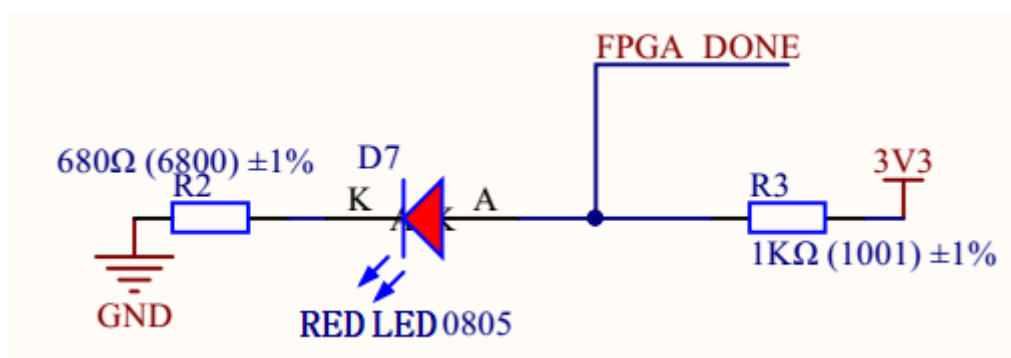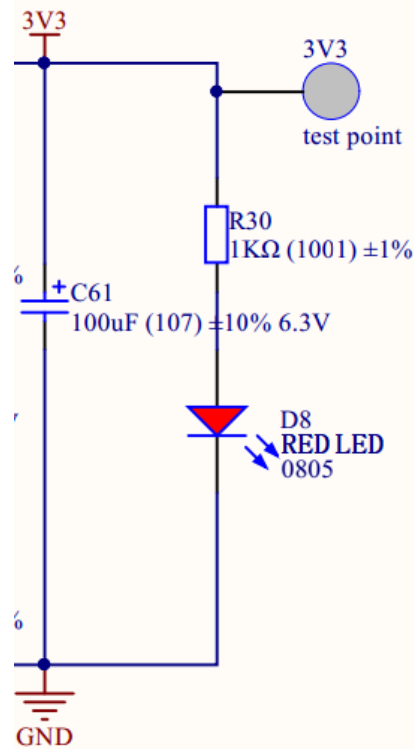

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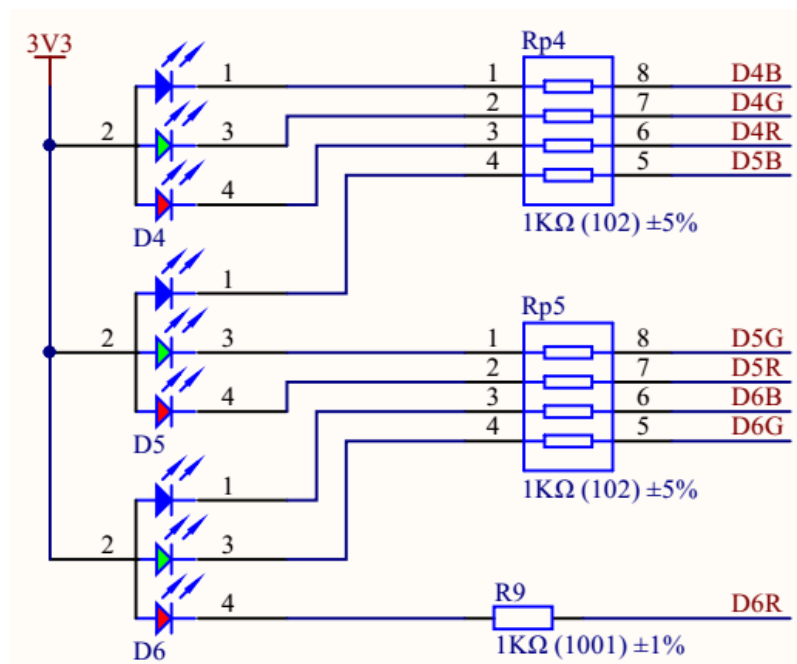MASTER SPI x4 by Default
M[2: 0]=001

2.6 LEDs and Buttons

2.6.1 LEDs

There are 9 LEDs on the development board, including 1 FPGA_DONE indicator, 1 3.3V power indicator, 3 RGB LEDs and 4 RED LEDs.
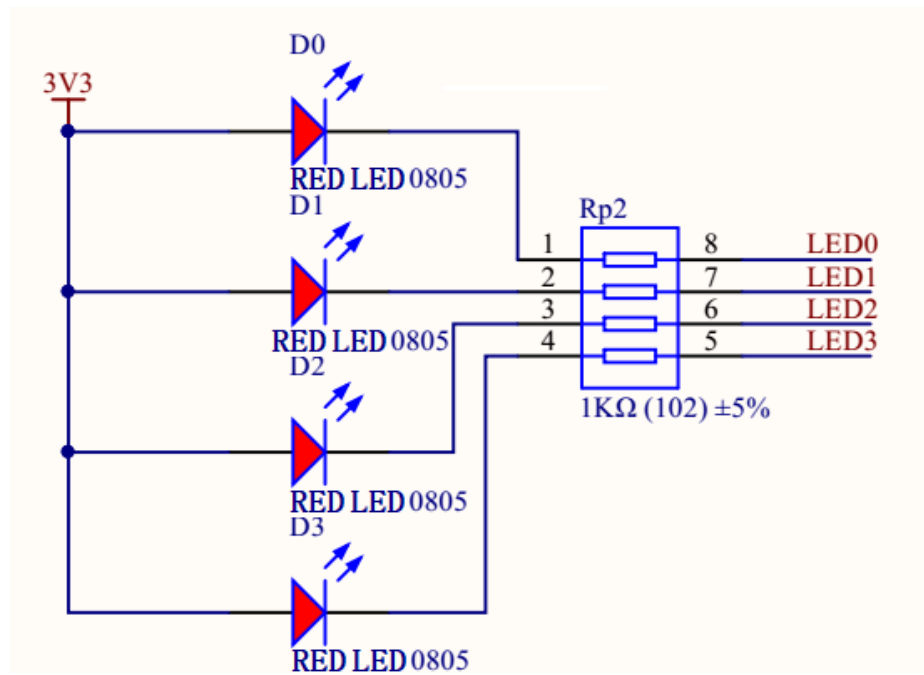

FPGA_DONE Indicator

One 3.3V Power Indicator

Three User RGB LEDs

Four User RED LEDs

9 LEDs Pin Assignment		
LED	Signal Name	FPGA Pin
D0	LED0	M16
D1	LED1	N16
D2	LED2	P15
D3	LED3	P16
D4	D4B	M2
	D4G	L5
	D4R	P5
D5	D5B	N12
	D5G	T9
	D5R	T10
D6	D6B	D10
	D6G	P6
	D6R	K12
D7	FPGA_DONE	H10
D8	Power Indicator	-

2.6.2 Buttons (Switches)

There are 9 buttons (switches) on the development board, including 1 RESET button, 4 user soft-touch buttons, and 4 user toggles switches. When the button is pressed, the corresponding I/O will be set to.
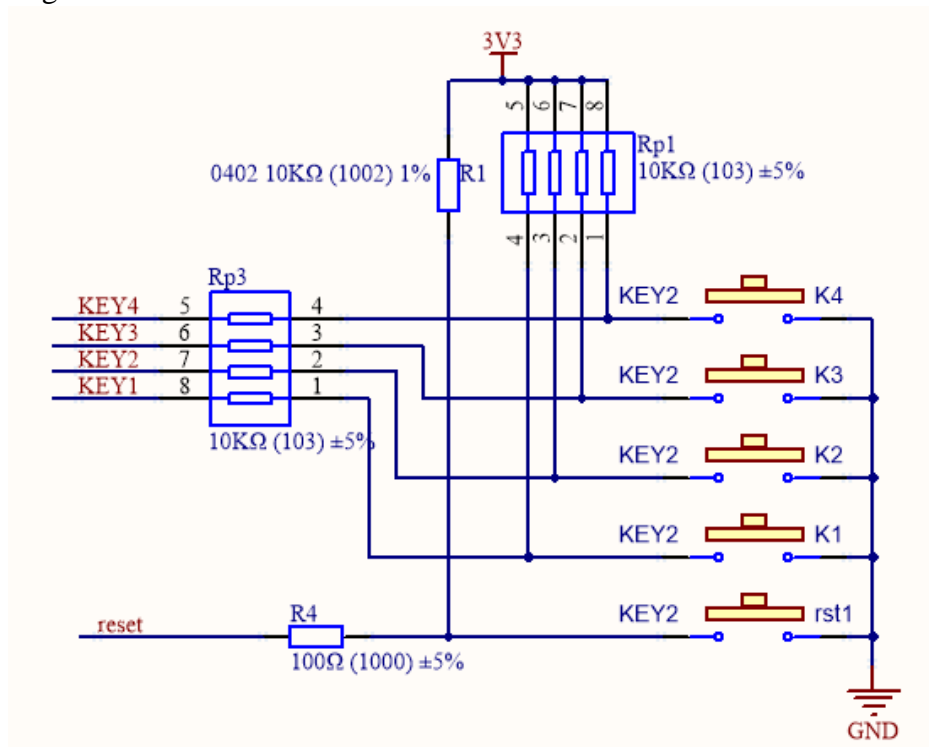
One RESET Button and Four User Soft-touch Buttons
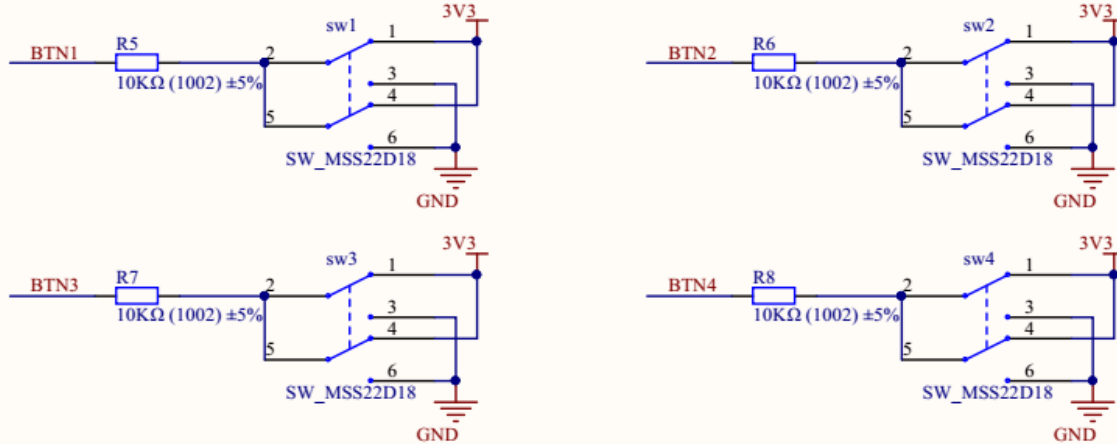
Four User Toggle Switches

9 Buttons (Switches) Pin Assignment		
KEY	Signal Name	FPGA Pin
rst1	reset	L13
K1	KEY1	M15
K2	KEY2	T14
K3	KEY3	R16
K4	KEY4	R15
sw1	BTN1	T15
sw2	BTN2	M14
sw3	BTN3	L14
sw4	BTN4	K13

2.7 XADC

The Artix-7 FPGA contains two 12-bit, 1 MSPS analog-to-digital converters, which can be configured to simultaneously sample two external analog channels. It supports single-ended and differential input analog signals, and can access up to 17 external analog input channels. The full scale input is 1V, LSB (Least Significant Bit) $= \dfrac{1V}{2^{12}} = \dfrac{1V}{4096} = 244\mu V$. JTAG can access ADC data continuously.
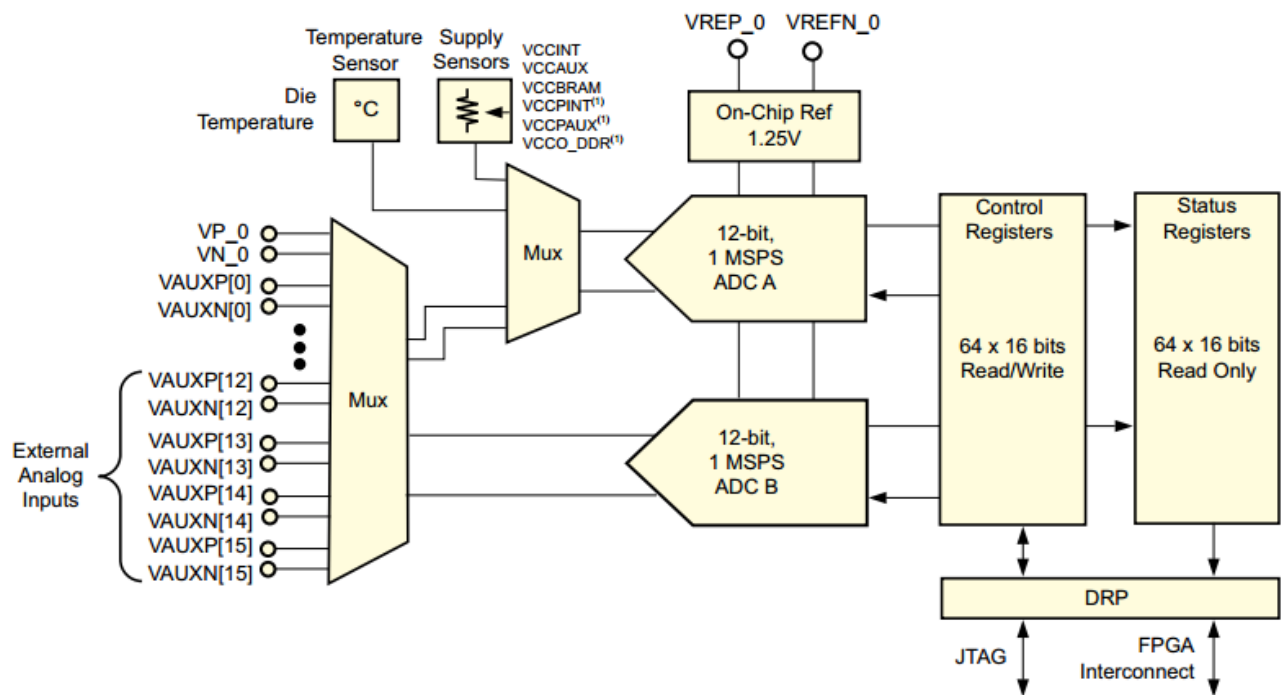
The AD sampling part of the development board uses the on-chip reference voltage of 1.25V. The on-chip reference voltage has good stability. P1 high speed connector contains two pairs of high speed differential input AD sampling ports; P2 is compatible with Arduino and contains 6 single-ended input or 6 pairs of differential input AD sampling ports.

2.8 DDR3

The development board has a high-speed DDR3 SDRAM, model number: MT41J128M16JT-093, storage capacity: 256MByte (128M*16bit), 16-bit bus. DDR3 SDRAM is connected to BANK35 of FPGA. The hardware design of DDR3 needs to take full account of signal integrity. In circuit design and PCB design, matching resistance/terminal resistance, line impedance control and line equal length control are fully considered to ensure the high-speed and stable operation of DDR3.

DDR3 SDRAM Pin Assignment			
Signal Name	FPGA Pin	Signal Name	FPGA Pin
DDR_A0	C2	DDR_D0	F5
DDR_A1	C6	DDR_D1	G4
DDR_A2	B1	DDR_D2	G2
DDR_A3	C3	DDR_D3	H5
DDR_A4	C7	DDR_D4	E5
DDR_A5	B2	DDR_D5	G1
DDR_A6	D6	DDR_D6	F4
DDR_A7	B4	DDR_D7	F3
DDR_A8	A7	DDR_D8	H1
DDR_A9	A2	DDR_D9	J4
DDR_A10	B5	DDR_D10	H2
DDR_A11	B7	DDR_D11	J1
DDR_A12	D5	DDR_D12	K3
DDR_A13	A3	DDR_D13	J5
DDR_BA0	D1	DDR_D14	L3
DDR_BA1	B6	DDR_D15	L2
DDR_BA2	E2	DDR_DQS0_P	F2
DDR_CLK_P	A5	DDR_DQS0_N	E1
DDR_CLK_N	A4	DDR_DQS1_P	J3
DDR_CKE	C1	DDR_DQS1_N	H3
DDR_WE	D3	DDR_DQM0	G5
DDR_CAS	D4	DDR_DQM1	K1
DDR_RAS	H4	DDR_RESET	C4
DDR_ODT	E3		

2.9 SPI FLASH

The development board uses two 8MB (64Mbit) SPI FLASH chips, model 25Q064A, using 3.3V CMOS voltage. Due to its non-volatile characteristic, SPI FLASH can store the boot image of the FPGA systems. The boot image mainly includes the bit files of FPGA, applications, and user data files.
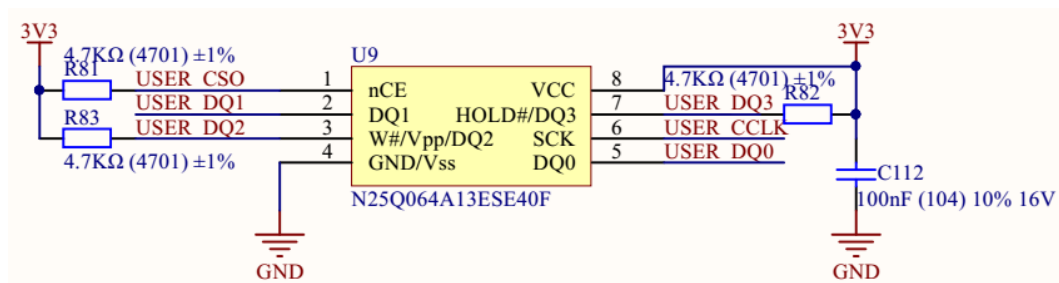
2.9.1 FLASH

In Master SPI mode, the FPGA will read the Bit Stream from this FLASH by default.
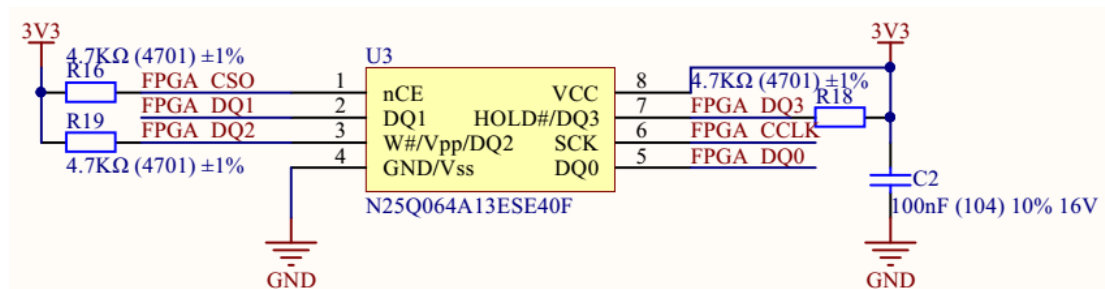
FLASH Pin Assignment					
FLASH Pin	Signal Name	FPGA Pin	FLASH Pin	Signal Name	FPGA Pin
1	FPGA_CSO	L12	2	FPGA_DQ1	J14
3	FPGA_DQ2	K15	4	GND	-
5	FPGA_DQ0	J13	6	FPGA_CCLK	E8
7	FPGA_DQ3	K16	8	3V3	-

2.9.2 USER FLASH

USER FLASH can be used to store user data and code.

USER FLASH Pin Assignment					
USER FLASH Pin	Signal Name	FPGA Pin	USER FLASH Pin	Signal Name	FPGA Pin
1	USER_CSO	M5	2	USER_DQ1	P1
3	USER_DQ2	P4	4	GND	-
5	USER_DQ0	N1	6	USER_CCLK	N4
7	USER_DQ3	P3	8	3V3	-

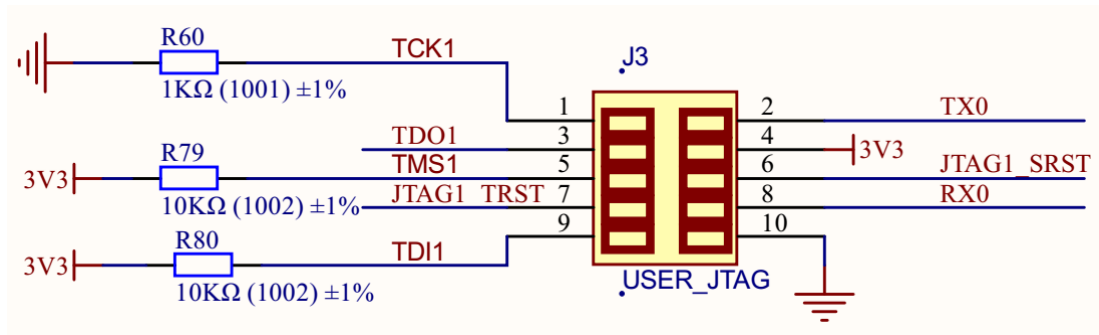# 2.10 JTAG Connectors

2.10.1 JTAG

Dedicated to download programs to FPGA or to FLASH. Hot-plug is not supported. Please power off when plugging or unplugging the JTAG cable.
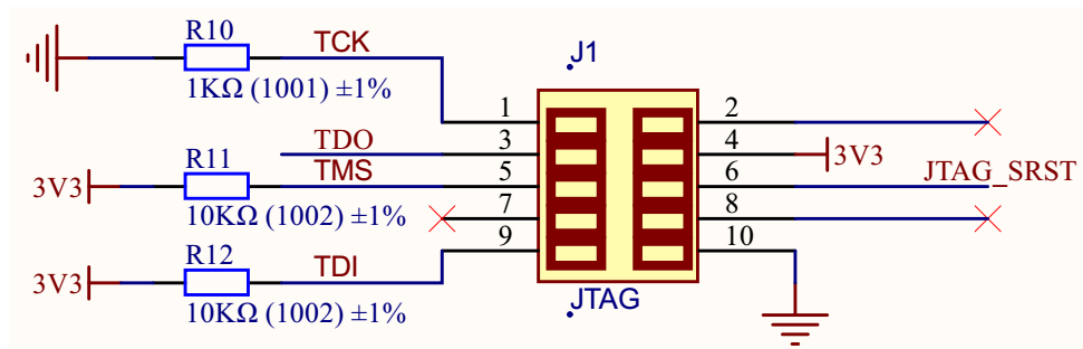
JTAG Connector Pin Assignment					
JTAG Pin	Signal Name	FPGA Pin	JTAG Pin	Signal Name	FPGA Pin
1	TCK	L7	2	-	-
3	TDO	N8	4	3V3	-
5	TMS	M7	6	JTAG_SRST	P14
7	-	-	8	-	-
9	TDI	N7	10	GND	-

2.10.2 USER JTAG

Can be used for debugging.

| USER JTAG Connector Pin Assignment					
USER JTAG Pin	Signal Name	FPGA Pin	USER JTAG Pin	Signal Name	FPGA Pin
1	TCK1	N11	2	TX0	P9
3	TDO1	M1	4	3V3	-
5	TMS1	N3	6	JTAG1_SRST	M4
7	JTAG1_TRST	L4	8	RX0	N9
9	TDI1	N2	10	GND	-

2.11 Connection between FPGA and Development Board

Hummingbird E203 Processor Core is pre-installed.

Hummingbird E203 Processor Core	Development Board Connector
QSPI	USER FLASH
UART0	USER JTAG
UART1	Arduino_D0/D1
CK_IO[0:19]	Arduino_D4…D13 Arduino_A0…A5 PMOD_P1…P4
SPI2	Arduino_D10…D13
JTAG	USER JTAG

3 Mechanical Dimensions and Weight

3.1 Mechanical Dimensions (mm)
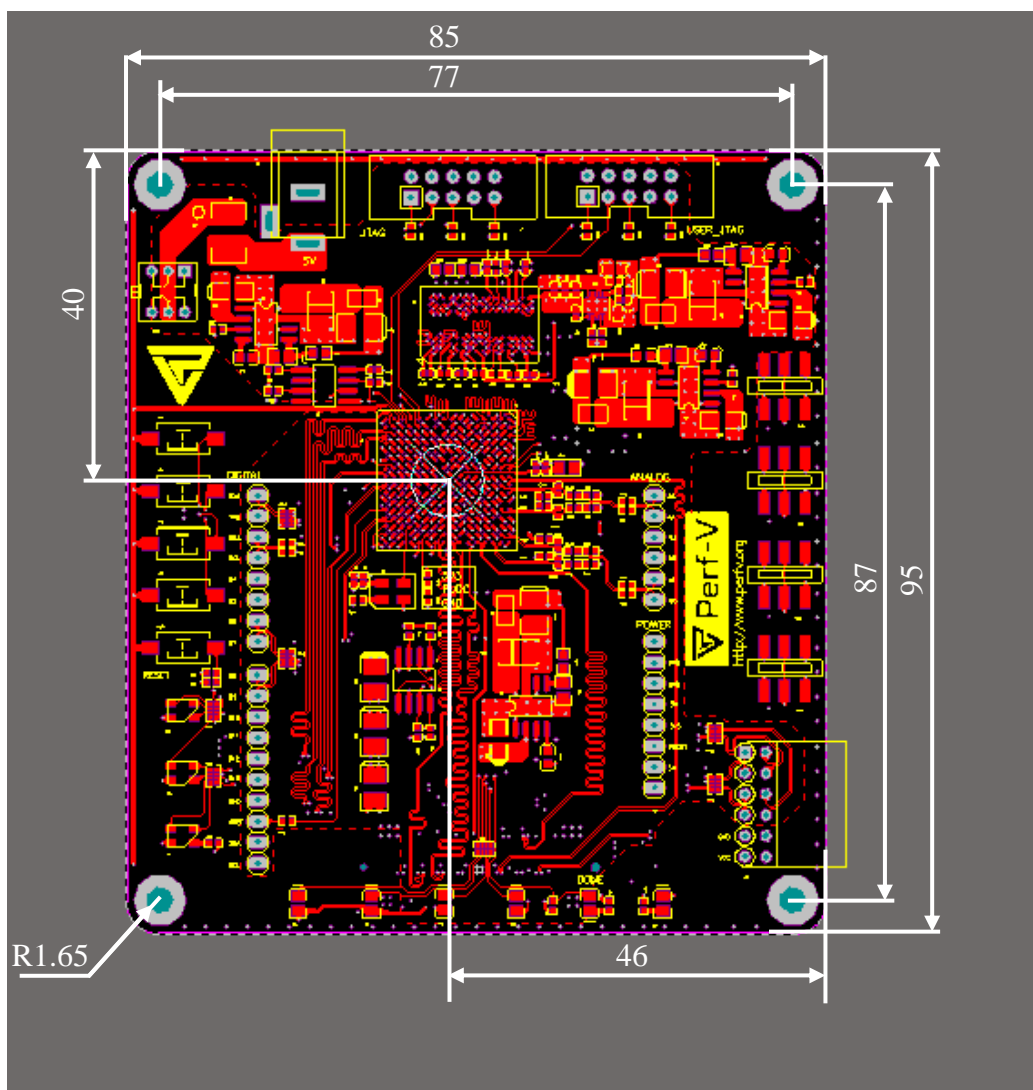
3.2 Weight (g)

Development Board (Without Copper Column)	43.4g
Development Board (Including Copper Column)	52.8g

4 Revision History

Date	Version	Revision
2018.04.01	1.0	Initial release