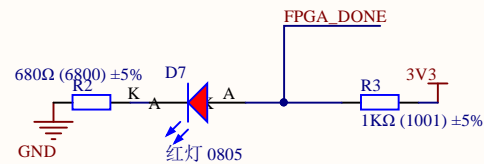
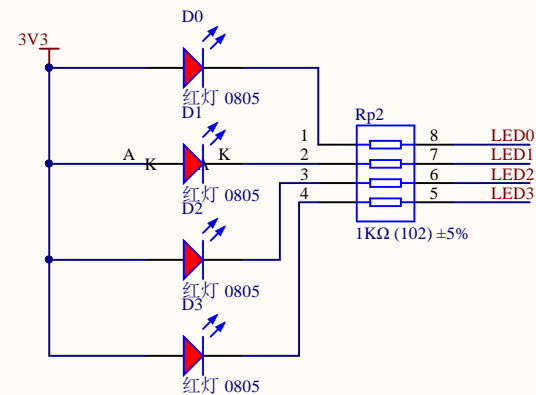


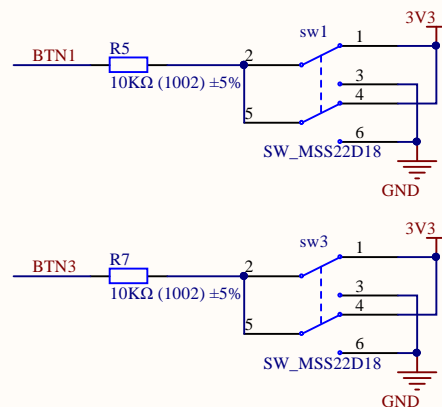
KEY (reset)



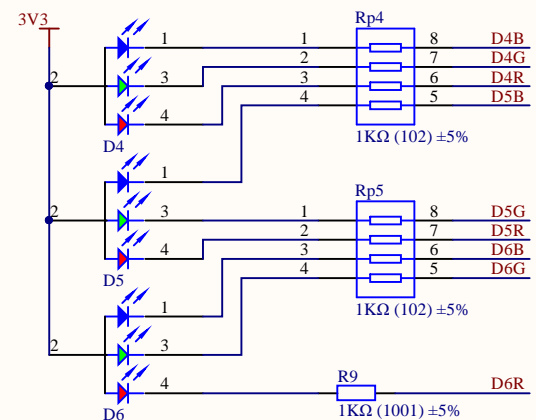
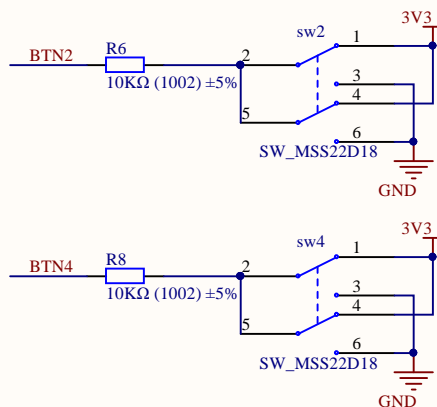
FPGA DONE LED



USER LED

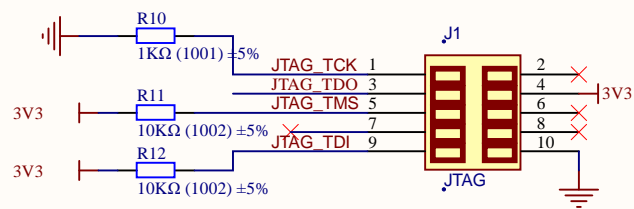


SWITCH

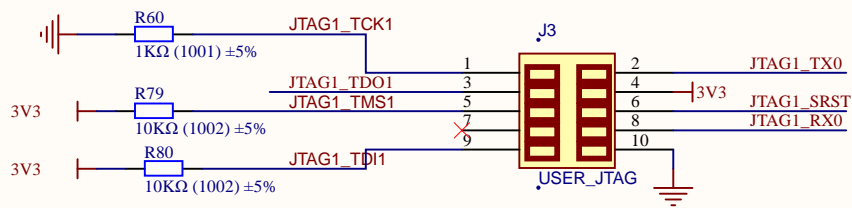
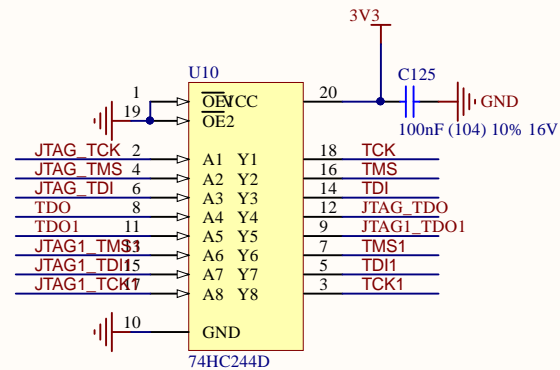


RGB LED

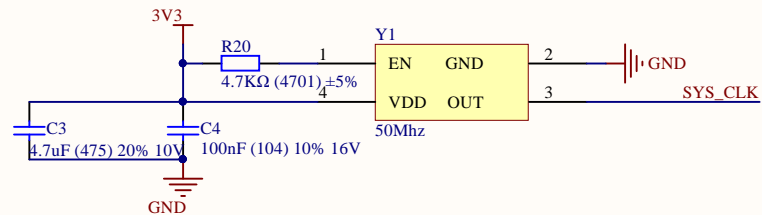
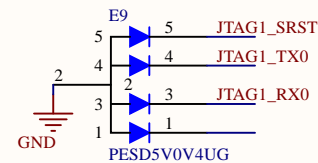
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A4		
Date:	2018/5/28	Sheet of
File:	F:\work\1_LED_KEY.SchDoc	Drawn By:



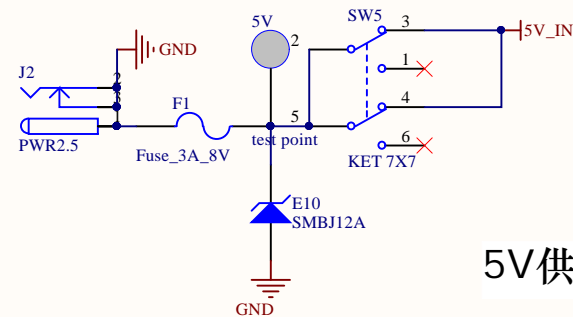
JTAG



USER JTAG

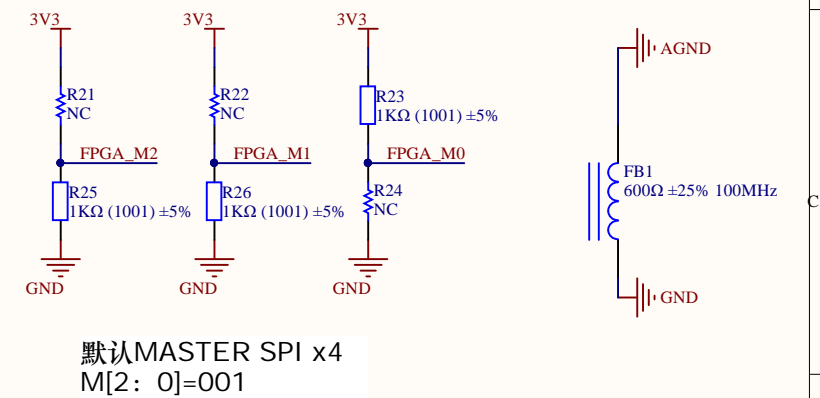
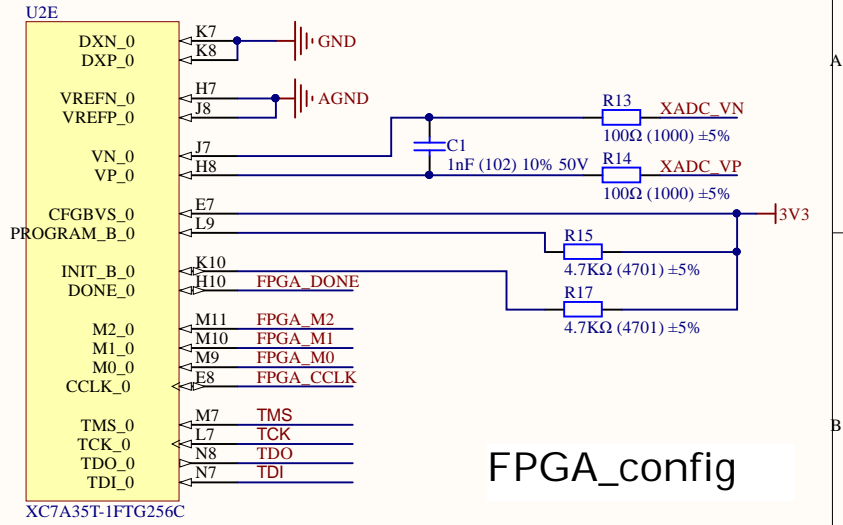
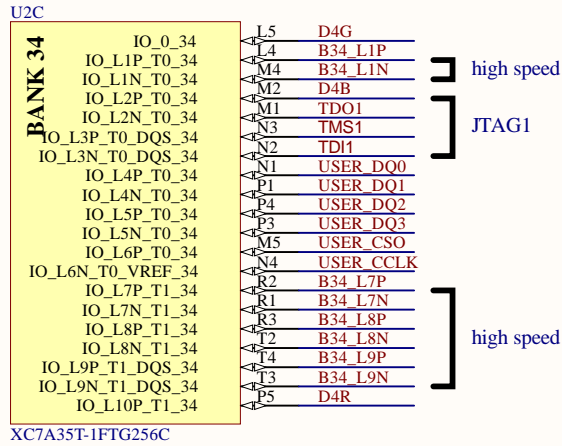
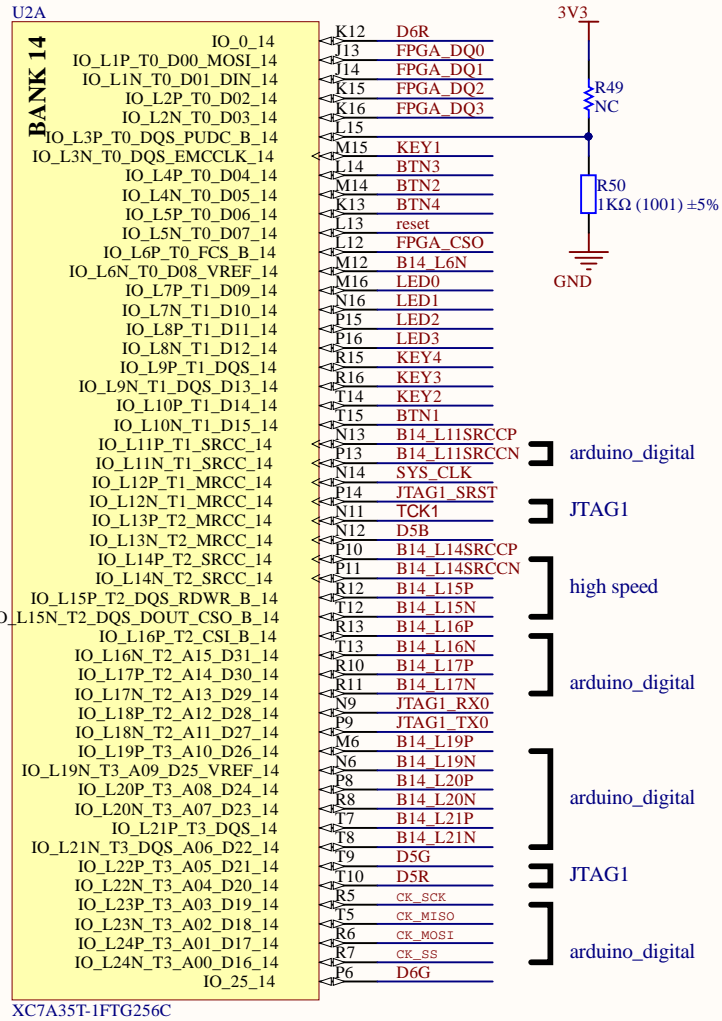


有源晶振
50M



5V供电

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Size	Number	Revision
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Date:	2018/5/28	Sheet of
File:	F:\work\...\2_XTAL_JTAG_FLASH (2).S	Drawn By:



Title		
Size	Number	Revision
A4		
Date:	2018/5/28	Sheet of
File:	F:\work\...\3_BANK1434conf.SchDoc	Drawn By:

U2B

BANK 15

IO_0_15
IO_L1P_T0_AD0P_15
IO_L1N_T0_AD0N_15
IO_L2P_T0_AD8P_15
IO_L2N_T0_AD8N_15
IO_L3P_T0_DQS_AD1P_15
IO_L3N_T0_DQS_AD1N_15
IO_L4P_T0_15
IO_L4N_T0_15
IO_L5P_T0_AD9P_15
IO_L5N_T0_AD9N_15
IO_L6P_T0_15
IO_L6N_T0_VREF_15
IO_L7P_T1_AD2P_15
IO_L7N_T1_AD2N_15
IO_L8P_T1_AD10P_15
IO_L8N_T1_AD10N_15
IO_L9P_T1_DQS_AD3P_15
IO_L9N_T1_DQS_AD3N_15
IO_L10P_T1_AD11P_15
IO_L10N_T1_AD11N_15
IO_L11P_T1_SRCC_15
IO_L11N_T1_SRCC_15
IO_L12P_T1_MRCC_15
IO_L12N_T1_MRCC_15
IO_L13P_T2_MRCC_15
IO_L13N_T2_MRCC_15
IO_L14P_T2_SRCC_15
IO_L14N_T2_SRCC_15
IO_L15P_T2_DQS_15
IO_L15N_T2_DQS_ADV_B_15
IO_L16P_T2_A28_15
IO_L16N_T2_A27_15
IO_L17P_T2_A26_15
IO_L17N_T2_A25_15
IO_L18P_T2_A24_15
IO_L18N_T2_A23_15
IO_L19P_T3_A22_15
IO_L19N_T3_A21_VREF_15
IO_L20P_T3_A20_15
IO_L20N_T3_A19_15
IO_L21P_T3_DQS_15
IO_L21N_T3_DQS_A18_15
IO_L22P_T3_A17_15
IO_L22N_T3_A16_15
IO_L23P_T3_FOE_B_15
IO_L23N_T3_FWE_B_15
IO_L24P_T3_RS1_15
IO_L24N_T3_RS0_15
IO_25_15

XC7A35T-IFTG256C

3V3

D10 D6B
C8
C9
A8 B15 L2P
A9 B15 L2N
B9 B15 L3P
A10 B15 L3N
B10 B15 L4P
B11 B15 L4N
B12 B15 L5P
A12 B15 L5N
D8 B15 L6P
D9 B15 L6N
A13 B15 L7P
A14 B15 L7N
C14 B15 L8P
B14 B15 L8N
B15 B15 L9P
A15 B15 L9N
C16 B15 L10P
B16 B15 L10N
C11 B15 L11P
C12 B15 L11N
D13 B15 L12P
C13 B15 L12N
E12 B15 L13P
E13 B15 L13N
E11 B15 L14P
D11 B15 L14N
D14 B15 L15P
D15 B15 L15N
F12 B15 L16P
F13 B15 L16N
E16 B15 L17P
D16 B15 L17N
F15 B15 L18P
E15 B15 L18N
H11 B15 L19P
G12 B15 L19N
H12 B15 L20P
H13 B15 L20N
G14 B15 L21P
F14 B15 L21N
H16 B15 L22P
G16 B15 L22N
I15 B15 L23P
I16 B15 L23N
H14 B15 L24P
G15 B15 L24N
G11 B15_25

arduino_analog

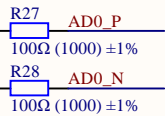
high speed

PMOD1

high speed

arduino_digital

2



high speed

U2D

BANK 35

IO_0_35
IO_L1P_T0_AD4P_35
IO_L1N_T0_AD4N_35
IO_L2P_T0_AD12P_35
IO_L2N_T0_AD12N_35
IO_L3P_T0_DQS_AD5P_35
IO_L3N_T0_DQS_AD5N_35
IO_L4P_T0_35
IO_L4N_T0_35
IO_L5P_T0_AD13P_35
IO_L5N_T0_AD13N_35
IO_L6P_T0_35
IO_L6N_T0_VREF_35
IO_L7P_T1_AD6P_35
IO_L7N_T1_AD6N_35
IO_L8P_T1_AD14P_35
IO_L8N_T1_AD14N_35
IO_L9P_T1_DQS_AD7P_35
IO_L9N_T1_DQS_AD7N_35
IO_L10P_T1_AD15P_35
IO_L10N_T1_AD15N_35
IO_L11P_T1_SRCC_35
IO_L11N_T1_SRCC_35
IO_L12P_T1_MRCC_35
IO_L12N_T1_MRCC_35
IO_L13P_T2_MRCC_35
IO_L13N_T2_MRCC_35
IO_L14P_T2_SRCC_35
IO_L14N_T2_SRCC_35
IO_L15P_T2_DQS_35
IO_L15N_T2_DQS_35
IO_L16P_T2_35
IO_L16N_T2_35
IO_L17P_T2_35
IO_L17N_T2_35
IO_L18P_T2_35
IO_L18N_T2_35
IO_L19P_T3_35
IO_L19N_T3_VREF_35
IO_L20P_T3_35
IO_L20N_T3_35
IO_L21P_T3_DQS_35
IO_L21N_T3_DQS_35
IO_L22P_T3_35
IO_L22N_T3_35
IO_L23P_T3_35
IO_L23N_T3_35
IO_L24P_T3_35
IO_L24N_T3_35
IO_25_35

XC7A35T-IFTG256C

1V5

E6
B7 DDR A11
A7 DDR A8
B6 DDR BA1
B5 DDR A10
A5 DDR CLK_P
A4 DDR CLK_N
B4 DDR A7
A3 DDR A13
C7 DDR A4
C6 DDR A1
D6 DDR A6
D5 DDR A12
C3 DDR A3
C2 DDR A0
B2 DDR A5
A2 DDR A9
C1 DDR CKE
B1 DDR A2
E2 DDR BA2
D1 DDR BA0
E3 DDR ODT
D3 DDR WE
D4 DDR CAS
C4 DDR RAS
F5 DDR D0
E5 DDR D4
F4 DDR D6
F3 DDR D7
E2 DDR DQS0_P
E1 DDR DQS0_N
G5 DDR DQM0
G4 DDR D1
G2 DDR D2
G1 DDR D5
H5 DDR D3
H4 DDR RESET
J5 DDR D13
J4 DDR D9
H2 DDR D10
H1 DDR D8
J3 DDR DQS1_P
H3 DDR DQS1_N
K1 DDR DQM1
J1 DDR D11
I3 DDR D14
I2 DDR D15
K3 DDR D12
K2
K5

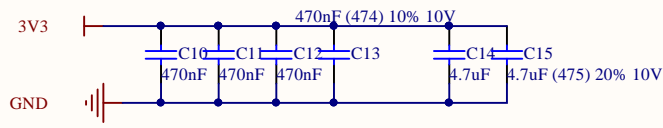
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Date:	2018/5/28	Sheet of
File:	F:\work\...\3_BANK1535.SchDoc	Drawn By:

1

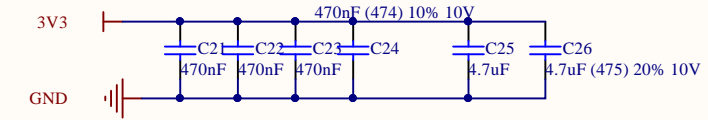
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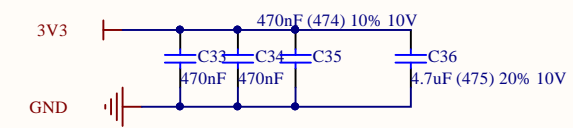
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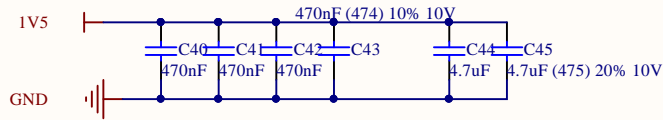
for VCCO_14



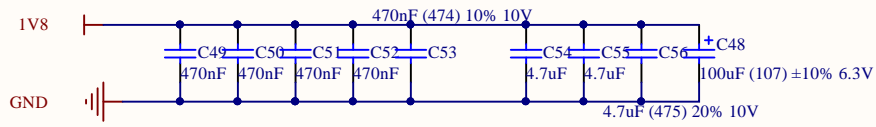
for VCCO_15



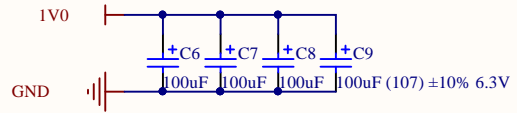
for VCCO_34



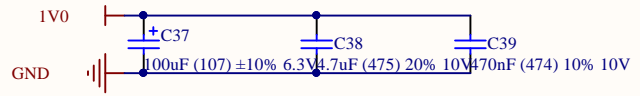
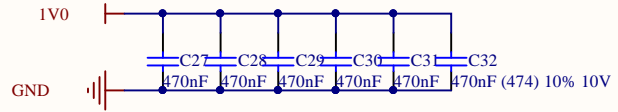
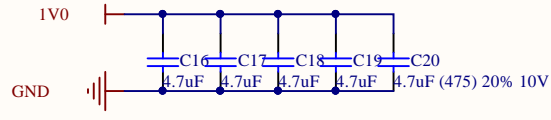
for VCCO_35



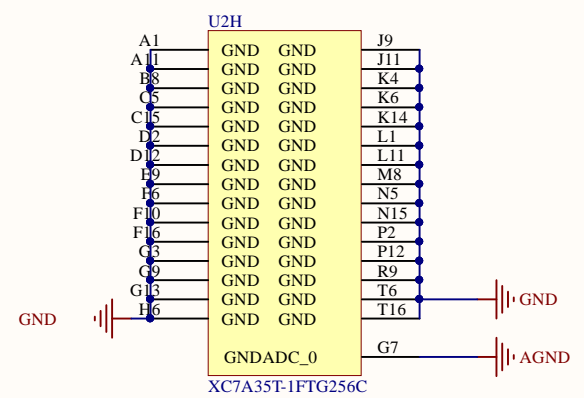
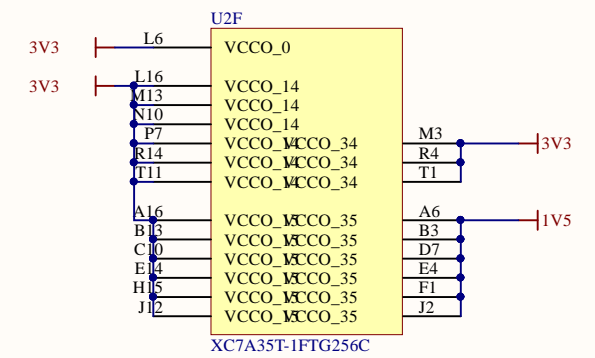
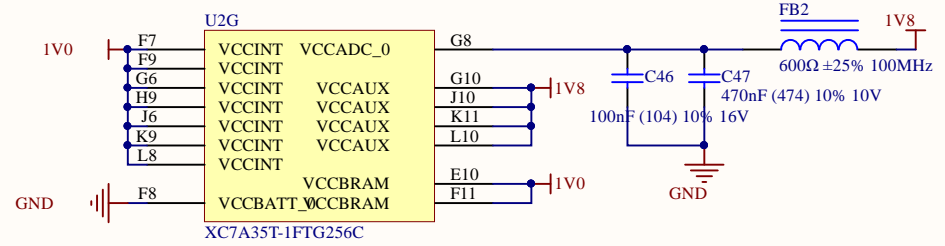
for VCCAUX&VCCBATT_0



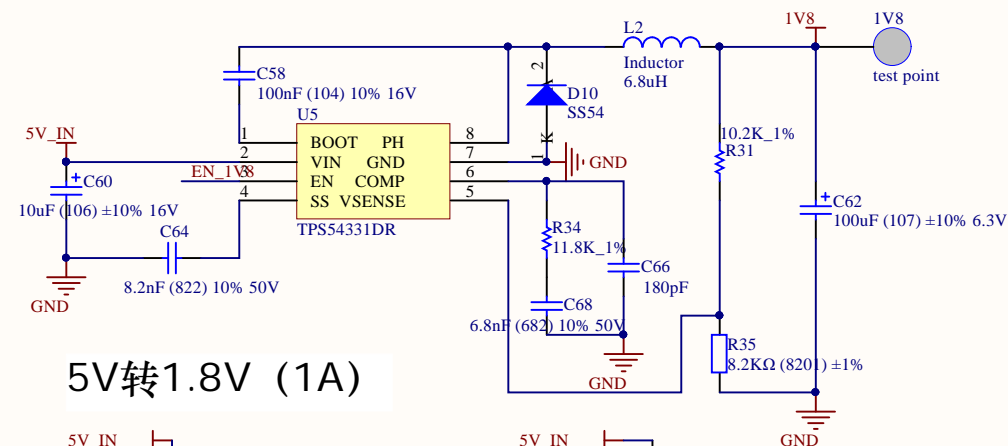
for VCCINT



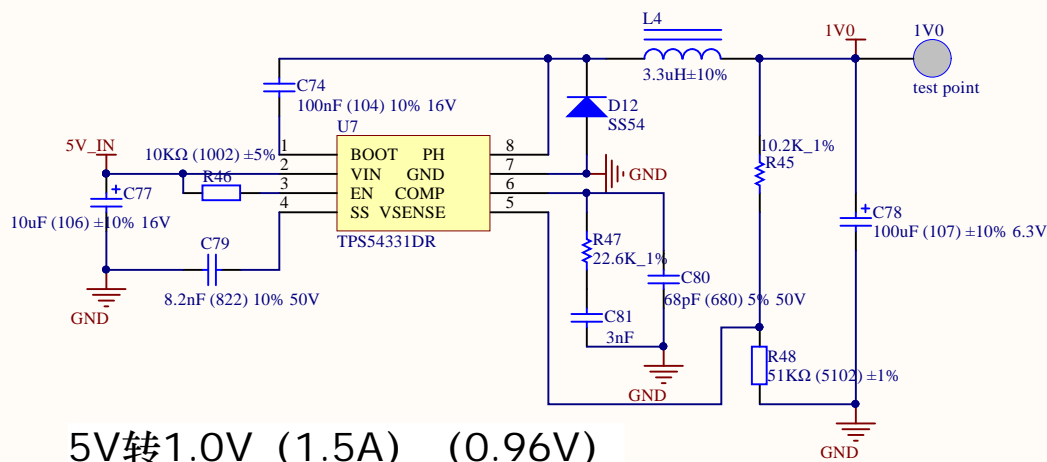
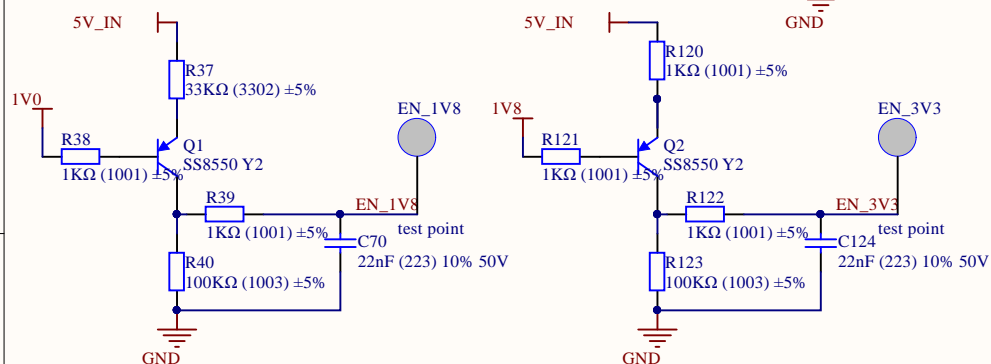
for VCCBRAM



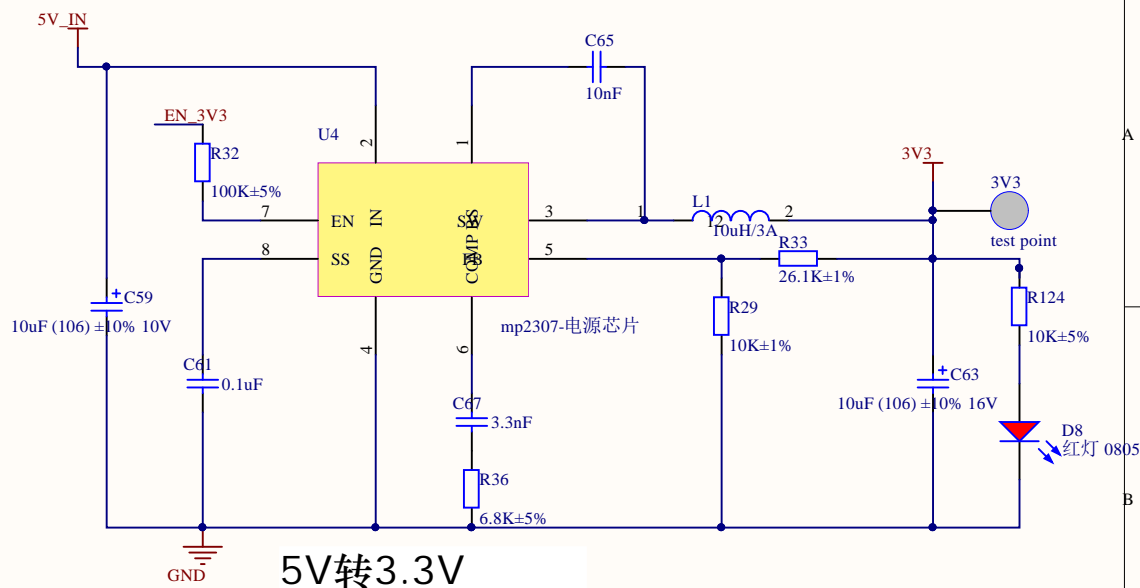
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Size	Number	Revision
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Date:	2018/5/28	Sheet of
File:	F:\work\...\4_FPGA_PWR.SchDoc	Drawn By:



5V转1.8V (1A)

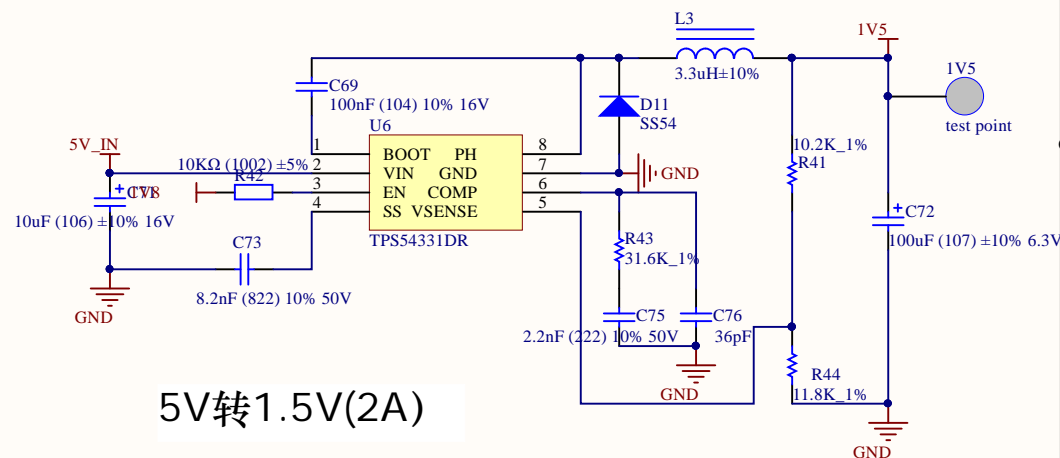


5V转1.0V (1.5A) (0.96V)



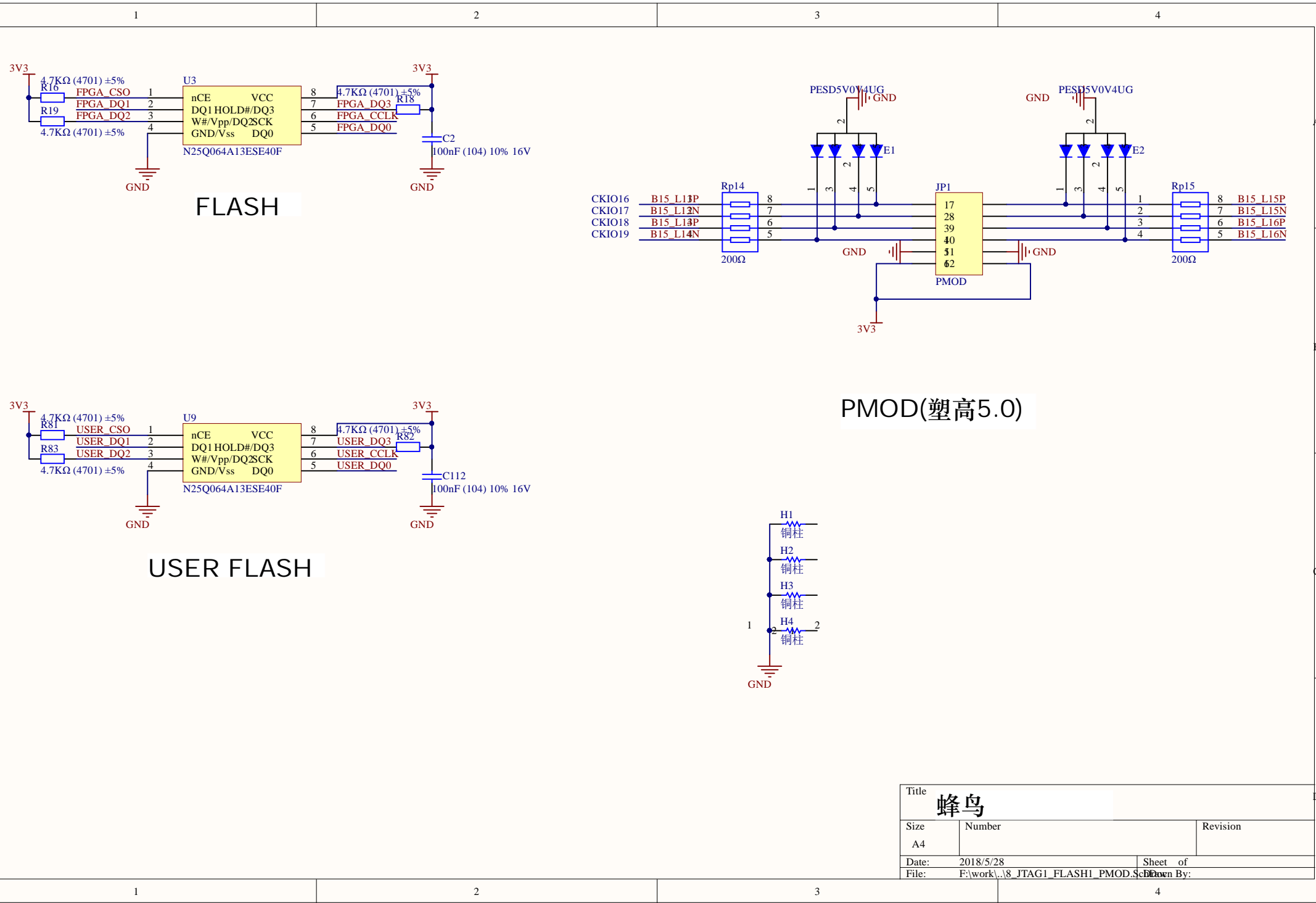
5V转3.3V

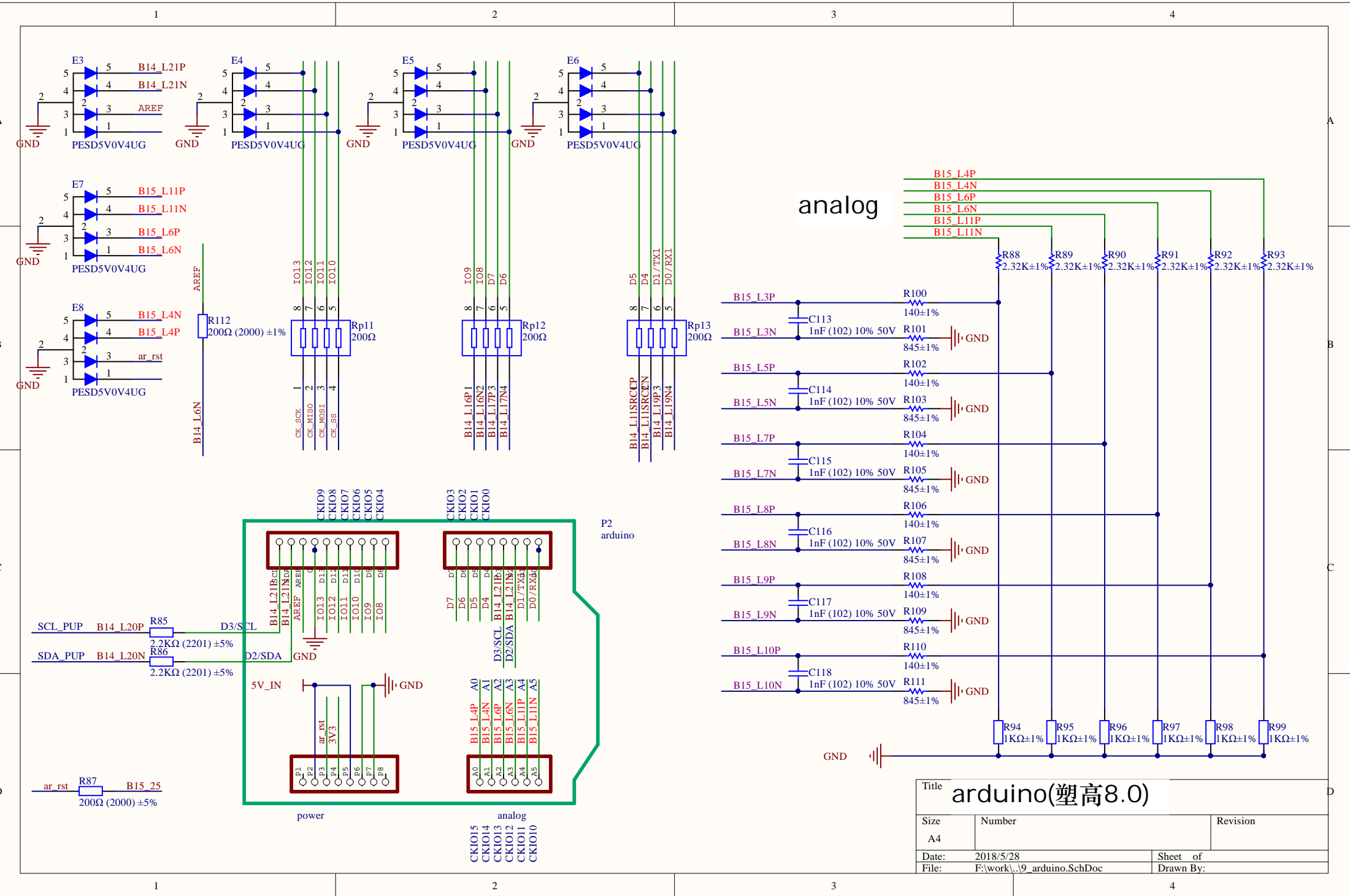
上电顺序 5V>1.0V>1.8V> (1.5V/3.3V)



5V转1.5V(2A)

Title		
Size A4	Number	Revision
Date:	2018/5/28	Sheet of
File:	F:\work\A6 POWER1 SchDoc	Drawn By:





Title			arduino(塑高8.0)	
Size	Number		Revision	
A4				
Date:	2018/5/28		Sheet of	
File:	F:\work\...\9_arduino.SchDoc		Drawn By:	