ANALOG COMPUTING

Vaire A British Startup Validates Reversible Computing

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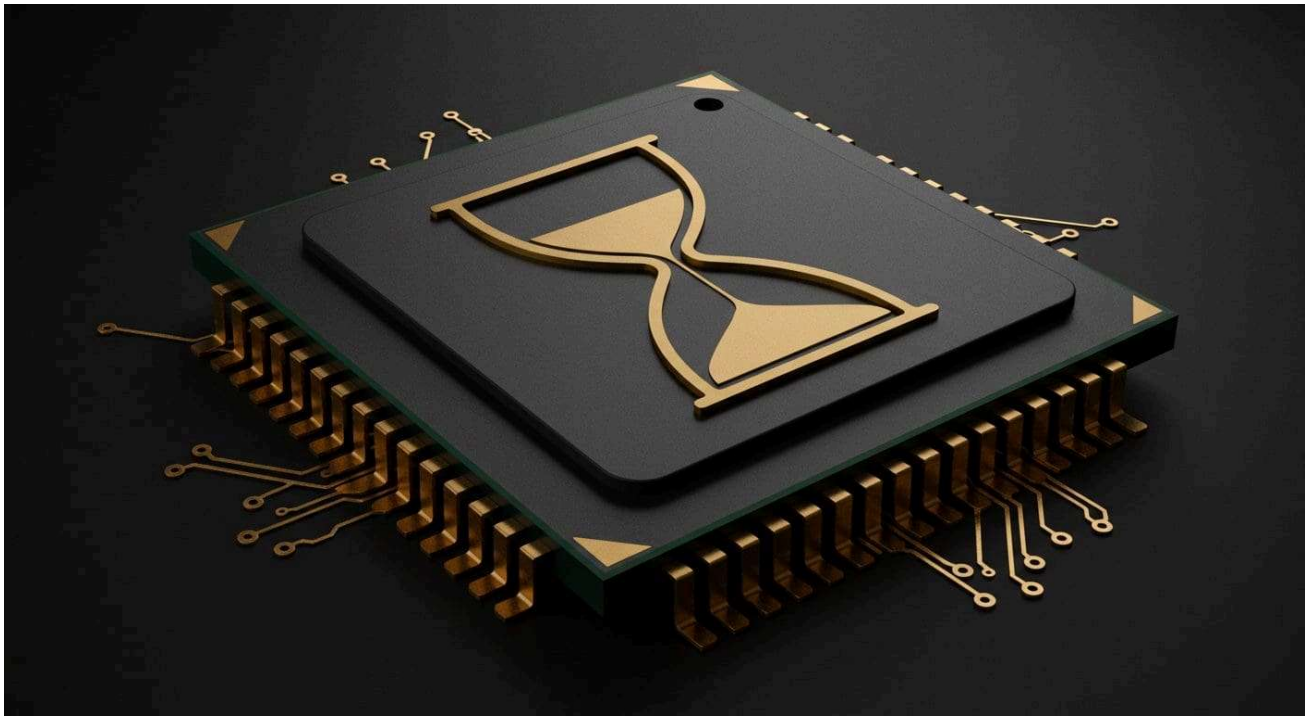

Hannah Earley from Vaire, the British reversible-computing startup, demonstrated an adiabatic reversible computing system with net energy recovery using the Ice River test chip fabricated in 22 nm CMOS. The chip achieved an energy-recovery factor of 1.77 for a capacitor array and 1.41 for an adder circuit, surpassing the proof-of-concept threshold of 1.0 and validating the resonator design that recycles energy between clock cycles. With a data frequency of 500 MHz and a target of 1 GHz for future production, this

milestone—after four years of focused development—opens a new scaling law for low-power computation.

Vaire Demonstrates First Energy Recovering Reversible Computing Chip

Vaire, a London-based reversible computing start-up, announced on 9 March 2025 that its first test chip, codenamed Ice River, has achieved net energy recovery in a fully CMOS-based adiabatic system. The 22 nm process chip demonstrates that a resonator-driven capacitor array can reclaim 1.77 times the energy that a conventional square-wave circuit would dissipate, while an on-chip adder recovers 1.41 times. These figures, reported by Vaire Chief Technology Officer Hannah Earley, represent the first publicly documented proof that reversible logic can be coupled with practical energy-recovery circuitry in silicon.

Ice River incorporates several specialised components that together realise adiabatic switching. A resonator delivers a trapezoidal, linear-ramp voltage that is dynamically synchronised with the high and low rails, ensuring that no potential difference exists during transition and that energy is not lost as heat. The chip also contains a custom driver that replenishes recovered energy, a passive distribution network that routes the trapezoidal signals without active clock-tree elements, and reversible logic blocks—including a shift register and an adder—implemented with CMOS transistors. The data path operates at 500 MHz, with the design team targeting 1 GHz in subsequent production runs, a speed that will test the limits of clock-distribution fidelity in a reversible architecture.

The resonator design, patented by former Sandia National Laboratories scientist Mike Frank in 2023, is central to the energy-recovery mechanism. By maintaining thermal equilibrium during transistor switching, the system can recover the (½CV^2) energy stored in gate capacitances and reuse it in the next cycle. The passive distribution network, a departure from conventional active clock trees, mitigates waveform distortion while preserving the reversibility of the logic stages. Together, these innovations allow Ice River to recover more energy than the theoretical 2× figure predicted by simulation, a shortfall attributed to the practical challenges of wafer-level fabrication and signal integrity.

The demonstration marks a milestone for reversible computing, a field that has long been considered a theoretical curiosity. As Vaire CEO Rodolfo Rosini explained, the chip shows that CMOS technology can approach its own terminal limit while still achieving significant energy savings, a development that could counteract the slowdown of Moore's Law and meet the escalating energy demands of AI workloads. The company now plans to refine performance, extend the resonator design to higher frequencies, and engage early-adopter partners to licence its intellectual property for specialised ASICs.

Looking ahead, Vaire's roadmap includes a second-generation chip that will push data frequencies toward 1 GHz, improve energy-recovery ratios, and broaden the range of reversible logic blocks. The firm also intends to offer its resonator IP to external designers, enabling a wider ecosystem of low-power, high-performance chips. By demonstrating that reversible computing can be realised in a commercial CMOS process, Vaire has opened a new scaling law that could reshape the energy profile of future processors.

Ice River Achieves 177 Fold Energy Recovery in 22nm CMOS

On 9 March 2025, Vaire—a London-based reversible-computing start-up—announced the launch of its prototype chip, codenamed Ice River, fabricated in a 22 nm CMOS process. The device, the first of its kind to demonstrate net energy recovery in a commercial CMOS node, achieved a 1.77-fold increase in energy reclamation compared with a conventional square-wave driven circuit. Chief technology officer Hannah Earley highlighted that the demonstration validates Vaire's core resonator concept and confirms the feasibility of reversible computing within mainstream semiconductor technology.

The evaluation employed a capacitive bank and an adder logic block as test structures, with the resonator supplying a trapezoidal voltage to drive the gates. Energy reclamation was quantified by comparing the power dissipated by the resonator against that of a standard square-wave driver; the capacitive bank yielded a recovery ratio of 1.77, while the adder block achieved 1.41. Earley noted that any metric exceeding unity would demonstrate feasibility, and the reported figures comfortably surpass that threshold, confirming the underlying principle.

By operating in an adiabatic regime, the chip keeps transistor switching within thermal equilibrium, allowing the ½ CV^2 energy stored in gate capacitances to be reclaimed and reused in subsequent cycles. The resonator's time-varying rails eliminate residual potential differences, and a dedicated driver restores the recovered energy to the system. The passive routing scheme delivers the trapezoidal waveforms to the logic stages without resorting to conventional active clock trees, thereby preserving the reversibility of the design.

Looking ahead, Vaire plans to raise the operating frequency from the prototype's 500 MHz to 1 GHz in future iterations, a move that will test the limits of clock-distribution fidelity in a reversible architecture. The company also intends to license its resonator intellectual property to external designers, enabling a broader ecosystem of low-power, high-performance ASICs that leverage reversible computing principles. By proving that reversible computing can be realized in a commercial CMOS process, the Ice River prototype offers a concrete pathway for future processors to meet the escalating energy demands of AI workloads while mitigating the slowdown of Moore's Law.

Reversible Computing Breaks Moores Law Limits and Meets AI Workload Demands

The breakthrough at Vaire lies in the resonator that couples adiabatic switching to conventional CMOS logic. The resonator supplies a trapezoidal voltage that ramps linearly between logic states, a waveform that minimises energy dissipation by keeping the transistor gates in thermal equilibrium. During each transition the high- and low-rail voltages are synchronised so that no potential difference remains, thereby preventing the non-equilibrium states that would otherwise dissipate heat. A dedicated driver restores the recovered energy to the logic, while a passive distribution network routes the trapezoidal signals to the reversible blocks without the active components that would break reversibility.

Rodolfo Rosini, Vaire's chief executive, frames this architecture as a means of sidestepping the terminal limit that is now approaching the end of Moore's Law. He notes that the resonator design, patented by former Sandia National Laboratories scientist Mike Frank in 2023, is the missing piece that allows reversible computing to be realised in a commercial 22 nm CMOS process. By recovering energy on every clock cycle, the system can sustain the

high-throughput, data-parallel workloads that drive modern artificial-intelligence applications, even as transistor scaling slows and power budgets tighten.

Looking ahead, Vaire plans to push the resonator-enabled design to 1 GHz data rates while refining the passive clock-distribution scheme to minimise waveform distortion. Chief solutions architect Alex Fleetwood highlights that the resonator IP can be licensed to designers of ASICs that favour highly parallel workloads, such as neural-network inference engines, thereby extending the benefits of reversible computing beyond Vaire's own product line. If the technology can be scaled to commercial volumes, it would offer a new scaling law that decouples performance growth from energy consumption, a prospect that could reshape the architecture of processors for the next decade.

Founders Rodolfo Rosini and Hannah Earley Drive Commercialisation Pathways

Rodolfo Rosini, chief executive of Vaire, and Hannah Earley, chief technology officer, have steered the company from a laboratory curiosity to a commercial proposition. Rosini, a serial entrepreneur who first encountered reversible computing in 2018 after meeting former Sandia National Laboratories scientist Mike Frank, assembled a team that included Earley, then a PhD researcher in unconventional computing, and Acorn/Arm veteran Andrew Sloss. Together they recognised that, although reversible computing had long been a theoretical curiosity, the advent of AI workloads and the plateauing of transistor scaling demanded a new approach to energy efficiency. Their joint decision to pursue a CMOS-based, adiabatic architecture has positioned Vaire at the forefront of a field that has, until now, remained largely academic.

The founders have chosen to embed the reversible-isation of algorithms directly into silicon rather than rely on software rewrites. Earley explains that "no one will ever write reversible computing software from scratch unless they are named Hannah Earley," so the company is integrating reversible logic gates into the core of the chip while keeping the external interface fully conventional. This design philosophy allows existing compilers and operating systems to drive the processor without modification, thereby reducing the barrier to adoption for customers who rely on legacy codebases. By keeping the input-output protocol unchanged, Vaire can deliver the energy-recovery

benefits of reversible computing to workloads that have already been optimised for performance.

Rosini emphasises that the most attractive applications for the technology are those that demand high parallelism, such as neural-network inference engines, but he also notes that single-core designs will eventually benefit as the resonator and adiabatic switching techniques mature. The company is therefore pursuing bespoke solutions that can be customised for specific workloads, a strategy that aligns with the current industry trend toward application-specific integrated circuits. The founders see reversible computing as a means to decouple performance growth from power consumption, a proposition that could reshape the economics of processor design over the next decade.

To translate the prototype into a market-ready product, Rosini and Earley are engaging early-adopter partners across the AI and edge-computing sectors. The founders are exploring ways to share the resonator technology with external designers, enabling a broader ecosystem of low-power, high-performance ASICs that leverage reversible computing principles. Their long-term vision is that, within twenty years, every new chip will incorporate some form of reversibility—whether classical or quantum—thereby establishing a new scaling law that balances performance with energy efficiency.

Technical Challenges of Adiabatic Switching and Resonator Design

Adiabatic switching, the cornerstone of reversible computing, requires that transistor charge and discharge occur while the system remains in thermal equilibrium. In Vaire's first test chip, Ice River, the resonator is the element that captures the energy released during each transition and feeds it back into the next clock cycle. The technical challenge lies in shaping the voltage waveform so that the energy can be recovered without generating non-equilibrium states that would otherwise dissipate heat. The design team therefore adopted a linear ramp that transitions between logic levels as a trapezoidal pulse. By keeping the high and low voltage rails dynamic—bringing them to the same potential during the transition—the resonator eliminates the potential difference that would otherwise drive energy loss. This trapezoidal waveform is then propagated through the logic stages, ensuring that each transistor sees a smooth, low-dissipation transition.

The resonator's operation is tightly coupled to a driver that can replenish the recovered energy, and to a passive distribution network that routes the trapezoidal signals across the chip. Conventional clock trees, which rely on active buffers, are unsuitable because the buffers would introduce irreversible dissipation. Instead, Vaire's design uses a purely passive clock tree, a choice that introduces its own set of challenges: waveform distortion and attenuation over long interconnects. To mitigate these effects, the distribution network incorporates carefully engineered impedance matching and shielding, allowing the trapezoidal signals to maintain their integrity as they travel to downstream logic blocks. The driver, meanwhile, must be capable of accepting the recovered energy and injecting it back into the resonator with minimal loss, a task that demands precise timing control and low-leakage transistor design.

Speed and energy efficiency are inherently at odds in an adiabatic system. Ice River operates at a data frequency of 500 MHz, a figure that the team considers a proof-of-concept benchmark. The resonator's energy-recovery factor—measured at 1.77 for a capacitor array and 1.41 for an adder—demonstrates the viability of the approach, yet the designers acknowledge that the recovery factor falls short of the 2× figure predicted by simulation. Achieving a higher factor would require pushing the operating frequency closer to 1 GHz, a target that introduces additional clock-distribution complexity and tighter timing margins. The semi-manual design methodology employed for Ice River reflects the lack of automated tools for such mixed-signal, reversible-logic circuits, and underscores the need for bespoke design flows that can handle the unique constraints of adiabatic operation.

The resonator design is a core component of Vaire's intellectual property portfolio and is fabricated in a 22 nm CMOS process. By integrating the resonator directly into the silicon, the chip demonstrates that reversible computing can be realised in a mainstream semiconductor technology node. The resonator's ability to recover and recycle energy after each clock cycle is the missing link that transforms logical reversibility into practical energy savings. As Vaire moves beyond the test chip, the technical challenges of waveform shaping, passive distribution, and speed scaling will dictate the pace at which reversible computing can be commercialised in conventional CMOS substrates.

Industry Implications New Scaling Law and Future ASIC Architectures

Vaire's Ice River test chip, fabricated in a 22 nm CMOS process, has delivered an energy-recovery factor of 1.77 for a capacitor array and 1.41 for an adder, confirming that reversible logic can be realised in a mainstream technology node. The team, led by Chief Technology Officer Hannah Earley, has interpreted these results as evidence of a new scaling law that ties the efficiency of adiabatic resonator-based recovery to the operating frequency and transistor dimensions. Ice River operates at 500 MHz, a figure that Earley described as a proof-of-concept benchmark; the company is targeting 1 GHz in its next production chip, a step that will push the limits of clock-distribution and waveform integrity.

The implications for the ASIC market are substantial. By embedding a resonator that recycles the energy released during transistor switching, Vaire removes the traditional heat-generation bottleneck that has long constrained transistor density and clock speed. The passive distribution network and energy-replenishing driver that accompany the resonator allow the chip to maintain reversible operation without the active buffers that would otherwise dissipate power. This architecture opens the door to ASIC designs in which intellectual-property blocks can be positioned more flexibly, hot-spot mitigation becomes less of a constraint, and overall power budgets shrink dramatically.

Looking ahead, Vaire plans to commercialise its reversible-computing IP through a dual strategy. The company will develop its own line of chips while simultaneously licensing the resonator and driver technology to third-party designers. Chief solutions architect Alex Fleetwood has highlighted that workloads which are highly parallelisable—such as those found in artificial-intelligence inference and training—stand to gain the most from reversible logic, though single-core applications will also benefit as the technology matures. The ability to embed reversible-isation directly into hardware, rather than relying on software compilers, is expected to provide modest performance gains on existing code bases, a proposition that Rosini argues is essential for industry adoption.

Rodolfo Rosini, Vaire's CEO, has framed reversible computing as a long-term paradigm shift. He envisions a future in which every new ASIC, whether classical or quantum, incorporates reversible principles to break the

entrenched link between energy consumption and performance. The company's demonstration of a practical energy-recovery mechanism in a 22 nm process marks a pivotal step toward that vision, signalling that reversible computing may soon transition from theoretical curiosity to a cornerstone of next-generation semiconductor design.

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