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Realization of Systolic Array using Ternary Reversible Gates

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Abstract

Multi valued logic synthesis is a very promising and affluent research area at present because of allowing designers to build much more efficient computers than the existing classical ones. Ternary logic synthesis research has got impetus in the recent years. Many existing literature are mainly perceptive to the realization of efficient ternary reversible processors. This research is based on the design of a reversible systolic array, which is one of the best examples of parallel processing, using micro level ternary Toffoli gate. General architecture of the ternary reversible systolic array multiplier is shown along with example. Lower bound for the garbage outputs produced in the proposed design and the quantum cost of the entire circuit is calculated here to prove the compactness of the design.

Keywords: Garbage Output, Reversible Gate, Systolic Array, Ternary Logic, Quantum Cost.

I. INTRODUCTION

In digital design, energy loss plays a significant role. Energy dissipation is associated to non-identity of switches and materials. It has been proved that, irreversible logic computation generate $kT*ln2$ heat for every bit that is lost (where k is the Boltzmann's constant and T is the temperature) [1, 2]. Though for a room temperature T, the amount of dissipating heat is minuscule (i.e. $2.9*10^{-21}$ joules) but not irrelevant. The design that doesn't resulting information loss called reversible. Reversible logic is emerging as a flourishing area of research having its applications in different sectors such as quantum computing, nanotechnology, and optical computing etc. Again systems that perform some operations in a reversible fashion can dissipate less energy and might prove competitive today.

Reversible are circuits (gates) in which the number of inputs is equal to the number of outputs and there is a one-to-one mapping between vectors of inputs and outputs; thus the vector of input states can always be re-constructed from the vector of output states [2]. More formally, a **reversible** logic gate is a k-input, k-output (denoted $k*k$) device that maps each possible input pattern into a unique output pattern [2]. This fact also applicable for multiple-valued logic, which demonstrates several potential advantages over binary technology. Quantum technology is inherently reversible and is one of the most potential technologies for future computing systems [3].

Ternary logic synthesis research provides a new-fangled era at present. Syntheses on ternary quantum logic using basic 2-qutrit controlled gates are presented on [4, 5]. The major sub-circuit needed for ternary logic has already been proposed in many literatures. Practically important ternary circuits like adder, subtractor, encoder, decoder, multiplexer, demultiplexer, comparators has already been proposed and currently been revising in many literatures. Realization of ternary reversible/quantum adder/subtractor is given in [5]. Synthesis of ternary reversible/quantum encoder and decoder is given in [6]. Realization of ternary reversible/quantum multiplexer/demultiplexer is given in [7]. In this paper, we present a design of reversible/quantum realization of ternary systolic array which is first proposed in literature. The design is based on Toffoli gates and 2-qutrit Muthukrishnan-Stroud (M-S) gates [8].

The rest of the paper is organized as follows: Section II provides the necessary background on reversible logic along with the examples of some popular reversible gates. Section III provides the design technique for Reversible Ternary Systolic Array. Evaluation of the proposed design is presented in Section IV. The paper concludes in Chapter V. Some important references are listed in Section VI.

II. BASIC DEFINITION & LITERATURE REVIEW

In this section introduces some basic terms and definitions used in this paper and some outcome of previous researchers.

A. TERNARY QUANTUM LOGIC

A ternary, three-valued or trivalent, logic is the simplest introduction of multivalued logic which is also referred to as 3VL. To define ternary logic let $A = \{0, 1, 2\}$. A ternary logic circuit f with n input variables, $A_1, \ldots, A_n$, and n output variables, $P_1, \ldots, P_n$, is denoted by $f: A^n \rightarrow A^n$, where $(A_1, \ldots, A_n) \in A^n$ is the input vector and $(P_1, \ldots, P_n) \rightarrow A^n$ is the output vector. There are $3n$ different assignments for the input vectors. A ternary logic circuit f is reversible if it is a one-to-one and onto function (bijection). A ternary reversible logic circuit with n inputs and n outputs is also called an n-qudit ternary reversible gate.

In ternary quantum logic system the unit of memory (information) is a qutrit (quantum ternary digit). Ternary logic values of *0, 1*, and *2* are represented by a set of distinguishable different states of an object that

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represent the qutrit. After encoding these distinguishable quantities into ternary constants, qutrit states are represented by $|0\rangle, |1\rangle and |2\rangle$ respectively, and are called the computational basis states [5].

B. TERNARY GALOIS FIELD LOGIC

Ternary Galois Field (TGF) consists of the set of elements $T = \{0, 1, 2\}$ and two basic binary operations– ***addition*** (denoted by +) and ***multiplication*** (denoted by . or absence of any operator) as defined in Table I. GF3 addition and multiplication are closed, i.e., for $x, y \in T$, $x + y \in T$ and $xy \in T$. GF3 addition and multiplication are also commutative and associative, i.e., $x + y = y + x$ and $xy = yx$ (commutative), and $x + (y + z) = (y + z) + x = z + x + y$ and $x(yz) = (xy)z$ (associative). GF3 multiplication is distributive over addition, i.e. $x(y + z) = xy + xz$

Table I Ternary Galois Field (GF3) operations

+	0	1	2
0	0	1	2
1	1	2	0
2	2	0	1

•	0	1	2
0	0	0	0
1	0	1	2
2	0	2	1

C. TERNARY MUTHUKRISHNAN-STROUD GATE

Muthukrishnan and Stroud proposed a family of 2-qudit (quantum digit) *d*-valued gates, which applies a 1-qudit unitary transform on the second qudit conditional on the first qudit being $(d - 1)$. The ternary M-S gate is a controlled gate [8] where the input A is the controlling input and the input B is the controlled input. The output P is equal to the input A. The output Q is the Z transform of the controlled input B if the controlling input $A = 2$, Q is equal to B otherwise. The ternary M-S gates can be realized using liquid ion trap quantum technology as an elementary gate [8]. Therefore, we assign these gates a cost of 1.

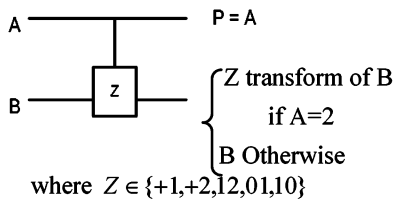

Fig. 1. Symbol of M-S gate

D. QUANTUM COST

Calculating Quantum cost of reversible circuit is a significant one. Every reversible gate can be calculated in terms of quantum cost and hence the reversible circuits can be measured in terms of quantum cost. Reducing the quantum cost from reversible circuit is always a challenging one and works are still going on in this area. In this paper we will show the quantum equivalent diagram of reversible gate that will be used to calculate the final quantum cost of proposed reversible ternary Systolic Array.

E. TERNARY TOFFOLI GATE

Ternary Toffoli gate is shown in Fig. 2(a), where its' corresponding MS implementation is shown in Fig. 2(b). If the two controlling input values are 2, then Z transform is applied on controlled input otherwise controlled input is passed unchanged. That is the outputs of the gate are $P = A$, $Q = B$, and $R = Z$ transform of C if $A = 2 \wedge B = 2$, where $Z \in \{+1,+2,12,01,10\}$; $C = Q$ otherwise.

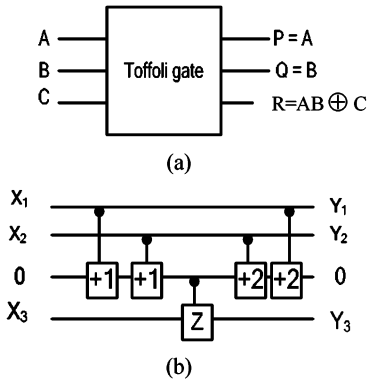

Fig. 2. 3-Qutrit ternary Toffoli gate: (a) Toffoli gate with I/O mapping (b) realization using M-S gates

Realization of this gate using M–S gates is shown in Fig. 2(b), where a constant input 0 is changed to 2 by using two +1 transforms controlled from the two controlling inputs A and B, and then the resultant constant 2 is used to control the input C [6]. The right most two gates are the inverse gates of the left most two gates used to restore the constant input 0. The quantum cost of this realization is 5.

F. GARBAGE OUTPUT

Every gate output that is not used as input to other gate or as a primary output is called garbage. The unutilized outputs from a gate are called "garbage". Heavy price is paid off for every garbage output. Suppose we want to find the Ex-OR between two variables in reversible computation, then the circuit will looks like Fig. 3. One extra output should be produced to make the circuit reversible and that unwanted output ($P=A$, marked as *) is known as garbage.

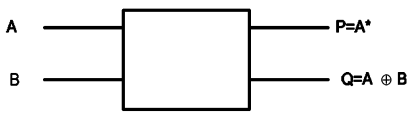

Fig. 3. The garbage output A*

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III. REALIZATION OF TERNARY SYSTOLIC ARRAY: THE PROPOSED DESIGN

Systolic array [9] is a specialized form of parallel computing. A systolic array formed by interconnecting a set of identical data-processing cells in a uniform manner is a combination of an algorithm and a circuit that implements it, and is closely related conceptually to arithmetic pipeline. In a systolic array, data words flow from external memory in a rhythmic fashion, passing through many cells before the results emerge from the array's boundary cell and return to external memory. The external memory connected to the systolic array's boundary cell stores both input data and results. Upon receiving data words, each cell performs same operation and transmits the intermediate results and data words to adjacent cells synchronously. The underlying principle of systolic array is used to achieve massive parallelism with a minimum communication overhead. The basic functional unit of a systolic array is cell which act as an autonomous processor. Cells (processors) compute data and store it independently of each other. The Fig. 4 demonstrates the elementary cell structure. The distinguish features of reversible systolic array have been discussed in many literature. The authors of the paper [10] have been illustrated the composition of fuzzy relations and describe a systolic array structure to compute that fuzzy relations on binary logic.

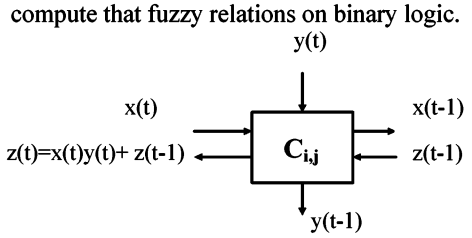

Fig. 4. Systolic array cell structure

But this paper provides a realization of ternary systolic array using M-S gate which is not introduced in any other literature in precedent.

In this paper each cell is intended to perform as a ternary systolic array operation. The function of proposed ternary systolic array processor is to execute the multiplication in pipeline fashion, which is represented by following equations:

$$z(t) = z(t-1) + x(t).y(t)$$

$$x(t) = (x_{n-1}, x_{n-2}, \ldots\ldots x_0)$$

$$y(t) = (y_{n-1}, y_{n-2}, \ldots\ldots y_0)$$

where, x is the multiplicand with n trits, y is the multiplier with n trits.

Ternary form of this equation becomes:

$$z(t) = (((a(t) * b(t)) \bmod 3 + z(t-1)) \bmod 3$$

or

$$z(t) = (z(t-1) + a(t) * b(t)) \bmod 3$$

First one is used for generating ternary performance of systolic array. From the first equation the subsequent Table II is generated.

Table II Truth Table for Ternary Systolic Array

a	b	(a*b) mod 3	z(t-1)	z(t)
0	0	0	0	0
0	0	0	1	1
0	0	0	2	2
0	1	0	0	0
0	1	0	1	1
0	1	0	2	2
0	2	0	0	0
0	2	0	1	1
0	2	0	2	2
1	0	0	0	0
1	0	0	1	1
1	0	0	2	2
1	1	1	0	1
1	1	1	1	2
1	1	1	2	0
1	2	2	0	2
1	2	2	1	0
1	2	2	2	1
2	0	0	0	0
2	0	0	1	1
2	0	0	2	2
2	1	2	0	2
2	1	2	1	0
2	1	2	2	1
2	2	1	0	1
2	2	1	1	2
2	2	1	2	0

where $z(t) = ((a*b) \bmod 3 + z(t-1)) \bmod 3$

By observing the truth table closely, we find that we can formulate Ternary Toffoli Gate as a single cell of the proposed Reversible Ternary Systolic Array. For clarity, truth table for Ternary Toffoli Gate in shown in Table III. After designing the cell, the full architecture can be realized using the same method of any conventional systolic array.

Table III Truth Table for Ternary Toffoli Gate

C\AB	00	01	02	10	11	12	20	21	22
0	0	0	0	0	1	2	0	2	1
1	1	1	1	1	2	0	1	0	2
2	2	2	2	2	0	1	2	1	0

Consider an example of 2×2 matrix multiplication.

$$\mathbf{X} = \begin{vmatrix} \mathbf{1}\,(x_{11}) & \mathbf{2}\,(x_{12}) \\ & \end{vmatrix} \quad \mathbf{Y} = \begin{vmatrix} \mathbf{1}\,(y_{11}) & \mathbf{1}\,(y_{12}) \\ & \end{vmatrix}$$

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2 (x_{21}) **1** (x_{22}) **0** (y_{21}) **2** (y_{22})

So, their resultant product is

$$\mathbf{Z} = \begin{vmatrix} \mathbf{1}\,(z_{11}) & \mathbf{2}\,(z_{12}) \\ \mathbf{2}\,(z_{21}) & \mathbf{1}(z_{22}) \end{vmatrix}$$

where $z_{11} = x_{11} \times y_{12} + x_{12} \times y_{22}$

$z_{12} = x_{11} \times y_{12} + x_{12} \times y_{22}$

And z_{21} and z_{22} is calculated by the same way.

IV. EVALUATION OF THE PROPOSED DESIGN

In this section, we will evaluate the proposed design with a Theorem and Lemma, along with examples.

Theorem 4.1 Let, the dimension of two matrices to perform systolic array are $n \times m$ and $m \times r$. If T_{GB} is the total number of garbage output generated to the realized systolic array then

$$T_{GB} >= (2n-1)\times(2n+2r-1)+ (p-(2n-1))\times(2n+2r-2)$$

where, p =total number of needed cycle.

Proof: To multiply 2 matrixes with dimension $n \times m$ and $m \times r$, we need a systolic array with $n\times(2r-1)$ cells.

Let p (the number of needed cycle) $= n\times(2r-1)-2$

Q denotes the total output = $n\times r$

T_{GB} denote the total number of garbage output generated by the systolic array.

If we consider a systolic array, we can observe that we get garbage output from three sides of a systolic structure. The side boundaries can denote by

G_L = left boundary = n

G_B = below/down/bottom boundary = $2r-1$

G_R = right boundary = n

The upper side of a systolic array is only restricted for to provide inputs.

Now consider the 1st cycle of a systolic array. In the case of 1st cycle the number of garbage output $=(n+2r-1+n)$. From the observation we see that up to $(2n-1)_{th}$ cycle the total garbage produced = $(2n-1)$ $\times(n+2r-1+n)$. Apart from first $(2n-1)_{th}$ cycle the number of garbage output produced by the other cycle = $(p-(2n-1))\times(n+2r-1+n-1)$.

So total number of garbage output produced by the systolic array

$$T_{GB} >= (2n-1)\times(n+2r-1+n) + (p-(2n-1))\times(n+2r-1+n-1)$$

$$T_{GB} >= (2n-1)\times(2n+2r-1) + (p-(2n-1))\times(2n+2r-2)$$

Example 4.1: Consider an example of 2×2 matrix multiplication. Initial state of the corresponding architecture is shown in Fig. 5. In this case the number of garbage output produced by 1st cycle is $(n+2r-1+n)=(2\times(2\times2-1)+2=2+3+2=7$

Up to (2n-1) cycle the garbage output is 7. That is for 2×2 matrix multiplication up to 3 cycles the produced garbage is 7. From the Fig. 6 we see that the $x_{11}\times y_{11}$ is produced at 2nd cycle and it appear as an output at 4th cycle (as in Fig. 8). Output of the 2nd cycle is shown in Fig. 7.

So up to 3rd cycle we get total 7 garbage output. After *(p-(2n-1))* that is, from the 4th cycle we get output from each of the left side boundary cell alternatively. From the 4th cycle to pth cycle the garbage output will be $(n + 2r - 1 + n - 1) = 6$.

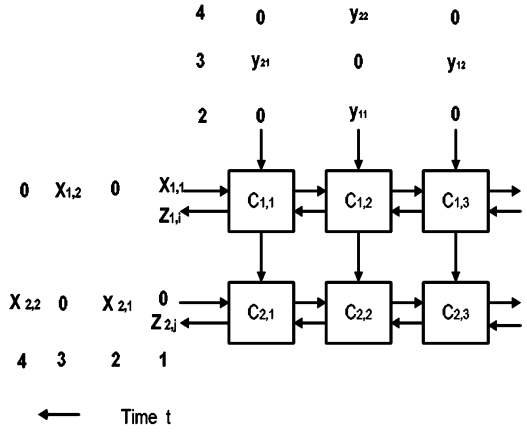

Fig. 5. Systolic array for 2×2 matrix multiplication

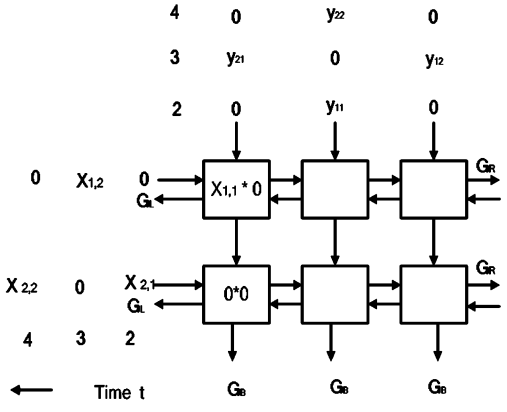

Fig. 6. The garbage output produced at 1st cycle

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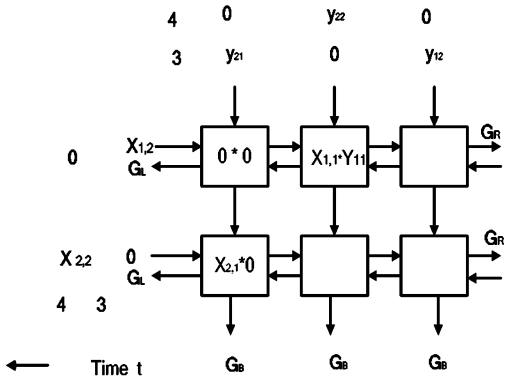

Fig. 7. The garbage output produced at 2nd cycle

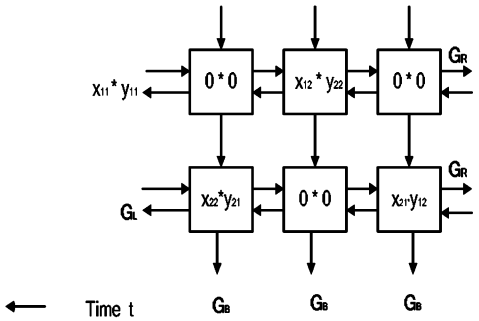

Fig. 8. First output ($x_{11} \times y_{11}$) produced at 4th cycle

Lemma 4.1: The quantum cost of a systolic array, using each cell as a Toffoli gate is 5 × C, where, C is the number of cell used in a systolic array.

Proof: As we know each quantum gate operates by manipulating qubits and and quantum cost is associated with qubits [3]. The proposed systolic array is implemented by using 3 qurit ternary Toffoli gate as a cell. The quantum cost of the used cell realization is 5. So if the number of cell required in a systolic array is C then the total quantum cost of the proposed realization is 5 ×C. □

V. CONCLUSION

In this paper, we present the realization of ternary reversible systolic array. We have developed the proposed architecture with the aid of Toffoli gate. Lower bound for Garbage output is developed very significantly to evaluate the proposed design. We haved proposed the first Ternary Systolic Array in [11], but this paper presents a procedural and step by step presentation of the idea.

VI. ACKNOWLEDGEMENT

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