CECS 361 Spring 2023

FINAL PROJECT – DIGITAL CLOCK

EDWARD RAMOS, MINH DAO, ALEX ROLDAN

Abstract

- This project is a culmination of our previous labs in the CECS digital logic series, where we implement a digital clock using the NEXYS A7 100-T board and program using Vivado software. The overall design of our project revolves around the instantiation of multiple modules, which control the different aspects of the board.

Introduction

- The purpose of this project is to program a digital clock using Verilog and to implement the design onto the NEXYS A7-100T FPGA. The clock is a standard 24-hour military time-based counter that stores real time. The clock will be displayed using the onboard 7-segment display.

- *An alternate function allows the clock to act as a stopwatch

Background & Preliminaries

- Previous Labs as example for calculating clock
- Reworked to account for user input

Functionality Inputs

Switches are used to control the clock (from least significant to most significant)

- Sw0: Reset Switch
- Sw1: Enable Switch (Starts counting)

Buttons are used to increase time

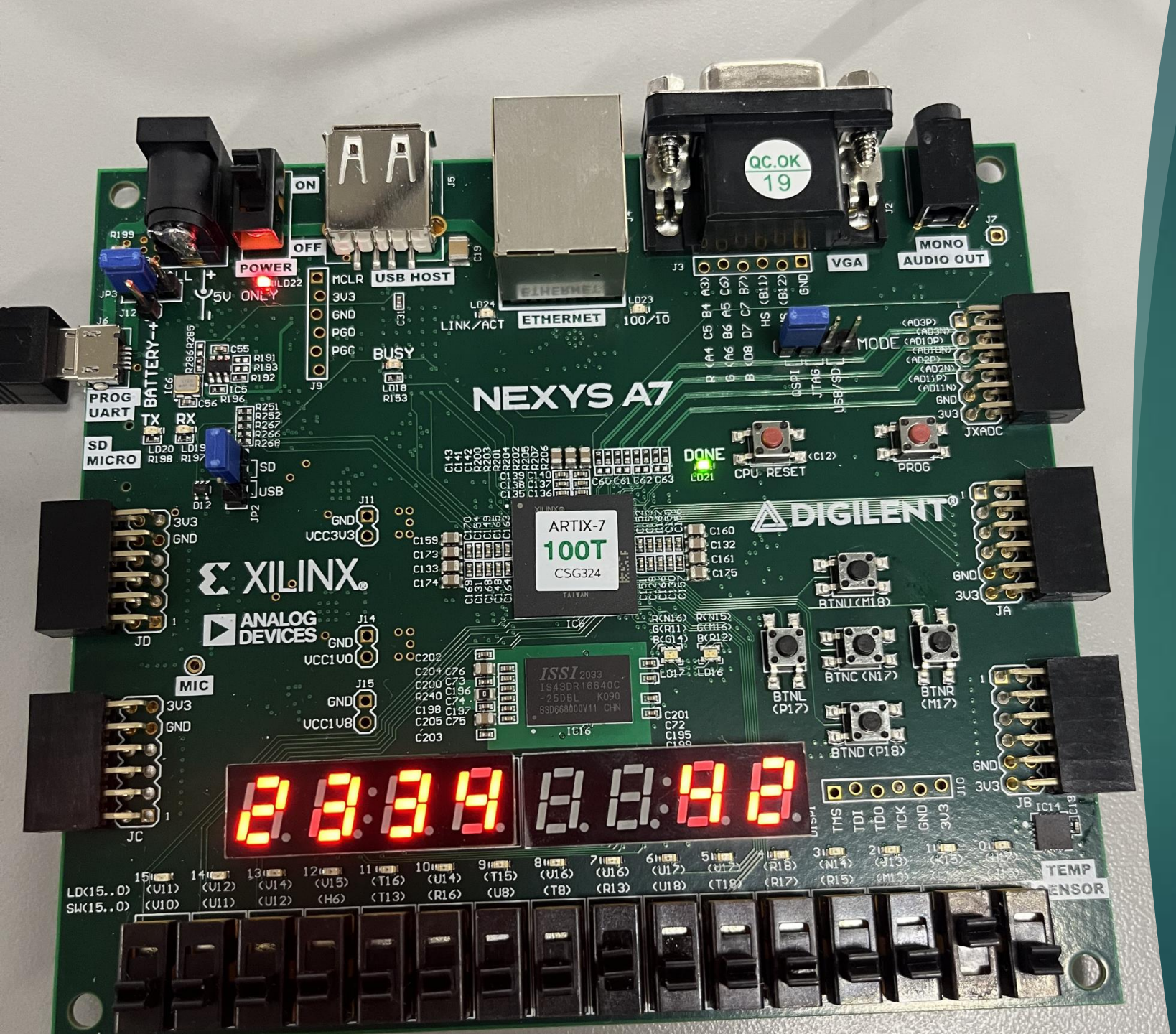
- BTN M18: Increments minute
- BTN N17: Increments hour

Functionality Outputs

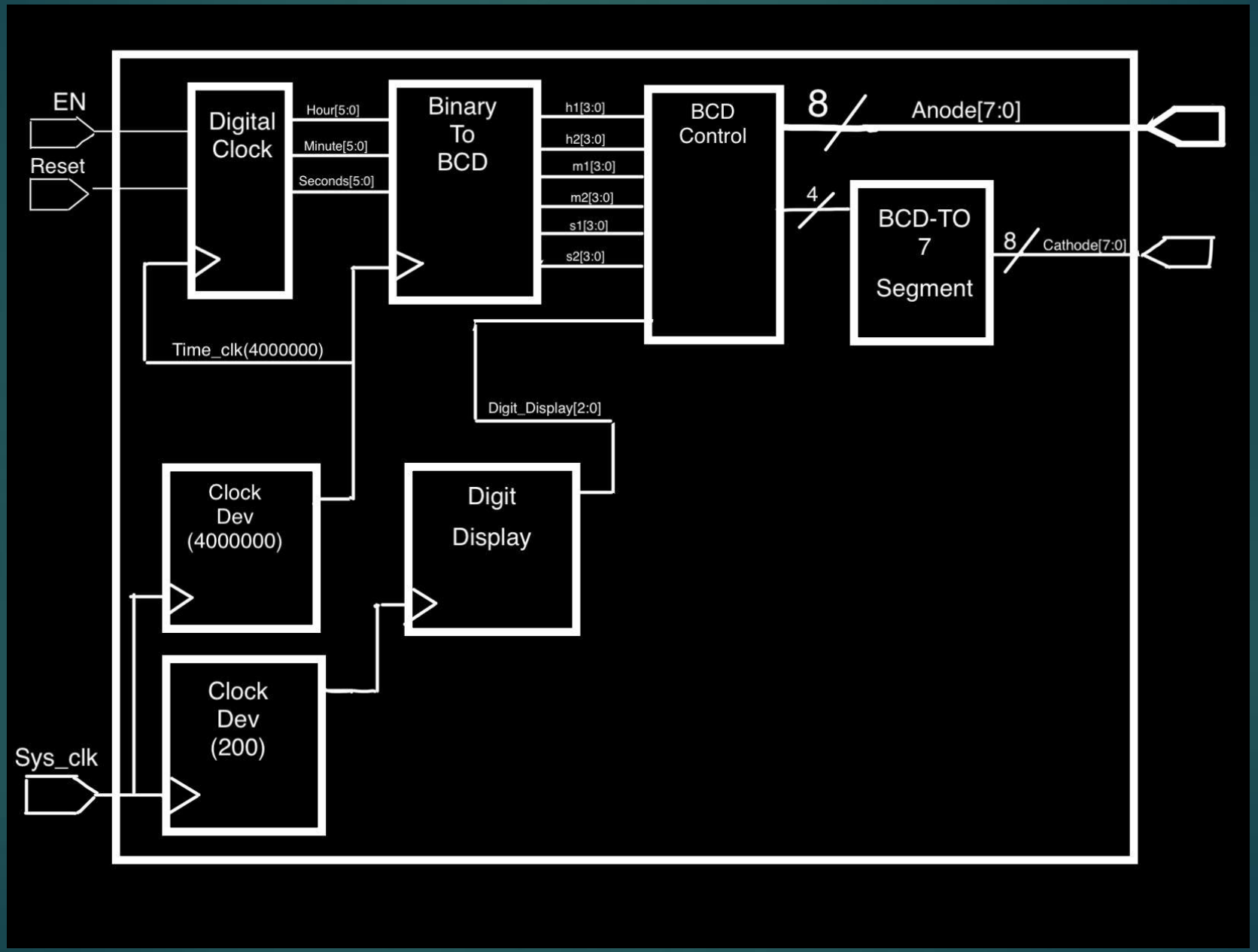
The clock is displayed using the Nexy's A7 100T 7-segment display

- Anode 4 & 5: Displays minute
- Anode 0 & 1: Displays second
- Anode 6 & 7: Displays hour

Clock is always displayed and changed according to the inputs



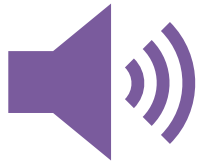
Output example


EN
Reset
Sys_clk
Digital Clock
Hour[5:0]
Minute[5:0]
Seconds[5:0]
Binary To BCD
h1[3:0]
h2[3:0]
m1[3:0]
m2[3:0]
s1[3:0]
s2[3:0]
BCD Control
8
Anode[7:0]
4
BCD-TO 7 Segment
8
Cathode[7:0]
Time_clk(4000000)
Digit_Display[2:0]
Clock Dev (4000000)
Digit Display
Clock Dev (200)

Evaluation

Time constraints/accuracy

Stopwatch record function



Audio Alarm

Blinking seperator every second