Digital Clock on FPGA 7-segment display

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***Abstract*—This project is a culmination of our previous labs in the CECS digital logic series, where we implement a digital clock using the NEXYS A7 100-T board and program using Vivado software. The clock is a standard 24-hour military time-based counter that stores real time as accurately as the board can handle. An alternate function allows the clock to function as a stopwatch with a start/stop function.**

Keywords—clock, BCD, FPGA, timer, stopwatch, display

I. Introduction

The purpose of this project is to program a digital clock using Verilog and to implement the design onto the Nexys A7-100T FPGA. The overall design of our project revolves around the instantiation of multiple modules, which control the different aspects of the board.

II. Background and Preliminaries

From our previous Digital Logic Design courses, we reused the BCD module. The BCD module was used in our previous project to display numbers on the 7-segment display by flipping specific switches. This module is applicable to our project as we will display time numbers on the 7-segment display on the Nexys A7 100t.

A. Clock

This module divides the clock signal into two new outputs. The Div value is 200 and can be changed from the top module. The counter is increased per positive edge of the input clock signal. The output clock signal toggles between 0 and 1 and the counter resets to zero after reaching the Div value. The output clock signal is set to whether the counter has reached the Div value. Overall, this module can be useful when the timing requirements of a design call for the input clock signal to be slowed down by a certain amount.

B. BCD

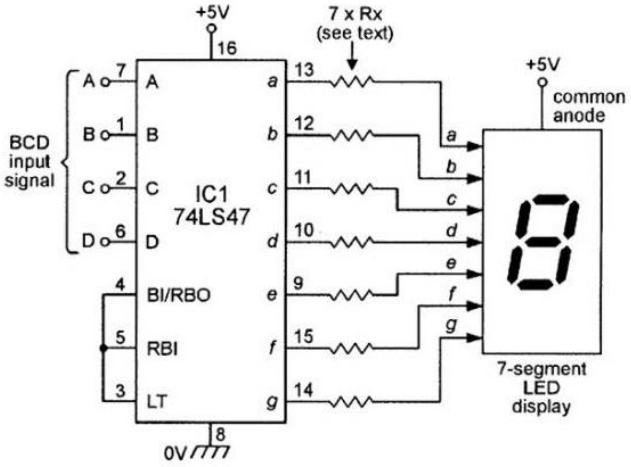
The BCD module works by taking an input Display that will output 9 different cases to the 7-segment display. The BCD to 7-segment display on the Nexys A7-100t operates by having 7 different anodes (which are the enables). The active low 0 turns on the LED. The output consists of an 8 bit cathode which controls each part of the common anodes in the BCD 7 segment display.

III. Implementation

Our design consists of a digital clock with a 7-segment display. The clock's input values are enabled, hour, reset and minute. The output will be displayed onto the 7-segment display. The digital clock is used to build the actual clock. Two clock dividers with the values of 200 and 4000000 are used to create the clock. The first clock divider generates a slow clock signal which helps refresh the display while the second is used to keep track of time. The digital display module is then utilized for the current digit to be displayed onto the 7-segment display.

A. BCD Control

To control a seven-segment display with multiple digits, use the BCD_control module. The values for each of the six digits to be displayed are represented by the six inputs, digits 1 through 6. Which digit is displayed at any given time is determined by the input Digit_Display. The value to display on the chosen digit is chosen by the output Output_Display. Which digit should be turned on is chosen by the output anode. It should be noted that this module sends the proper input signals to a different BCD_To_7seg module, which would translate the Output_Display value to the proper segment values, rather than directly controlling the segments of the seven-segment display. Based on the value of Digit_Display, a case statement in the module chooses the appropriate Output_Display and anode values. The seven-segment display's corresponding digit is activated using the anode values.



B. Binary to BCD

The Binary to BCD module will split the 6-bit input value into three values. They each will yield to the hundreds, tens, and one's places of the original input. They will be assigned to the 4-bit outputs with their respective names.

C. Anode Control

The role of the anode_control module is to controll the BCD to 7-segment display. It consisits of one input and one output. They are Digit_Display and anode. The Digit_display input takes a 2-bit value that is 10khz and checks which case should output to the anode 4-bit value.

D. Digit Display

The Digit Display module takes an input clock value amd outputs to a 3-bit Digit_Display. This will allow us to see the correct digits shown onto the display. When the Digit_Display value reaches a value of 6, it resets to 0.

E. Digital Clock

A digital clock module that displays the hour, minute, and second. When enable is activated, the clock is incremented by one every second and the second display increases by one. The Binary_to_BCD module changes the binary values of the hour, minute, and second displays into BCD format to be displayed on 7-segment displays.

IV. Evaluation

When began the project we had difficulty with displaying counted numbers to the BCD 7-segment display. After some researching, we were supposed to implement essential modules which are creating a refresh clock generator, which utilizes clock dividers. A clock divider in digital logic divides the frequency of an input clock signal. This yields a slower clock signal. The refresh clock generator periodically refreshes the board's memory. This will allow us to view the display numbers on the 7-segment display. After applying these modules, it has helped us map our design of our Digital clock.

V. Conclusion

The original concept for our project was a digital stopwatch that outputs sound once it has reached its limit (99 seconds). However, we were unable to output the sound properly, so we designed a digital clock. This project has emphasized the importance of referencing work such as old modules that we created and looking at similar designs that can help us achieve closer to our goal. The project was a success despite the challenges we faced.

References

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