ES204 Digital Systems
LAB Assignment - 4

Indian Institute of Technology, Gandhinagar
January 28, 2025

Marks : 40

Submission instructions:

Only one student from the team will submit with the word doc name Rollno1_Rollno2.pdf. The PDF will contain the code, testbench and simulation results.

For each of the questions, write a Verilog code. You also need to create a **testbench** and show the simulation results.

Smart Math Tutor Hardware

1. [20] Write a Verilog code to implement a positive edge triggered D-Flip flop with active low reset. Do you observe any difference when you use blocking vs non-blocking statements?

   Now implement the 2-bit shifter code discussed in the class with blocking and non-blocking statements and see if you observe any difference. Note your observations.

2. [20] Implement a 4-bit prime number detector using “case” statements.

   Each question should take no more than 45 mins. You can use any of structural, assignment based or procedural coding styles.