ES204 Digital Systems
LAB Assignment - 2

Indian Institute of Technology, Gandhinagar
January 15, 2025

Marks : 40

Submission instructions:

Only one student from the team will submit with the word doc name Rollno1_Rollno2.pdf. The PDF will contain the code, testbench and simulation results.

For each of the questions, write a Verilog code. You also need to create a **testbench** and show the simulation results.

Smart Math Tutor Hardware

1. [20] Write a Verilog code for 4:1 multiplexer. A 4:1 multiplexer has a, b, c, d as inputs s1 and s0 as select lines. Based on the values of [s1, s0], one of the inputs is passed to the output. Show the functional simulations for all binary combinations on input and select signals. Show also the simulation output when any of the signal is z or x.

2. [20] Write a Verilog code to implement $f(x, y, z, w) = \sum m(0,1,5,7,10)$. Show the functional simulation for all the possible cases.

Each question should take no more than 45 mins. You can use any of structural, assignment based or procedural coding styles.