

ES204 Digital Systems

LAB Assignment - 3

Indian Institute of Technology, Gandhinagar
January 21, 2025

Marks : 40

Submission instructions:

Only one student from the team will submit with the word doc name Rollno1_Rollno2.pdf. The PDF will contain the code, testbench and simulation results.

For each of the questions, write a Verilog code. You also need to create a **testbench** and show the simulation results.

Smart Math Tutor Hardware

1. [20] Write a Verilog code to implement a 1:4 demultiplexer. Check all possible cases in simulations. You can use your own variable names.
2. [20] Implement a 1-bit adder using only NAND gates. Show the simulation results for all possible combinations, and a few samples with 1'bx and 1'bz at the inputs.

Each question should take no more than 45 mins. You can use any of structural, assignment based or procedural coding styles.