1)

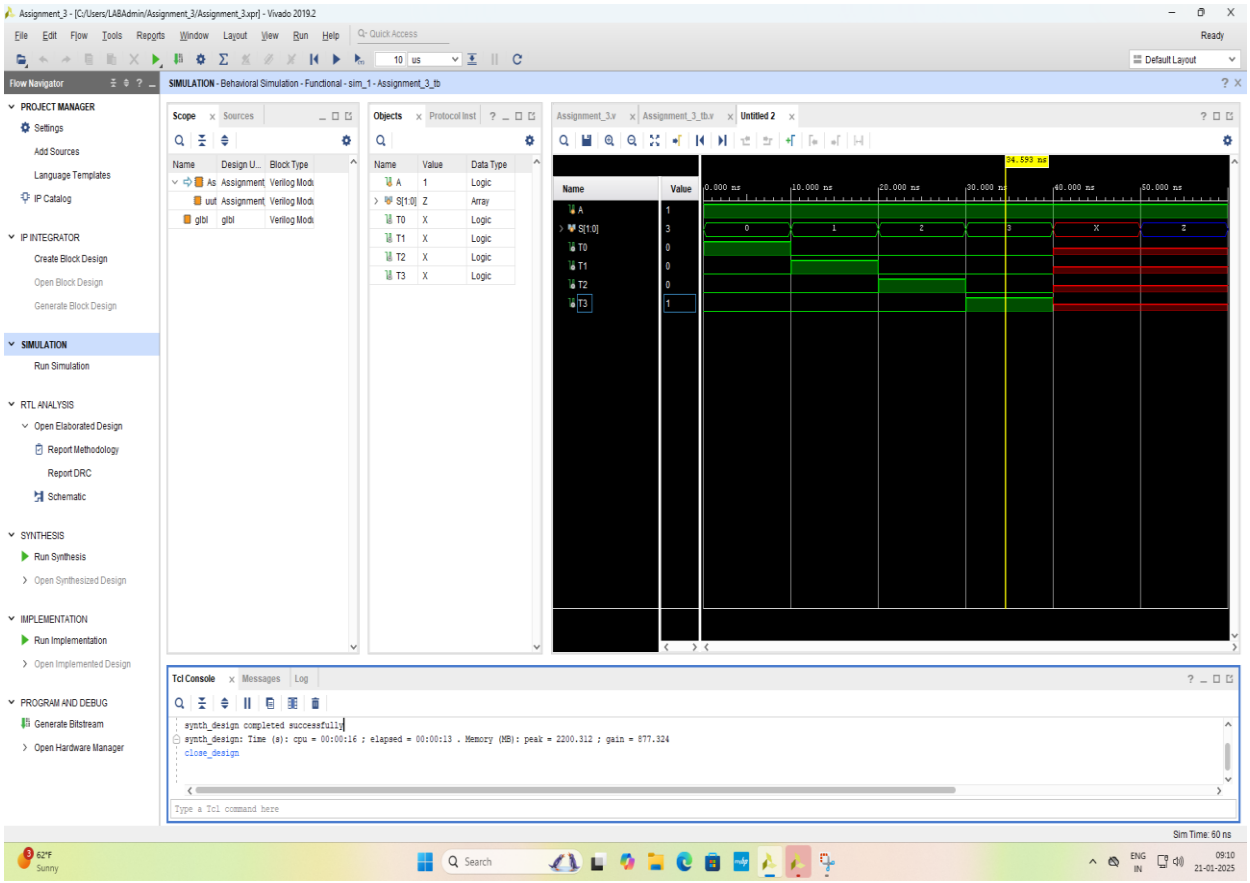
Code:

```
module Assignment_3(
input wire A,
input wire [1:0]S,
output wire T0,T1,T2,T3
);
   assign T0=(S==2'b00)?A:0;
   assign T1=(S==2'b01)?A:0;
   assign T2=(S==2'b10)?A:0;
   assign T3=(S==2'b11)?A:0;
endmodule
```

Test Bench code:

```
module Assignment_3_tb();
reg A;
reg [1:0]S;
wire T0,T1,T2,T3;
Assignment_3 uut (
   .A(A),
   .S(S),
   .T0(T0),
   .T1(T1),
   .T2(T2),
   .T3(T3)
);
   initial begin;
      A=1;S=2'b00; #10;
      A=1;S=2'b01; #10;
      A=1;S=2'b10; #10;
      A=1;S=2'b11; #10;
      A=1;S=2'bX;#10;
```

```
    A=1;S=2'bZ;#10;
    $stop();
  end
endmodule
```



2)

Code:

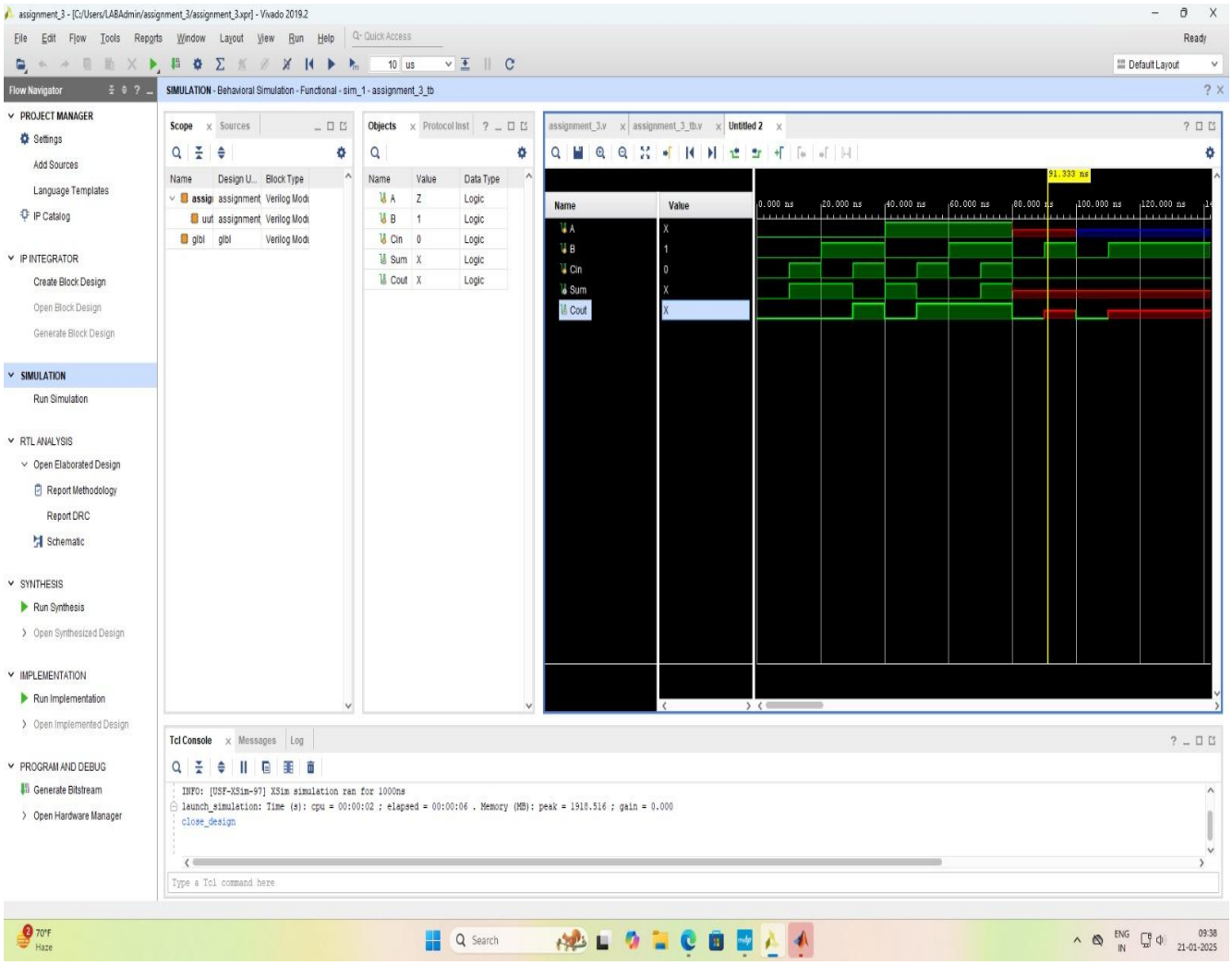
```
module assignment_3(
input A,
input B,
input Cin,
output Sum,
output Cout
);
```

```
wire n1,n2,n3,n4,n5,n6,n7,n8;


nand (n1,A,B);

nand (n2,A,n1);

nand (n3,B,n1);

wire N;          //AxorB

nand (N,n2,n3);


nand (n4,N,Cin);

nand (n5,N,n4);

nand (n6,Cin,n4);

nand (Sum,n5,n6);


nand (n7,A,B);

nand (n8,N,Cin);

nand (Cout,n7,n8);

endmodule
```

Test Bench Code:

```
module assignment_3_tb();

reg A,B,Cin;

wire Sum,Cout;


assignment_3 uut(

   .A(A),

   .B(B),

   .Cin(Cin),
```

```
    .Sum(Sum),
    .Cout(Cout)
);

    initial begin
    A=0;B=0;Cin=0;#10;
    A=0;B=0;Cin=1;#10;
    A=0;B=1;Cin=0;#10;
    A=0;B=1;Cin=1;#10;
    A=1;B=0;Cin=0;#10;
    A=1;B=0;Cin=1;#10;
    A=1;B=1;Cin=0;#10;
    A=1;B=1;Cin=1;#10;

    A=1'bx;B=0;Cin=0;#10;
    A=1'bx;B=1;Cin=0;#10;
    A=1'bz;B=0;Cin=0;#10;
    A=1'bz;B=1;Cin=0;#10;
end

endmodule
```


assignment_3 - [C:/Users/LABAdmin/assignment_3/assignment_3.xpr] - Vivado 2019.2
File Edit Flow Tools Reports Window Layout View Run Help
Quick Access
Ready
Default Layout
Flow Navigator
SIMULATION - Behavioral Simulation - Functional - sim_1 - assignment_3_tb
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
Report Methodology
Report DRC
Schematic
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager
Scope
Sources
Objects
Protocol Inst
assignment_3.v
assignment_3_tb.v
Untitled 2
Name
Value
A
B
Cin
Sum
Cout
91.333 ns
Tcl Console
Messages
Log
INFO: [USF-XSim-97] XSim simulation ran for 1000ns
launch_simulation: Time (s): cpu = 00:00:02 ; elapsed = 00:00:06 . Memory (MB): peak = 1918.516 ; gain = 0.000
close_design
Type a Tcl command here
70°F
Haze
Search
ENG
IN
09:38
21-01-2025