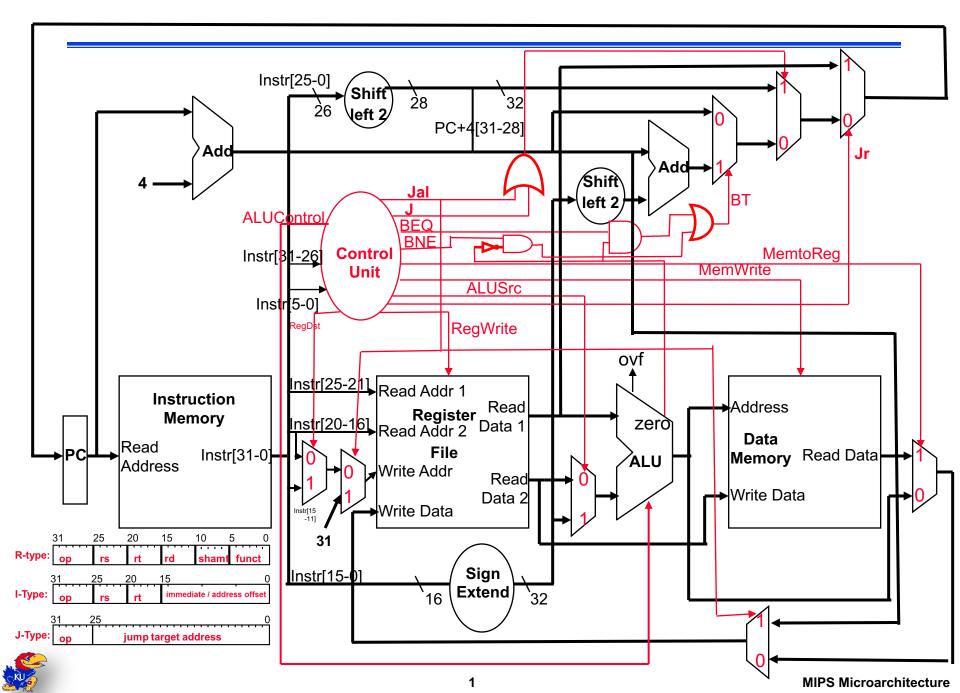
## Single-Cycle/Non-Pipelined Datapath (Modify to Support 16 Instructions)



## **Extended ALU Control (Use This Table to Complete the CU Table)**

## □ ALUControl derived from opcode and funct

Combinational logic derives ALU control

opcode	rs rt		rd	shamt	funct	
31:26	25:21	20:16	15:11	10:6	5:0	

Operation	ation opcode		ALU function	ALUControl	
AND	R-type ≡ 000000	100100	AND	0000	
OR		100101	OR	0001	
add		100000	add	0010	
subtract		100010	subtract	0110	
set-on-less-than		101010	set-on-less-than	0111	
NOR		100111	NOR	1100	
add immediate	addi ≡ 001000				
load word	lw ≡ 100011	xxxxxx	add	0010	
store word	sw = 101011				
branch on equal	beq ≡ 000100	200000	subtract	0110	
branch not equal	bne ≡ 000101	XXXXXX	Subtract	0110	
or immediate	ori ≡ 001101	xxxxxx	OR immediate	1101	
load upper immediate	lui ≡ 001111	xxxxxx	shift left 16	1111	



## **Extended Control Unit (Modify to Support 16 Instructions)**

opcode	funct	ALUControl	RegDst	ALUSrc	MemToReg	RegWr	MemWr	BEQ	J	BNE	Jal	Jr
<b>R-type</b> ≡ 000000	<b>AND</b> 100100	0000										
	<b>OR</b> 100101	0001										
	<b>add</b> 100000	0010	4	0	0	1	0	0	0	0	0	0
	<b>sub</b> 100010	0110	1			'	o o	U	U	0	U	U
	<b>slt</b> 101010	0111										
	<b>NOR</b> 100111	1100										
	<b>jr</b> 001000	0000	0	0	0	0	0	0	0	0	0	1
<b>Iw</b> ≡ 100011	xxxxxx	0010	0	1	1	1	0	0	0	0	0	0
sw ≡ 101011	xxxxxx	0010	0	1	0	0	1	0	0	0	0	0
<b>beq</b> ≡ 000100	xxxxxx	0110	0	0	0	0	0	1	0	0	0	0
<b>j</b> ≡ 000010	xxxxxx	0000	0	0	0	0	0	0	1	0	0	0
<b>addi</b> ≡ 001000	xxxxxx	0010	0	1	0	1	0	0	0	0	0	0
<b>bne</b> ≡ 000101	xxxxxx	0110	0	0	0	0	0	0	0	1	0	0
jal ≡ 000011	xxxxxx	0000	0	0	0	1	0	0	0	0	1	0
<b>ori</b> ≡ 001101	xxxxxx	1101	0	1	0	1	0	0	0	0	0	0
lui ≡ 001111	xxxxxx	1111	0	1	0	1	0	0	0	0	0	0

