NP V& P

P = class of problems for which ED

efficiently find a solution Shortest Paths

polynomial time

NP = class of problems for which efficiently verify a given solution.

NP 7. P

HAMILTONIAN
RUDRATA CYCLE

INPUT: GRAPH G= (Y,E)

Solution: Find a cycle that visits every vertex

exactly once

RUDRATA CYCUE ENP

Proof: VERIFY (Graph, a cycle)

Check if E is a Rudrata Cycle in G.

FACTORIZATION ENP

INPUT: An n-bit integer N

Soc: Some P,9 >1 integers

such that P-9= N.

Solution INPUT Verify (P, 9, N) P.9 = N

FACTORIZATION & P (general belief)

Halting 3-COL, Homiltonian Cycle NP-complete ___ NP Problems Break RSA Factorijation MST, Shortest Paths A problem A is NF complete if every problem in NP reduces to A.

REDUCTIONS: < problem B Def: Problem A (P) reduction contake polytime problem A reduces in polytime to problem B you can use an algorithm for B to solve A problem B Maxflow problem A P

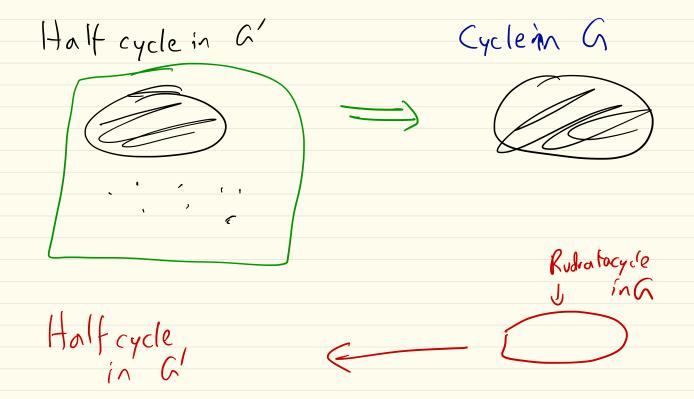
HAMILTONIAN RUDRATA CYCLE INPUT: GRAPH G= (V,E) Solution: Find a cycle that visits every vertex exactly once HALF - CYCLE INDUT : Graph G=(U,E)

INPUT: Graph G=(U,E)

Solution: Find a cycle that visits half the rodes

|V|/2

using an algorithm for B to nother A Rudvalta Half-Cycle ? same (ycle return cycle Solution Recover TUPUT ALGORITHM FOR to A B = Haf Cycle 6=(Y,E) Reduction 1) Describe reduction G= GU en disjoint vertices) Solution to B =) Soln to A 3) No sola to B => No sola to A.



NP- complete Problems 1) All of them are reducible to one another 300L < Rudiata Cycle 2) Hardust problems within NP a polytime algo for one of them
gives a polytime algo for all of NP
NP=P

CIRCUIT SAT INPUT: A boolean circuit (with n boolean & one output. An input assignment x 3.t Output of C = 1. Thm: Circuit SAT is NP-complete Mother of all NP- completens X, X,